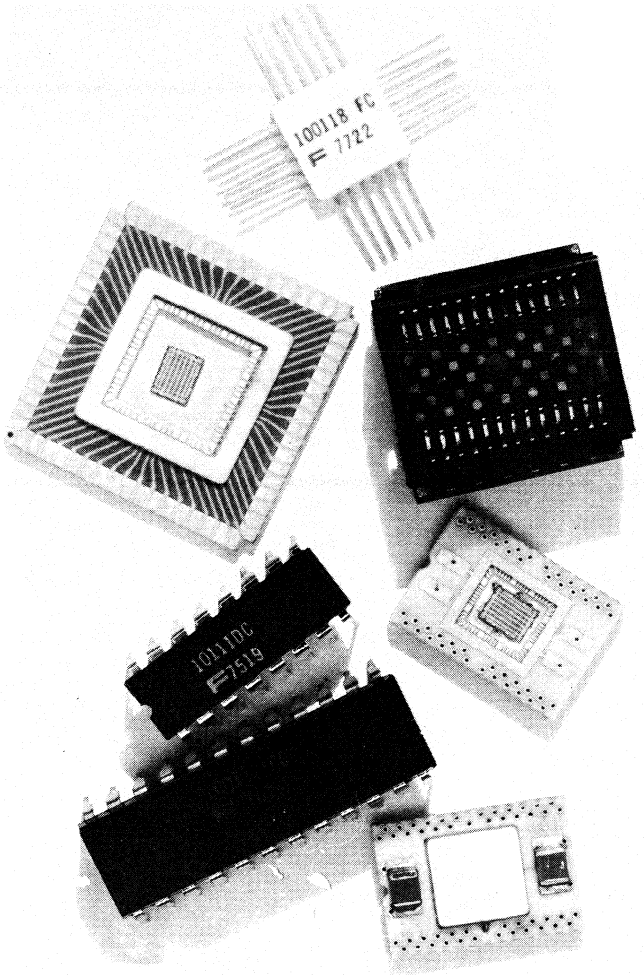
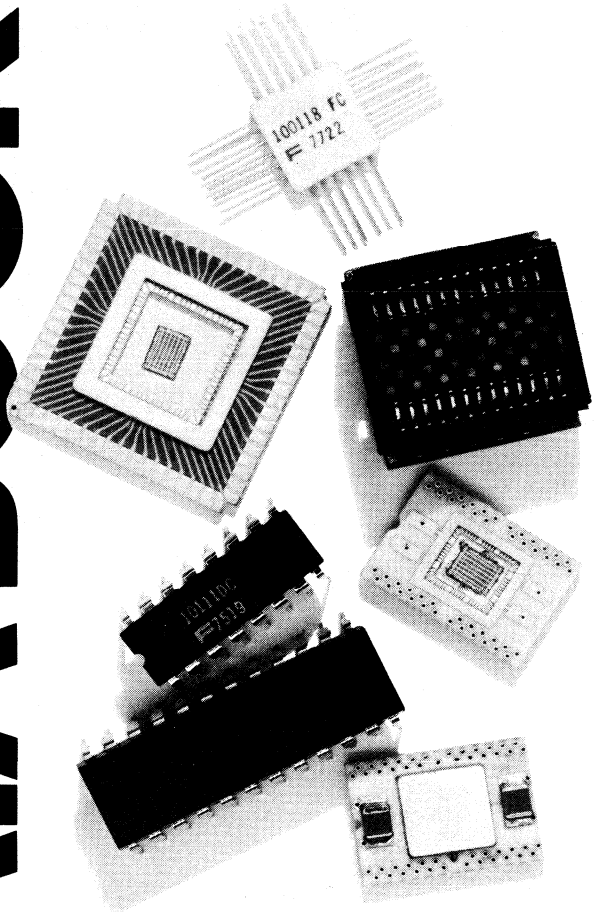


FAIRCHILD

ECL DATA BOOK



FAIRCHILD

464 Ellis Street, Mountain View, California 94042

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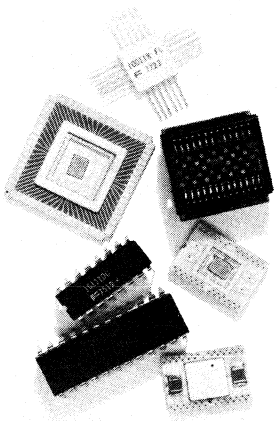
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INTRODUCTION

Most systems in operation today use TTL logic circuits. The continuing pressure for higher performance in these systems has been satisfied, in part, by the designer's ingenuity in partitioning and, in part, by selective substitution of faster TTL elements. Eventually, however, the point is reached where the extremely fast rise times cause coupling problems; the rapid current changes cause excessive impulse voltages across ground inductances; and simple interconnect wires exhibit dynamic impedance and noticeable propagation delay. At this point, some drastic rethinking is in order with due consideration for better packaging, controlled interconnection characteristics, impedance matching, and logic circuits designed for such an environment . . which brings us to the subject of this handbook, ECL.

Emitter Coupled Logic (ECL) has long been used in mainframe computers, wherein the fastest possible switching rates translate almost directly into system performance and sales. More recently, ECL usage has expanded into a broader range of applications, including those listed in the table below.

Although ECL integrated circuits have been available for a decade, their characteristics are relatively unfamiliar to many designers. A broad view of ECL characteristics is given in Chapter 1, which summarizes the key features, compares them with TTL, and points out their advantages in high speed systems. Also listed are the extra advantages of temperature and voltage compensated ECL, which make the designer's task much easier and extend the useful lifetime of a system.

Systems tend to pass through the development stage and reach production more quickly and easily when the designer is familiar with circuit input thresholds and output voltages, what determines their values, and how they are affected by supply voltage and temperature environment. Chapter 2 discusses the various internal subcircuits and their influence on circuit characteristics. It also contains a sample analysis of noise margin deterioration with adverse conditions of supply voltage regulation, distribution gradients, temperature, and voltage drops along the ground distribution.

The designer who is accustomed to forming complex functions with TTL NAND gates may, for a time, be ill at ease with ECL gates. Chapter 3 gives representative examples of duplicating TTL gate functions with ECL. Also included is a sample conversion of a TTL network to ECL, first by brute force substitution then again by more judicious use of ECL capabilities. The latter conversion is more efficient in terms of logic levels, interconnections, and package count, illustrating how ECL versatility affords greater range for the designer's ingenuity. A comparison chart in Chapter 3 illustrates that many ECL/MSI functions are quite similar to TTL elements.

Communications	**Instrumentation**	**Peripherals**
Error detection and correction	Signal generators	Add-on memories
High speed modems	Correlators	Memory control systems
Signal processors	Frequency meters	Fast Fourier processors
Data compression	Counting/timing circuits	Dedicated computers
Digital filters	Frequency synthesizers	Preprocessors
Phase-locked loops	A/D converters	

In high speed systems, the inductance, capacitance, and signal delay along interconnections cannot be ignored. The only practical way of dealing with these factors is to treat interconnections as transmission lines. Chapter 4 reviews briefly the concept of characteristic impedance and propagation constant and discusses termination mismatch, reflections and the types of waveforms to be expected in the various combinations of overtermination and undertermination at each end of a line. The relationships between rise time, line delay, and ringing are also discussed. All sample calculations and waveforms are normalized to a 1 V signal swing, which makes the quantitative results easier to understand and adapt to any logic circuit family.

In the early days of digital ICs, many designers tried ECL, only to become frustrated and give up when they couldn't get their breadboards to operate properly. From these experiences, there developed a general impression that ECL is prone to oscillation; indeed, statements to this effect still appear in print occasionally. Continued efforts, using better test equipment and distributed circuit theory, have shown that the interaction between high speed circuits and their interconnections is the decisive factor, previously overlooked. Chapter 5 extends the transmission line approach to the specific configurations, signal levels and parameter values of ECL. Various methods of driving and terminating signal lines are discussed, along with their advantages and limitations. Specific guidelines and recommendations are based on assumed worst case combinations. Many of the recommendations may seem conservative, compared to typical observations, but the intent is to help the designer achieve a reliable system in a reasonable length of time with a minimum amount of redesign.

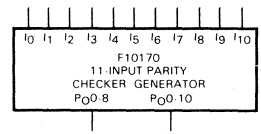
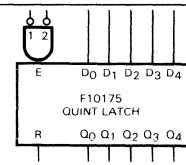
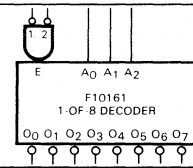
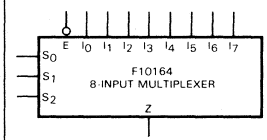
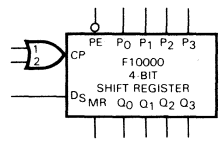
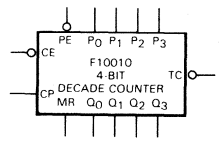
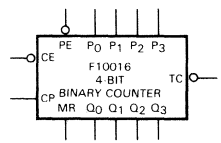
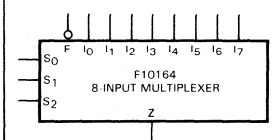
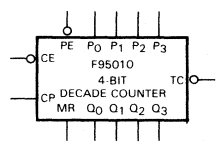
Power consumption and heat dissipation are necessarily greater with high speed circuits, due partly to circuit power drain and partly to dissipation in terminations. The increased supply currents, compared to medium speed circuits, place extra emphasis on the voltage drop along power distribution busses, including ground busses. Chapter 6 discusses methods of calculating bus resistances and estimating ground drops, and suggests general considerations regarding the relative location of communicating logic boards. Also discussed are power supply decoupling and system cooling requirements.

For convenience, a Product Information section is incorporated, making up the latter part of this handbook. Data sheets for available SSI, MSI and memory circuits are included. A list of definitions of terms and symbols is also incorporated in this section.

Logic symbols used throughout the handbook follow the positive True option of MIL-STD-806B. Symbols with unique shapes are used for the simpler functions, *e.g.,* NOR, OR, NAND, AND. MSI elements are represented by rectangular blocks with appropriate external gate symbols when necessary. A small circle at an external input means that the specific input is active LOW; *i.e.,* it produces the desired function, in conjunction with other inputs, if its voltage is the lower of the two logic levels in the system. A circle at the output indicates that when the function designated is True, the output is LOW. Generally, inputs are at the top and left and outputs appear at the bottom and right of the logic symbol. An exception is the asynchronous Master Reset in some sequential circuits which is always at the left bottom corner.

Inputs and outputs are labeled with mnemonic letters as illustrated in the table opposite. Note that an active LOW function labeled outside of the logic symbol is given a bar over the label, while the same function inside the symbol is labeled without the bar. When several inputs or outputs use the same letter, subscript numbers starting with zero are used in an order natural for device operation.

LABELING FOR ECL INPUTS AND OUTPUTS

LABEL	MEANING	EXAMPLE
I_X	General term for inputs to combinatorial circuits.	
J,K S,R D P	Inputs to JK, SR, and D flip-flops, latches, registers, and counters.	
A_X, S_X	Address or Select inputs, used to select an input, output, data route, junction, or memory location.	
E	Enable, active Low in most cases.	
PE	Parallel Enable, a control input used to synchronously load information in parallel into an otherwise autonomous circuit.	
MR	Master Reset, asynchronously resets all outputs to zero, overriding all other inputs.	
CP CE	Clock Pulse, generally a High-to-Low-to-High transition. An active High clock (no circle) means outputs change on Low-to-High clock transition. Count Enable inputs for counters.	
Z_X, O_X, F_X	General terms for outputs of combinatorial circuits.	
Q_X TC	General term for outputs of sequential circuits. Terminal Count output (1111 for up binary counters, 1001 for up decimal counters).	

DEFINITIONS OF SYMBOLS AND TERMS

The symbols and terms used in the data sheets have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits are referenced to an algebraic scale. The extremities of the scale are:

"A" the value closest to positive infinity.
"B" the value closest to negative infinity.

CURRENTS

Positive current is defined as conventional current flow *into* a device lead. Negative current is defined as conventional current flow *out of* a device lead.

I_{EE} (Power Supply Current) — The current required by each device from the V_{EE} supply. This value represents only the internal current required by the specified device, and does not include the current required for loads or terminations.

I_{IH} (Input Current HIGH) — The current flowing into a device lead with the specified V_{IH} applied to the input. This value represents the worst case dc input load that a device presents to a driving element.

I_{IL} (Input Current LOW) — The current flowing into a device lead with the specified V_{IL} applied to the input.

VOLTAGES

All voltage values are referenced to V_{CC} (or ground) which is the most positive potential in an ECL system.

V_{BB} (Bias Voltage) — The internally generated reference voltage which is used to set the input and output threshold levels.

V_{CC} (Circuit Ground) — This is the most positive potential in the ECL system and it is used as the reference level for other voltages.

V_{CS} (Current Source Voltage) — The internally generated potential used to control the level of the active current source.

V_{EE} (Power Supply Voltage) — This potential is the system power supply voltage and it is the most negative potential in the system.

V_{IH} (Input Voltage HIGH) — The range of input voltages that represents a logic HIGH level in the system.

V_{IHA} — The most positive V_{IH}.

V_{IHB} — The most negative V_{IH}. This value represents the guaranteed input HIGH threshold for the device.

V_{IL} (Input Voltage LOW) — The range of input voltages that represents a logic LOW level in the system.

V_{ILA} — The most positive V_{IL}. This value represents the guaranteed input LOW threshold for the device.

V_{ILB} — The most negative V_{IL}.

V_{OH} (Output Voltage HIGH) — The range of voltages at an output terminal with the specified output loading and with the inputs condition to establish a HIGH level at the output.

V_{OHA} — The most positive V_{OH} under the specified input and loading conditions.

V_{OHB} — The most negative V_{OH} under the specified input and loading conditions.

V_{OHC} — The output HIGH corner point or guaranteed HIGH threshold voltage with the inputs set to their respective threshold levels.

V_{OL} (Output Voltage LOW) — The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a LOW level at the output.

V_{OLA} — The most positive V_{OL} under the specified input and loading conditions.

V_{OLB} — The most negative V_{OL} under the specified input and loading conditions.

V_{OLC} — The output LOW corner point or guaranteed LOW threshold voltage with the inputs set to their respective threshold levels.

V_{NH} (HIGH Level Noise Margin) — Noise margin between the output HIGH level of a driving circuit and the input HIGH threshold level of its driven load. A conservative value for V_{NH} is the difference between V_{OHC} and V_{IHB}.

V_{NL} (LOW Level Noise Margin) — Noise margin between the output LOW level of a driving circuit and the input LOW threshold level of its driven load. A conservative value for V_{NL} is the difference between V_{ILA} and V_{OLC}.

AC SWITCHING PARAMETERS

f_{COUNT} (Count Frequency/Toggle Frequency/Operating Frequency) — The maximum repetition rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

t_{AA} (Address Access Time) — 50% points of address input pulse to data output pulse.

t_{ACS} (Chip Select Access Time) — 50% points of select pulse to data output pulse/leading edges.

t_h (Hold Time) — The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its continued recognition.

t_{PLH} (Propagation Delay Time) — The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} (Propagation Delay Time) — The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_{RCS} (Chip Select Recovery Time) — Data output pulse/trailing edges.

t_s (Set-up Time) — The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its recognition.

t_{TLH} (Transition Time, LOW to HIGH) — The time between two specified reference points on a waveform which is changing from LOW to HIGH.

t_{THL} (Transition Time, HIGH to LOW) — The time between two specified reference points on a waveform which is changing from HIGH to LOW.

t_w (Pulse Width) — The time between 50 percent amplitude points on the leading and trailing edges of a pulse.

t_W (Write Pulse Width) — 50% points of write enable input pulse.

t_{WHA} (Address Hold Time) — 50% points of address pulse to trailing edge of write enable pulse.

t_{WHCS} (Chip Select Hold Time) — 50% points of trailing edges of chip select pulse to write enable pulse.

t_{WHD} (Data Hold Time After Write) — 50% points of trailing edges of data input pulse to write enable pulse.

t_{WR} (Write Recovery Time) — 50% points of trailing edges of write enable pulse to data output pulse.

t_{WS} (Write Disable Time) — 50% points of leading edges of write enable pulse to data output pulse.

t_{WSA} (Address Set-up Time) — 50% points of address pulse to leading edge of write enable pulse.

t_{WSCS} (Chip Select Set-up Time) — 50% points of leading edges of chip select pulse to write enable pulse.

t_{WSD} (Data Set-up Time Prior to Write) — 50% points of leading edges of data input pulse to write enable pulse.

LINEAR APPLICATION TERMS

BANDWIDTH — The frequency at which the gain is 3 dB below its low frequency value.

COMMON MODE REJECTION RATIO — The ratio of a change in input common mode voltage to the resulting change in output offset voltage referred to the input.

COMMON MODE INPUT VOLTAGE RANGE — The permissible range of input bias voltage.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT OFFSET CURRENT — The difference between the currents into the two input terminals.

INPUT RESISTANCE — The resistance seen looking into either input terminal with the other tied to V_{BB}.

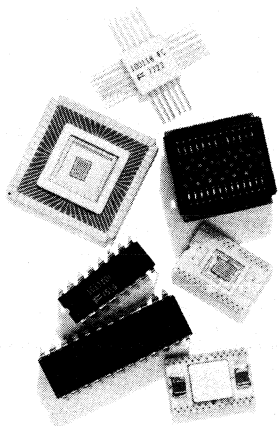
OUTPUT RESISTANCE — The resistance seen looking into an output terminal.

OUTPUT SOURCE CURRENT — Peak positive current available at an output.

OUTPUT VOLTAGE SWING — The peak-to-peak output swing that can be obtained without clipping. The output is loaded with 220 Ω to -5.2 V.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.

VOLTAGE GAIN — The ratio of the change in the output voltage to the change in voltage between the input terminals producing it.



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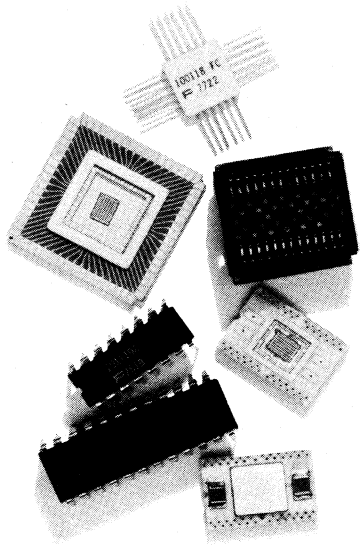
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CHAPTER 1

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Chapter 1
ECL FOR HIGH PERFORMANCE SYSTEMS

INTRODUCTION

ECL circuits incorporate features and capabilities that system designers have found offer significant advantages in high speed digital systems. These include high switching rates with moderate power consumption, short propagation delays with slow edge rates, ability to drive low impedance interconnections, compatibility with various termination methods, and wired-OR capability.

- **10,000 Series ECL** is an industry accepted, multiple-sourced ECL line offering a broad range of SSI, MSI, memory and interface elements.
- **100,000 Series ECL** is the first standard ECL line offering subnanosecond propagation delays and is accepted as the industry standard. It offers a complete line of SSI, MSI, and LSI circuit functions. It is the first line designed from its inception for easy use in systems.
- **95,000 Series ECL** is fully compensated for temperature and supply voltage variations, and offers the same functions, pinouts and operating speeds as 10,000 Series.
- **11C00 Series ECL** is a family designed specially for use in high speed communications and instrumentation applications. It offers a broad range of functions from low speed TTL interface circuits to counters with operating frequencies in excess of 1 GHz.

FEATURES AND CHARACTERISTICS

ECL is designed for use in high speed low noise systems and ECL features are particularly advantageous in these applications. Some of the features are summarized below.

Low Propagation Delays

F100K ECL features gate delays that are typically 0.75 ns with counters, registers and flip flops in the 400–500 MHz range. F10K and F95K feature 2 ns gate delays with counters, registers, and flip flops which operate in the 200 MHz range. Therefore, an ECL system can be expected to operate at speeds 2 to 6 times faster than an equivalent TTL system.

Slow Edge Rates

Because of the nature of current mode switching which uses differential comparison techniques and avoids transistor storage delays, rise times can be controlled by internal time constants without sacrificing throughput times. Slower rise times minimize ringing and reflections on interconnect wiring and simplify physical design. Typical edge rate for F10K ECL is 200 mV per ns; in comparison, the edge rate for Schottky TTL is typically six times greater. The typical edge rate for subnanosecond F100K is 1 V per ns which is only about 80% of the edge rate Schottky TTL. The rise and fall times for F10K, F100K, and F95K are typically equal to the respective propagation delays. This is considered as optimum for use in high speed systems.

Wired-OR Capability

ECL outputs can be wired together, where wiring rules permit, to form the positive True OR function thus achieving an extra level of gating without extra packages. The same technique permits data bussing and party line operations.

Complementary Outputs

Many ECL elements have complementary outputs, providing numerous opportunities for reduction of package count and power consumption when mechanizing logic equations. Further, the system incurs no extra penalty in time delay since the complementary ECL outputs switch simultaneously.

Low Output Impedance, High Current Capability

As operating speeds are increased to achieve the higher performance levels demanded of digital systems, ordinary wiring begins to exhibit distributed parameter characteristics, as opposed to a lumped capacitance nature at low speeds.

Since the distributed parameters cause the wiring to exhibit impedances in the 50 to 250 Ω range, signal edges are attenuated by the voltage divider action between the circuit output impedance and the wiring impedance.

Voltage mode circuits have a HIGH state output impedance of 50 to 150 Ω and thus exhibit an output step of about half that exhibited at low speeds, while ECL output impedance of 7 Ω assures a complete signal into the wiring impedance. Also, ECL outputs are fully specified for driving a 50 Ω load and have a rated output current capability of 50 mA; they can thus supply the quiescent current required for resistive terminations.

Convenient Data Transmission

The complementary high current outputs of standard ECL elements are well suited for driving twisted pair or other balanced lines in a differential mode, thereby enhancing field cancelation and minimizing crosstalk between subsystems.

High Common Mode Noise Rejection

Differential line receivers provide common mode noise rejection of 1 V or more for induced and ground noise. Differential receiving requires less signal swing than single-ended and is thus capable of restoring attenuated signals.

Constant Supply Current

The supply current drain of an ECL element is governed principally by one or more internal constant current sources, which supply operating currents for differential switches and level shifting networks. Since the current drain is the same in either state of the switches, ECL circuits are constant current loads on the supply.

Low Power Loss In Stray Capacitance

High frequency switching often consumes appreciable power when charging and discharging parasitic capacitance. Energy is consumed each time a capacitance is charged or discharged, so the energy loss rate, or power, goes up with switching frequency. Since the energy stored in a capacitor is proportional to the square of the voltage and ECL signal swings are four to five times less than those of TTL, power loss in stray capacitance is an order of magnitude less than with TTL.

Low Noise Generation

Power supply lines are not subjected to the large current spikes common with TTL circuits. ECL does not use a totem pole output structure, thus is free of internally generated spikes. Current spikes caused by charging and discharging stray capacitance are much smaller with ECL because of the lower signal swing and slower rise time, compared to high speed TTL.

Low Crosstalk

Since induced signals are proportional to signal swings and rise times, the lower signal swings and slower rise times of ECL result in low crosstalk levels.

Voltage Variation Insensitivity

F10K, F100K, and F95K ECL parameters are insensitive to supply voltage variation. As a result, requirements are relaxed on power supply ripple, regulation, and distribution without sacrificing noise

margins or operating speeds. ECL systems can tolerate greater variations in ac power levels, power supply regulators can be simpler and less expensive, and the physical arrangement of the dc distribution busses can be simplified.

ADDITIONAL FEATURES AND BENEFITS OF F100K AND F95K

The Fairchild F100K and F95K ECL lines add temperature and voltage compensation to the 10,000 Series functions, pinouts and nominal speeds. This gives F95K all the advantages of the 10,000 Series ECL as well as the following added features and benefits.

Easier Engineering

Designers have more confidence that the performance characteristics observed in small scale hook-ups on the lab bench will apply in the different environments expected in prototypes, in production versions, and in field operation. Considerably less effort is expended in estimating all possible extremes of temperature and supply voltage to be expected in the final system, and translating these environmental extremes into worst case variations of output levels and input thresholds, rise times and ringing, signal swing and reflections, propagation delay and timing skew, etc. Similarly, less effort is required to design both a workable power supply regulation/distribution system and an effective cooling system.

Reduced Design Time

The time required from initial development to production start-up is greatly reduced. The reduction in time required for worst case considerations, the simplification of the power system, and relaxed cooling requirements all contribute to a shorter, and therefore less expensive development cycle.

Temperature Variation Insensitivity

The complex cooling systems required to preserve noise margins, maintain speed, and control signal swings of conventional ECL are not required with F100K and F95K ECL. Output level specifications for the F100K and F95K series elements apply over the entire temperature range and the specified noise margins assume an ambient temperature gradient of $\pm 75^\circ$ C/$\pm 85^\circ$ C between one circuit acting as a signal source and another circuit receiving the signal. Thus a simpler and less costly cooling system can be used and still achieve an error-free system with high performance.

High Performance

The regulation and control of dc and ac parameters achieved by F100K and F95K ECL assures that signal timing and propagation delays in critical paths are insensitive to changes or gradients of temperature and supply voltage. Guardbands can be much narrower, yet provide a higher degree of confidence, due to the elimination of skew between output levels at one location and input thresholds at another. The consistency of response and security of noise margins permit operation at higher clock rates, increasing system performance. In some cases the temperature and voltage compensation features of F100K and F95K enable a system to operate at clock rates two times as fast as in comparable system built with incompensate ECL.

Easier Component Testing

There is no prolonged period of waiting for thermal stabilization nor any need for a complex cooling set-up to correlate with data sheet specifications when testing F95K ECL. Thus, incoming inspection testing is easier, faster, and the results more meaningful. Testing is accomplished at lower cost and greater effectiveness throughout the production lifetime of systems using F95K ECL.

Easier Debugging

Debugging is simplified and proceeds more rapidly in prototype development, production testing and in field operation. When a cabinet or other enclosure is opened for access in debugging, the resultant

change of thermal conditions has no effect on F95K ECL. Signal swings, propagation delays, edge rates and noise margins do not change, thus the altered temperature conditions do not make existing problems disappear nor create new ones.

Lower Manufacturing Costs

Savings continue to accrue during the production lifetime of the equipment, due to the less expensive power supply and cooling systems, simplified assembly of the power bussing system, easier testing of components, card assemblies, and subsystems, easier debugging, and overall reduction in manufacturing throughput time.

Less Field Service

The broader tolerance to ac power fluctuations and ambient temperature conditions in the field minimizes service calls. When field maintenance or calibration is required, procedures are simplified and less time consuming for the same reasons that make debugging easier.

More System Sales

Shorter design time places the system on the market sooner, permitting faster recovery of investment. Higher performance plus the built-in tolerance to a wider range of installation environments broadens application areas, providing a larger potential market. Lower manufacturing costs make the system competitive over a longer period of time.

ADDED FEATURES OF F100K

F100K ECL is specified to operate at -4.5 V for reduced power dissipation. If compatibility with other ECL is a requirement, F100K can be specified to operate anywhere within the range of -4.2 V and -5.7 V. This can be done with only a lower increase in power dissipation due to the voltage conpensation.

PROCESS TECHNOLOGY

F100K is manufactured using Fairchild's advanced Isoplanar II process. This process not only makes possible propagation delays of less than 1 ns, but makes possible more tightly controlled switching characteristics.

RADIATION TOLERANCE

F100K ECL manufactured using the Isoplanar II process is one of the most radiation hard I/C technologies in production. This means extended equipment lifetime of up to 50% in some applications requiring radiation hardened devices.

POWER SUPPLY

F100K ECL is specified to operate at -4.5 V for reduced power dissipation. If compatibility with other ECL is a requirement, F100K can be specified to operate any where within the range of -4.2 V and -5.7 V. This can be done with only a lower increase in power dissipation due to the voltage conpensation.

PACKAGING

F100K ECL is packaged in 24-pin packages, both flatpak and DIP. Twenty-four-pin packages were selected for the F100K family to allow for better logic density. The F100K ECL family was intended to be predominately an MSI family.

PINOUTS

F100K ECL pinouts were designed to ease and assist in system design and layout. Functional inputs which are common to all functions in a package such as Master Resets, Clocks, Enables, etc are always located on the same set of pins i.e. (pins 20, 22, 23). The input to output flow through the logic function is from one side of the package to the other. Non-inverting outputs as opposed to inverting outputs are

placed adjacant to inputs, where possible, to dominate negative feedback which reduces performance. Output pores are located, where possible, to assist in wire-or'ing. Output pores and V_{CC} pores are distributed to reduce noise generation and coupling to a minimum.

FAN-IN/FAN-OUT

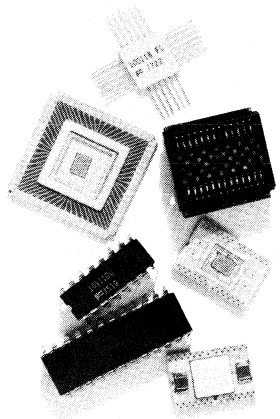
All F100K ECL outputs are specified to drive 50 Ω transmission lines which also makes them suitable for driving very high output fanouts. Unlike other logic families, all F100K inputs were designed and are specified to represent 200 more than a load of two and in most cases a load of one. This specification applies to both dc and capacitance specifications. In those places where an input goes to more than two loads an internal buffer gate has been inserted. This causes some 0.2 ns to 0.5 ns additional delay, but in a system it reduces reflected noise on signed lines and the resulting line delay.

SYSTEM DESIGN

F100K ECL was designed to be the ultimate in standard I/C logic families for performance. System design constraints were considered and the F100K family was designed for overall ease of system design and use while making the maximum use of the very fast propagation delays available.

LSI

F100K ECL is being expanded. All planned expansion is into LSI functions with up to 1000 gate complexity.



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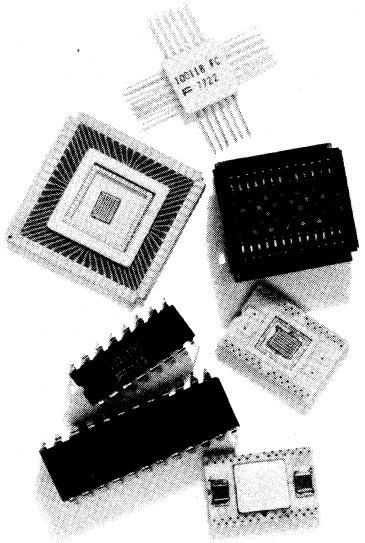
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CHAPTER 2

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- Basic ECL Switch
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- Multiple Inputs
- Power Conservation, Complementary Functions
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- The Current Source, Output Regulation
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- Mixing F10K and Conventional 10,000 Series Circuits
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Chapter 2
ECL CIRCUIT BASICS

INTRODUCTION

ECL circuits, except for the simplest elements, are schematically formidable and many of the specified parameters are relatively unfamiliar to system designers. The relationships between external parameters and internal circuitry are best determined by individually examining the fundamental subcircuits of a simple element. System variables such as supply voltage tolerances and temperature have predictable effects on circuit parameters, thus allowing a systematic evaluation of noise margins. A discussion of mixing F10K and conventional 10,000 circuits emphasizes their compatibility.

BASIC ECL SWITCH

At the bottom of every ECL circuit, literally and figuratively, is a current source. In the basic ECL switch *(Figure 2-1),* a logic operation consists of steering the current through either of two return paths to V_{CC}; the state of the switch can be detected from the resultant voltage drop across R1 or R2. The net voltage swing is determined by the value of the resistors and the magnitude of the current. Further, these two values are chosen to accomplish the charging and discharging of all of the parasitic capacitances at the desired switching rate.

REQUIRED INPUT SIGNAL

The voltage swing required to control the state of the switch is relatively small due to the exponential change of emitter current with base-emitter voltage and to the differential mode of operation. For example, starting from a condition where the two base voltages are equal, which causes the current to divide equally between Q1 and Q2, an increase of V_{IN} by 125 mV causes essentially all of the current to flow through Q1. Conversely, decreasing V_{IN} by 125 mV causes essentially all of the current to flow through Q2. Thus the minimum signal swing required to accomplish switching is 250 mV centered about V_{BB}. The signal swing is made larger (approximately 850 mV) to provide noise immunity and to allow for differences between the V_{BB} of one circuit and the output voltage levels of another.

TRANSITION REGION

If the voltage at the collector of Q1 is monitored while varying V_{IN} above and below the value of V_{BB}, the relationship between V_{C1} and V_{IN} appears as shown in *Figure 2-2.* Note that the horizontal axis of the graph is centered on V_{BB}; this emphasizes the importance of V_{BB} in fixing the location of the transition region. The shape of the transition (or threshold) region is governed by the transistor characteristics and the value of current to be switched. Both of these factors are determined by the circuit designer. The shape of the transition region is essentially invariant over a broad range of conditions, due to the matching of transistor characteristics inherent with IC technology and because the transistors are at the same temperature. The inherent matching of IC resistors assures equal voltage swings at the two collectors.

EMITTER-FOLLOWER BUFFERS

In *Figure 2-2,* V_{C1} ranges from V_{CC} (gnd) when Q1 is off to approximately −0.98 V when Q1 is conducting all of the source current. To make these voltage levels compatible with the voltages required to drive the input of another current switch, emitter followers are added as shown in the buffered current switch *(Figure 2-3).* In addition to translating V_{C1} and V_{C2} downward, the emitter followers also isolate the collector nodes from load capacitance and provide current gain. Since the output impedance of the emitter followers is low (approximately 7 Ω), ECL circuits can drive transmission lines — coaxial cables, twisted pair, and etched circuit — having characteristic impedances of 50 Ω or less.

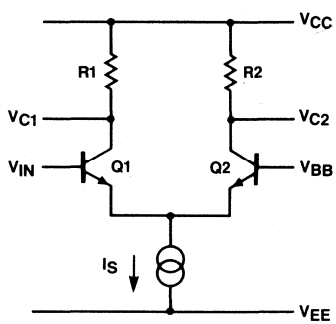


Fig. 2-1 Basic ECL Switch

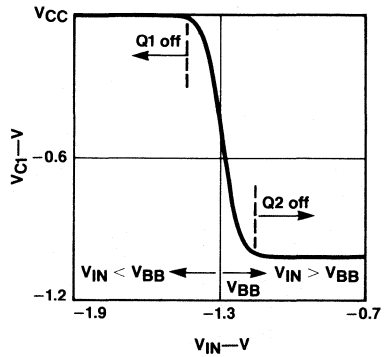


Fig. 2-2 V_{C1}-V_{IN} Transition Region

In this buffered current switch, the collectors of Q3 and Q4 return to a separate V_{CC} lead. This separation insures that any changes in load currents during switching do not cause a change in V_{CC2} through the small but finite inductance of the V_{CC1} bond wire and package lead. Outside the package, the two V_{CC} leads should be connected to the common V_{CC} distribution.

For internal functions of complex circuits where loading is minimal, the buffer transistors are scaled down to maintain high switching speeds with modest source currents. For service as output buffers, the emitter followers are designed for a maximum rated output current of 50 mA. For standardization of testing, detailed specifications on guaranteed min/max output levels apply when an output is loaded with 50 Ω returned to −2 V. The emitter followers have no internal pull-down resistors; consequently, there is maximum design flexibility when optimizing line terminations and using wired-OR techniques for combinatorial logic or data bussing.

MULTIPLE INPUTS

The buffered switch of *Figure 2-3* is essentially an ECL line receiver circuit with the bases of both Q1 and Q2 available for receiving differential signals. With one input connected to the V_{BB} terminal, the switch can receive a signal transmitted in a single-ended mode or it can act as a buffer or logic inverter. To perform the OR and NOR of two or more functions, additional transistors are connected in parallel with Q1 as indicated in *Figure 2-4*. When any input is HIGH, its associated transistor conducts the source current and Q2 is turned off; this causes the collector of Q1 to go LOW and the collector of Q2 to go HIGH, with the emitters of Q3 and Q4 following suit. When two or more inputs are HIGH, the results are the same. Thus, with a HIGH level defined as a True or logic One signal, Q3 provides the NOR of the inputs while Q4 simultaneously provides the OR. In addition to the logic design flexibility afforded by the availability of both the assertion and negation, the Q3 and Q4 outputs can drive both conductors of a differential pair for data transmission. Also shown in *Figure 2-4* are the bleeder resistors, nominally 50 kΩ, connected between ECL inputs and the negative supply. These resistors serve the purpose of holding unused inputs in the LOW state by sinking I_{CBO} current and preventing the buildup of charge on input capacitances. Accordingly, most non-essential ECL inputs are designed to be active HIGH. When such inputs are not used, the bleeder resistors eliminate the need for external wiring to hold them LOW.

POWER CONSERVATION, COMPLEMENTARY FUNCTIONS

Power dissipation in an ECL circuit is due in part to the output load currents and in part to the internal operating currents. Load currents depend on system design factors and are discussed in Chapter 6. In the

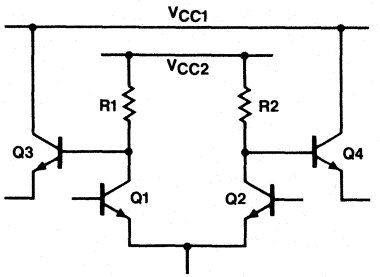


Fig. 2-3 Buffered Current Switch

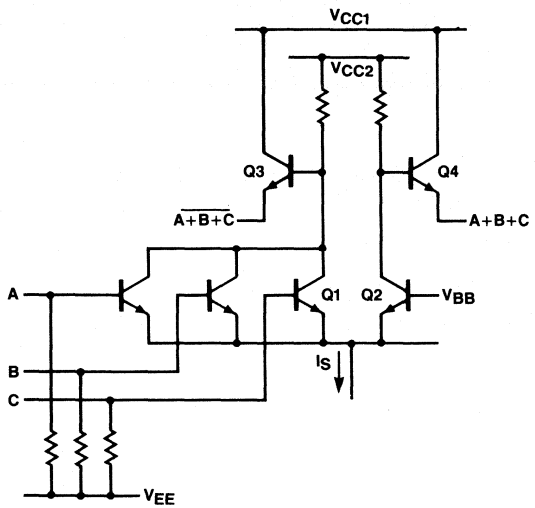


Fig. 2-4 Input Expansion by Parallel Transistors

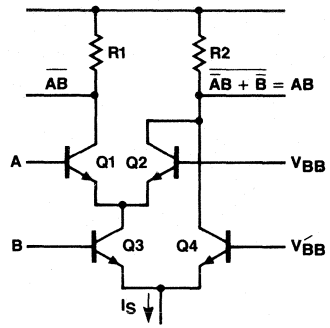


Fig. 2-5 Series/Parallel Gating

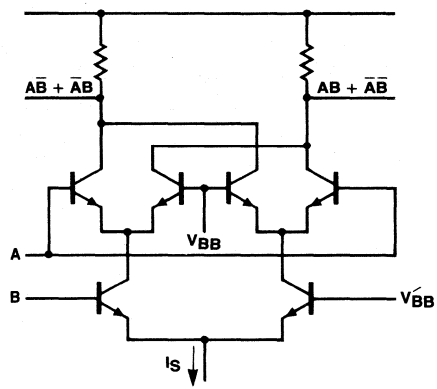


Fig. 2-6 Exclusive OR/NOR

basic switch *(Figure 2-1),* power dissipation is fixed by the source current and the supply voltage, whether the circuit is in a quiescent or a transient state. There is no mechanism for causing a current spike such as occurs in TTL circuits, and thus the power dissipation is not a function of switching frequency.

A distinct advantage of the ECL switch is the ease of forming both the assertion and negation of a function without additional time delay or complexity. This is very significant in complex MSI functions, since it helps to maximize the efficiency of the internal logic while minimizing chip area and power consumption. Since many of the ECL elements have complementary outputs, the system designer has similar opportunities to reduce package count and power consumption while enhancing logic efficiency and reducing throughput times.

SERIES GATING, WIRED AND

Quite often in ECL elements, the circuitry required to generate functions is much simpler than the detailed logic diagrams suggest. In addition to readily available complementary functions and the wired-OR option, other techniques providing high performance with low part count are series gating and wired collectors. These are illustrated in principle by the simplified schematics of *Figure 2-5* and *2-6.*

In *Figure 2-5,* if both A and B are HIGH, then Q1 and Q3 conduct and I_S flows through R1, making the collector of Q1 go LOW, thereby achieving the NAND of A and B. Connecting the collectors of Q2 and Q4 to the same load resistor provides the AND of A and B. If the collectors of Q3 and Q4 were interchanged, a different pair of functions of A and B would be produced. Similarly, a third functional pair is achieved by

interchanging the collectors of Q1 and Q2. For Q3 and Q4 to operate at a lower voltage level than Q1 and Q2, the voltage level of B is translated downward from the normal ECL levels and V'_{BB} is similarly translated downward from the V_{BB} voltage. In the slightly more complex circuit in *Figure 2-6,* another pair of transistors is added to obtain the Exclusive OR and Exclusive NOR functions.

Connecting transistors in series is not limited to two levels of decision making; three levels are shown in the simplified schematic of an octal decoding tree *(Figure 2-7).* If the three input signals are all HIGH, Q1 conducts through Q9 and Q13 to make the collector of Q1 LOW. In all, there are eight possible paths through which the source current can return to the positive supply. A LOW signal at the collector of any one of the transistors in the top row represents a unique combination of the three input signals. This 1-of-8 decoding circuit illustrates very clearly how ECL design techniques make the most efficient use of components and power to generate complex functions. This same set of switches, with the upper collectors wired in two sets of four collectors each, generates the binary sum and its complement of the three input signals.

THE CURRENT SOURCE, OUTPUT REGULATION

All elements of the F10K, F100K and F95K series use a transistor current source illustrated in *Figure 2-8.* Source current is determined by an internally generated reference voltage V_{CS}, the emitter resistor R_S and the base-emitter voltage of Q5. The reference voltage is designed to remain fixed with respect to the negative supply V_{EE}, which makes I_S independent of supply voltage.

Regulating the current source simplifies system design because output voltage and switching parameters are not sensitive to V_{EE} changes. Output voltage levels are determined primarily by the voltage drops across R1 and R2 resulting from the collector currents of Q1 and Q2. Since the collector current of the conducting transistor (Q1 or Q2) is determined by I_S and the transistor α, the voltage drop across the collector load resistor is not sensitive to V_{EE} variations. For example, a 1 V change in V_{EE} changes the output level V_{OL} by only 20 mV.

Switching parameters are affected by transistor characteristics, the collector resistor (R1 or R2), stray capacitances, and the amount of current being switched. In other forms of ECL where source currents change with V_{EE}, switching parameters are directly affected. This sensitivity is eliminated in F10K and F95K circuits by regulating I_S against V_{EE} changes.

Power dissipation in an ECL switch is the product of I_S and V_{EE}. By holding I_S constant with V_{EE}, incremental changes in dissipation are linear with V_{EE} changes. In non-regulated ECL, I_S increases with V_{EE}, causing switch dissipation to change more rapidly with V_{EE}.

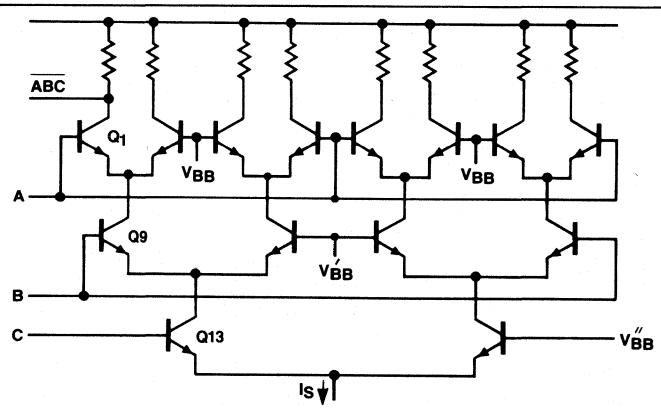


Fig. 2-7 Octal Decoding Tree

In the F10K circuits, the output voltage levels go more positive as temperature increases. Change rates for V_{OH} and V_{OL} are approximately 1.5 and 0.7 mV/°C, respectively. In F100K and F95K circuits, output voltage levels are regulated with temperature, discussed later under temperature compensation.

THRESHOLD REGULATION

As previously discussed, the input threshold region of an ECL switch is centered on the internal reference V_{BB}. In F10K, F100K and F95K elements, the on-chip bias driver holds V_{BB} constant with respect to V_{CC}, thus minimizing changes in input thresholds with V_{EE}. For a V_{EE} change of 1 V, for example, V_{BB} changes by approximately 10 mV.

With output voltage levels and input thresholds regulated, F10K, F100K and F95K circuits tolerate large differences in V_{EE} between a driving and a receiving circuit and still maintain good noise margins. For example, a driving circuit operated with −4.7 V and receiving circuit operated with −5.7 V experience a LOW state noise margin loss of only 15 to 20 mV, compared to the ideal case of both circuits with V_{EE} = −5.2 V. This insensitivity to V_{EE} simplifies the design of system power distribution and regulation.

In F10K circuits, V_{BB} goes more positive, at a rate of approximately 1.1 mV/°C, as temperature increases. Since the transition region is centered on V_{BB}, the input thresholds change with temperature at the same rate.

TEMPERATURE COMPENSATION

The output levels and input thresholds of F10K circuits vary with temperature as do those of conventional 10,000 series circuits. In F100K and F95K circuits, input thresholds are made insensitive to temperature by regulating V_{BB}. Output voltage levels are made insensitive to temperature by a correction factor designed into the current source and by a simple network connected between the bases of the output transistors as shown in *Figure 2-9.*[1-5]

With Q1 conducting and Q2 off, most of the source current flows through R1, while a small amount flows through R2, D1 and R3. If the chip temperature increases, the source current is made to increase, causing an increase in the voltage drop across R1 of sufficient magnitude to offset the decrease in base-emitter voltage of Q3. The voltage drop across R1 increases with temperature at the rate of approximately 1.5 mV/°C, while the voltage drop across D1 decreases at the same rate. This means that there is a net

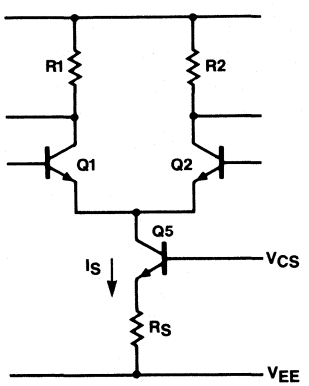


Fig. 2-8 Constant Current Source for a Switch

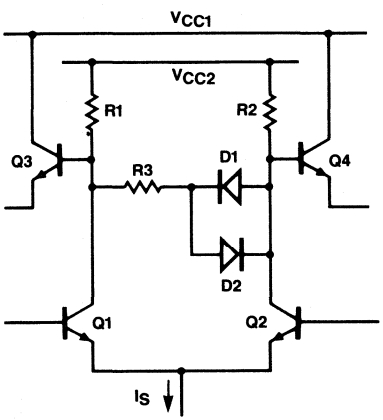


Fig. 2-9 Temperature Compensation

voltage increase of 3 mV/°C across the series combination of R2 and R3. This increase is equally divided between the two resistors since R3 is equal to R2 (and R1); thus the voltage at the base of Q4 goes negative by 1.5 mV/°C, offsetting the decrease in the base-emitter voltage of Q4. When Q2 is on and Q1 is off, the same relationships apply except that most of the current flows through R2, and D2 conducts instead of D1. F100K and F95K change rates for V_{OH}, V_{BB}, and V_{OL} are approximately 0.06, 0.08 and 0.1 mV/°C, respectively.

The stabilization of output levels against changes in temperature provides significant advantages to both the user and manufacturer. In testing, an extended thermal stabilization period is not required, nor is an elaborate air cooling arrangement necessary to obtain correlation of test results between user and supplier. In a system, the output signal swing of a circuit does not depend on its temperature, nor do temperature differences cause a mismatch in signal levels between various locations. With temperature gradients thus eliminated as a system constraint, the design of the cooling system is greatly simplified.

NOISE MARGINS

The most conservative values of ECL noise margins are based on the dc test conditions and limits listed on the data sheets. Acceptance limits on V_{OH} and V_{OL} are identified on a symbolic waveform in *Figure 2-10,* with the boundaries of the input threshold region also identified. The HIGH state noise margin is usually defined as the difference between V_{OHB} and V_{IHB}, with the LOW state margin defined as the difference between V_{OLA} and V_{ILA}. These two differences are identified as V_{NH} and V_{NL} respectively. The worst case input and output test points are also identified on the OR gate transfer function shown in *Figure 2-11.* The transition region indicated by the solid line is applicable when the internal reference V_{BB} has the design center value of −1.29 V for F10K (at +25°C) or −1.32 V for F100K and F95K circuits. The transition regions indicated by the dashed lines represent the lot-to-lot displacement resulting from the normal production tolerances on V_{BB}, which amount to ±60 mV and ±40 mV for F10K and F100K circuits respectively. Using F10K circuit values as an example, the dashed curve on the right correlates with a V_{BB} value of −1.23 V, and the input test voltage V_{IHB} is −1.105 V, for a net difference of 125 mV. Similarly, the dashed curve on the left applies when V_{BB} is −1.35 V, with V_{ILA} specified as −1.475, which also gives a net difference of 125 mV. The points V_{IHB}, V_{OHC} and V_{ILA}, V_{OLC} are commonly referred to as the *corner points* because of their location on the transfer function of worst case circuits.

In actual system operation, the noise margins V_{NH} and V_{NL} are quite conservative because of the way V_{IHB} and V_{ILA} are defined. From the transfer function of *Figure 2-11,* for example, V_{IHB} is defined as a value of input voltage which causes a worst case output to decrease from V_{OHB} to V_{OHC}. This change in V_{OH} amounts to only 20 mV for F10K circuits or 10 mV for F100K circuits. Thus, if a worst case OR gate has a quiescent input of V_{OHB}, a superimposed negative-going disturbance of amplitude V_{NH} causes an output change of only 10 or 20 mV, assuming that the time duration of the disturbance is sufficient for the OR gate to respond fully. In contrast, a system fault does not occur unless the superimposed noise at the OR input is of sufficient amplitude to cause the output response to extend into the threshold region(s) of the load(s) driven by the OR gate. In general, noise becomes intolerable when it propagates through a string of gates and arrives at the input of a regenerative circuit (flip-flop, counter, shift register, etc) with sufficient amplitude to reach the V_{BB} level.

The critical requirement for propagating either a signal or noise through a string of gates is that each output must exhibit an excursion to the V_{BB} level of the next gate in the string, assuming, of course, that the time duration is sufficient to allow full response. If the excursion at the input of a particular gate either falls short of or exceeds V_{BB}, the effect on its output response is magnified by the voltage gain of the gate. On the voltage transfer function of a gate, the slope in the transition region is not, strictly speaking, constant. However, for input signal excursions of about ±50 mV on either side of V_{BB}, a value of 5.5 may be used for the voltage gain. For example, if the noise (or signal) excursion at the input of a gate falls short of V_{BB} by 20 mV, the gate output response is 110 mV less. Another useful relationship is that if the input voltage of a gate is equal to its V_{BB}, the output voltage is also equal to V_{BB}, within perhaps 30 mV.

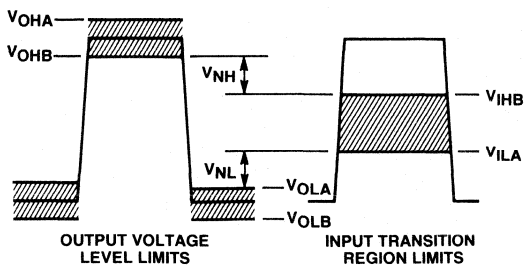


Fig. 2-10 Identifying Specification Limits on Input and Output Voltage Levels

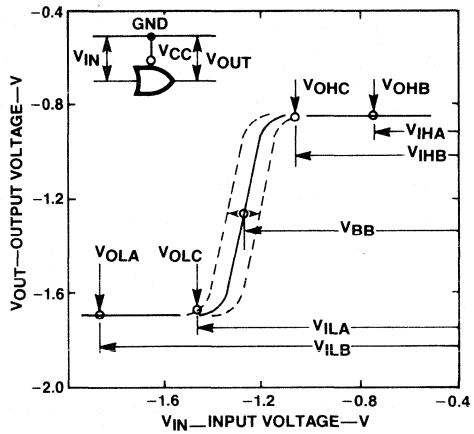


Fig. 2-11 Location of Test Points and Threshold on a Transfer Function

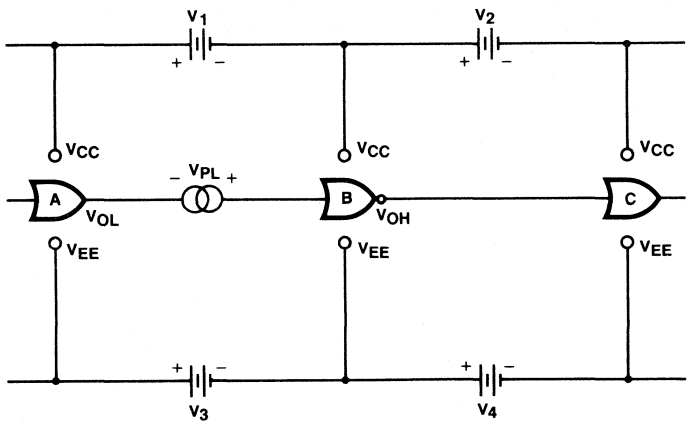


Fig. 2-12 Arrangement for Noise Propagation Analysis

To determine the combined effects of circuit and system parameters on noise propagation through a string of gates, refer to *Figure 2-12*. The voltages V_1 and V_2 represent differences in ground potential, while V_3 and V_4 are V_{EE} differences. The output of gate A is in the quiescent LOW state and V_{PL} is a positive-going disturbance voltage. Now, how large can V_{PL} be without causing propagation through gate C? For a starting point, assume all three gates are identical with typical parameters; V_{EE} is -5.2 V, the ground drops are zero, and there are no temperature gradients. Voltage parameters of F10K circuits at $+25°C$ are used. With typical circuits and the idealized environment, the maximum tolerable value of V_{PL} for propagation is the difference between the nominal V_{BB} of -1.29 V and V_{OL} of -1.75 V, or 460 mV. The following steps treat each non-ideal factor separately and the required reduction in V_{PL} is calculated.

Non-typical V_{BB} of gate B. Specifications provide for V_{BB} variations of ± 60 mV. If the V_{BB} of gate B is 60 mV more negative than nominal, V_{PL} must be reduced by the same amount.

$$\Delta V_{PL} = -60\ mV$$
$$V_{PL} = 460 - 60 = 400\ mV$$

Non-typical V_{OL} of gate A. V_{OL} limits are -1.65 to -1.85 V corresponding to the $\pm 3\sigma$ points on the distribution. Statistically, this means that 98% of the circuits have V_{OL} values of -1.68 V or lower. Since this value differs from the nominal V_{OL} by 70 mV, V_{PL} must be reduced accordingly.

$$\Delta V_{PL} = -70\ mV$$
$$V_{PL} = 400 - 70 = 330\ mV$$

Difference in ground (V_{CC}) potential between gates A and B. Since the V_{CC} lead of gate B is the reference potential for input voltages, V_1 in the polarity shown effectively makes the V_{OL} of gate A more positive. Minimizing ground drops is one of the system designer's tasks (Chapter 6) and its effect on noise margins emphasizes its importance. For this analysis, a value of 30 mV is assumed.

$$\Delta V_{PL} = -30\ mV$$
$$V_{PL} = 330 - 30 = 300\ mV$$

Difference in V_{EE} between gates A and B. In the polarity shown, V_3 reduces the supply voltage for gate A since it is assumed that gate B has V_{EE} of -5.2 V. The indicated polarities of V_1 and V_3 seem to be in conflict if it is assumed that V_3 represents only ohmic drops along the V_{EE} bus. Since V_3 may, however, be caused by the use of different power supplies or regulators as well as by ohmic drops, the polarities may exist as indicated. In any actual situation, the designer can usually predict the directions of supply current flow by observation of the physical arrangement. As mentioned earlier, a 1 V change in V_{EE} causes a V_{OL} change of 20 to 30 mV, or 2% to 3%. Assuming a value of 0.5 V for V_3 and adding the 30 mV of V_1, the net reduction in supply voltage for gate A is 0.53 V. Using 3% of this reduction as the change in V_{OL} gives a positive V_{OL} shift of 16 mV, which is a reduction of noise margin.

$$\Delta V_{PL} = -16\ mV$$
$$V_{PL} = 300 - 16 = 284\ mV$$

If the net supply voltage of gate A is assumed to be -5.2 V, then V_1 and V_3 cause gate B to have a greater supply voltage. This, in turn, causes the V_{BB} of gate B to go more negative at the rate of 10 mV/V of V_{EE} change, or 1%. Thus, for the same values of V_1 and V_3, the required reduction of V_{PL} is only 5 mV instead of the 16 mV computed above. However, if gate A is a conventional 10,000 series circuit, the rate of change of V_{OL} with V_{EE} is much greater, amounting to approximately 25%. Thus, it may not be feasible to allow V_3 to be as great as 0.5 V since the noise margin loss of 125 mV could be prohibitive. It is common practice with these types of circuits to limit V_{EE} differences to about 0.1 V, thus limiting noise margin loss to 25 mV.

Non-typical V_{BB} of gate B. This was considered earlier for its effect at the input of gate B. It must also be considered for its effect on the excursion of the output voltage of gate B. Since the net input voltage of gate B ($V_{OL} + V_{PL}$) reaches the V_{BB} level of gate B, the output excursion also extends to the V_{BB} level and perhaps 30 mV beyond (more negative). This means that the output excursion of gate B could be 90 mV more negative than the nominal V_{BB} of gate C. This excess excursion must be divided by the voltage gain of gate B to determine exactly how much V_{PL} must be reduced as compensation.

$$\Delta V_{PL} = -90/5.5 = -16\ mV$$
$$V_{PL} = 284 - 16 = 268\ mV$$

Non-typical V_{BB} of gate C. The V_{BB} of gate C could be 60 mV more positive than the nominal value of -1.29 V. Dividing by the voltage gain of gate B gives the necessary reduction of V_{PL}.

$$\Delta V_{PL} = -60/5.5 = -11\ mV$$
$$V_{PL} = 268 - 11 = 257\ mV$$

Difference in V_{CC} potential between gates B and C. For the polarity shown, V_2 makes the net voltage at the C input more negative with respect to the V_{CC} lead of gate C. Assume 30 mV for V_2 as was done for V_1.

$$\Delta V_{PL} = -30/5.5 = -5.0\ mV$$
$$V_{PL} = 257 - 5 = 252\ mV$$

Difference in V_{EE} between gates B and C. In the polarity shown, V_4 reduces the supply voltage for gate C, as does V_2. As previously mentioned, V_{BB} changes with V_{EE} at a rate of 10 mV/V, or 1%. Assuming a value of 0.5 V for V_4, as was done for V_2, adding V_2 gives a net V_{EE} reduction of 0.53 V. This makes the V_{BB} of gate C about 5 mV more positive, with respect to its own V_{CC} lead. This must also be divided by the gain of gate B to determine the effect on the permissible value of V_{PL}.

$$\Delta V_{PL} = -5.3/5.5 \simeq -1.0\ mV$$
$$V_{PL} = 252 - 1 = 251\ mV$$

If gate C is a conventional 10,000 series circuit, the V_{BB} shift with V_{EE} amounts to approximately 15%, requiring a proportionally larger reduction of V_{PL}.

At this point the more conservatively defined V_{NL} *(Figure 2-10)* should be evaluated and compared with V_{PL}. Subtracting the 25°C values of V_{OLA} and V_{ILA}, a value of 175 mV for V_{NL} is obtained. This automatically accounts for non-typical V_{OL} of gate A and V_{BB} of gate B but does not take into account V_1 and V_3. For the same assumed values of V_1 and V_3, V_{NL} must be reduced by 46 mV, giving a net value of 129 mV. Because of the way it is defined, V_{NL} is not affected by V_2, V_4 or a non-typical V_{BB} of gate C. V_{NL} is defined as the value of noise superimposed on the input of gate B that causes its output to exhibit an excursion to V_{OHC}, which is only 20 mV below the worst case quiescent output level V_{OHB}. This leaves room for negative-going noise to be induced at the input of gate C at the same time V_{NL} is present at the input to B.

The primary advantage of using V_{NH} and V_{NL} as the limits of tolerable noise is that they provide for simultaneous appearance of noise on inputs and outputs. Whatever the system designer's preference regarding noise margin definitions, the important factor is to recognize that the differences in V_{CC} and V_{EE} potentials decrease the noise margins and therefore should be minimized.

Differences in ambient temperature can also decrease noise margins. Referring again to *Figure 2-12,* if gate B is operating at +25°C but the ambient temperature of gate A goes up, then the V_{OL} of gate A goes more positive and thus reduces the noise margin at the input to gate B. The temperature coefficient of V_{OL} is approximately 0.7 mV/°C. If, for example, gate A is operating at +55°C, the noise margin is reduced by the product (0.7) (30) which is 21 mV.

Similarly, if the temperature of gate C increases, V_{BB} of gate C goes more positive at the rate of 1.1 mV/°C. If gate C is operating at +55°C, the allowable noise disturbance is reduced by 33 mV, whether the disturbance is caused by the gate B output excursion or by an independent noise source.

If the temperature gradients are reversed, *i.e.,* if gates A and C remain at +25°C but the temperature of gate B increases, there is an increase in LOW state noise margin at the input of B, because V_{BB} of B is more positive, and an increase in HIGH state noise margin at the input of C because the V_{OH} of B is more positive. The disadvantage comes when gate A changes to the V_{OH} state. In this state, the elevated V_{BB} of gate B subtracts from the HIGH state noise margin at its input. Simultaneously the elevated V_{OL} out of B decreases the LOW state noise margin at the input of gate C. It is apparent that any temperature gradient is a disadvantage because it decreases either the LOW or HIGH state noise margin. This points out the advantage of the F100K and F95K series circuits, with output levels and input thresholds only slightly affected by temperature. Data sheet test limits and conditions of F100K and F95K circuits automatically

include an assumed temperature gradient of ±75° C/±85° C between communicating circuits. If system temperature conditions are subject to wide variations, the use of F95K circuits is recommended if dynamic performance is important, the F100K is recommended.

MIXING F10K AND CONVENTIONAL 10,000 SERIES CIRCUITS

The F10K series is designed to be fully compatible with 10,000 series elements of other manufacturers. They have the same functions, pinouts, specifications, part numbers and temperature behavior. The F10K series circuits, however, tolerate a much broader range of V_{EE} gradients, regulation, and ripple without degradation of the dc and ac characteristics. If a system is designed to operate with both types of circuits, the more restrictive V_{EE} requirements of conventional 10,000 series circuits must be met.

When the two types of circuits are randomly mixed in the same system, the effects of V_{EE} variations and gradients on noise margins are not identical for all combinations of driving and receiving circuits. In the general case of two communicating circuits such as gates A and B in the arrangement for noise propagation analysis *(Figure 2-12),* there are four possible combinations of circuit types; the driver can be either an F10K or a 10,000 series and so can the receiver. If gate A is in the V_{OL} state and both gates start with a V_{EE} of −5.2 V, the LOW state noise margin decreases if the V_{EE} of gate A goes more positive, because the V_{OL} goes more positive. The V_{OL} shift is only 2% of the V_{EE} change if gate A is an F10K type, but the shift is 25% of the V_{EE} change if gate A is a conventional 10,000 series type. If the V_{EE} of gate A is held at −5.2 V and the V_{EE} of gate B goes more negative, the LOW state noise margin decreases because the V_{BB} of gate B goes more negative. This in turn, shifts the entire transition region more negative. The shift is only 1% of the V_{EE} change if gate B is an F10K type, but is 15% of the V_{EE} change if gate B is a conventional 10,000 series type. If the two supply voltages vary independently about −5.2 V, then the effects of the V_{OL} shift of gate A and the V_{BB} shift of gate B are additive, which gives the worst case loss of noise margin.

If gate A is in the V_{OH} state, its output is not affected by V_{EE} changes, assuming that the input of A is not biased in the transition region. If the V_{EE} of gate B goes more positive, the HIGH state noise margin is reduced by the positive going shift of the V_{BB} of gate B. Again, the shift is 1% of the V_{EE} change if B is an F10K circuit or 15% of the V_{EE} change if B is a conventional 10,000 series type.

In large systems designed with the conventional 10,000 series circuits, it is common practice to restrict V_{EE} tolerance to ±2% and V_{EE} gradients to 2% or less between circuits communicating in the single-ended mode. This keeps noise margin losses to manageable levels, considering that differences in temperature and V_{CC} potential must also be accommodated.

The noise margin between two circuits as a function of V_{EE} gradients is shown in *Figure 2-13* for the four possible combinations of circuit types. The margins shown are either V_{NH} or V_{NL}, whichever is least. This is in recognition of the fact that noise can be of either polarity and thus the smaller of V_{NH} or V_{NL} is the critical margin for the system. The graph assumes that both the driving and receiving circuit start with the nominal V_{EE} of −5.2 V and then the V_{EE} shifts by the same magnitude but in opposite directions at the two circuits. The horizontal axis of the graph indicates the net difference in V_{EE} between the two circuits. The mixed combinations B and C either have the same or improved noise margins compared to the conventional 10,000 series types (combination A), while the F10K combination is only slightly affected by gradients. Differences in temperature and V_{CC} potential are not considered in this graph, but they have the same effects with either type of circuit.

When V_{EE} changes in the same direction at both the driving and receiving circuit, *i.e.,* no gradient, the worst case losses of noise margin are less than in the case of a gradient. *Figure 2-14* shows noise margin as a function of ±V_{EE} tolerance. Again, the noise margins shown are the smaller of V_{NH} or V_{NL}, and differences in temperature and V_{CC} potential are not considered.

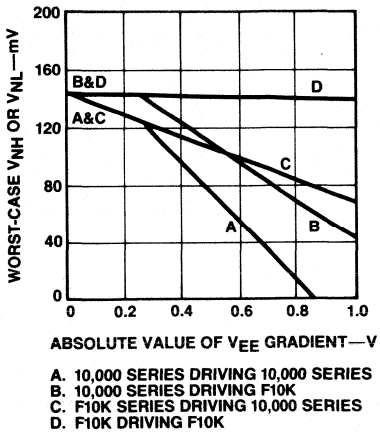


Fig. 2-13 Worst Case Noise Margin Versus V_{EE} Gradient

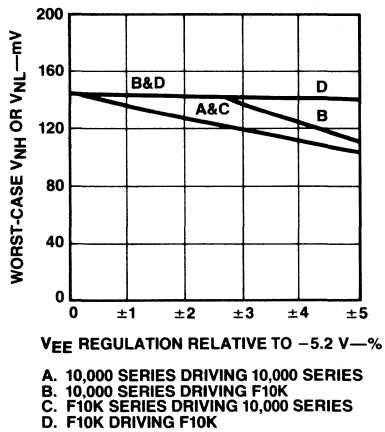


Fig. 2-14 Worst Case Noise Margin Versus V_{EE} Tolerance

RADIATION TOLERANCE

Table I presents a summary of radiation tolerances of various semiconductor processes. The oxide isolated structure of Isoplanar II makes this process the most tolerant, high volume, standard process in existance today.

TABLE I - SUMMARY OF SEMICONDUCTOR VULNERABILITY ASSESSMENT

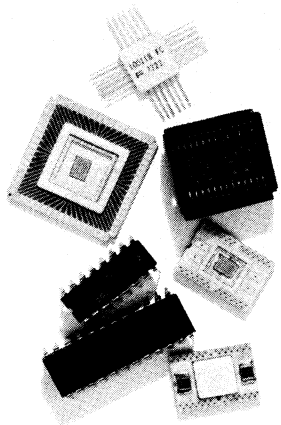
RADIATION ENVIRONMENT	Bipolar Trans. & J-FET. Discretes	SCR	TTL	LSTTL	ANALOG IC	CMOS	NMOS	LED	ISO II ECL
NEUTRONS n/cm^2	10^{10}-10^{12}	10^{10}-10^{12}	10^{14}	10^{14}	10^{13}	10^{15}	10^{15}	10^{13}	$> 10^{15}$
IONIZING TOTAL DOSE Rads (Si)	$> 10^4$	10^4	10^6	10^6	5×10^4 10^5	10^3 10^4	10^3	$> 10^5$	10^7
TRANSIENT DOSE RATE RADS (Si) /seconds (UPSET OR SATURATION)		10^3	10^7	5×10^7	10^6	10^7	10^5		$> 10^8$
TRANSIENT DOSE RATE Rads (Si) /seconds (SURVIVAL)	10^{10}	10^{10}	$> 10^{10}$	$> 10^{10}$	$> 10^{10}$	10^9	10^{10}	$> 10^{10}$	$> 10^{11}$
DORMANT TOTAL DOSE (ZERO BIAS)	$> 10^4$	10^4	10^6	10^6	10^5	10^6	10^4	$> 10^5$	$> 10^7$

TABLE II - ISOPLANAR II PRODUCTS

11C01	**F10166**	**F100117**	**F100158**
11C05	**F10170**	**F100118**	**F100160**
11C06	**F10181**	**F100122**	**F100163**
11C70	**F10210**	**F100123**	**F100164**
11C83	**F10211**	**F100130**	**F100165**
11C90	**F10212**	**F100131**	**F100166**
11C91	**F10414**	**F100136**	**F100170**
		F100141	**F100171**
		F100142	**F100179**
F10136	**F100101**	**F100145**	**F100180**
F10137	**F100102**	**F100150**	**F100181**
F10141	**F100107**	**F100151**	**F100194**
F10145A	**F100112**	**F100155**	**F100414**
F10160	**F100114**	**F100156**	**Gate Array**

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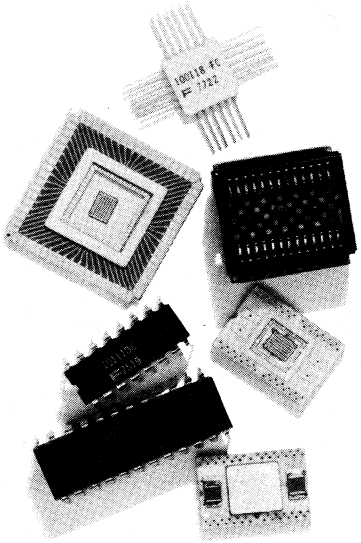
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CHAPTER 3

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- OR/NOR Gates
- OR/AND, OR/AND/INVERT Gates
- Flip-Flops
- MSI
- Converting a TTL Design to ECL

Chapter 3
ECL LOGIC DESIGN

INTRODUCTION

The 10K and 95K ECL families offer a broad line of SSI, MSI and memory functions. Basic gates and flip-flops are described, followed by design applications using ECL MSI. Finally, a few guidelines are given to help designers, already familiar with DTL and TTL, to readily convert to ECL.

Fairchild ECL logic symbols use the positive logic or "active level HIGH" option of MIL-STD-806B. Logic One is therefore by definition the most positive algebraic voltage, *i.e.*, nearest ground. Logic Zero is the most negative, nearest V_{EE}. In some cases it may be easier to think in terms of negative logic; for example, a positive logic OR is a negative logic AND. The positive and negative logic symbols for the common gating types are shown in *Figure 3-1*.

This section deals only with ECL logic design using the F10K and F95K families. These two families with typical propagation delays of 2 ns are usually the families used when a designer is making a transition from TTL to ECL. Designing with F100K logic is an extension of the rules used for F10K and F95K with many functions being more complex.

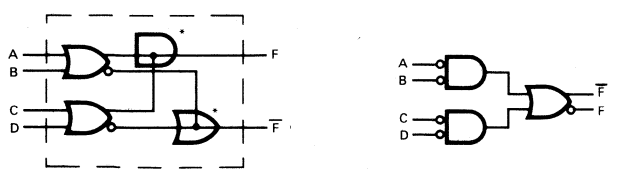
POSITIVE LOGIC **NEGATIVE LOGIC** **TRUTH TABLE**

OR/NOR



A	B	F	$\bar{F}$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	H	L

OR/AND, OR/AND/INVERT



*INTERNAL SERIES CONNECTION, NOT THE WIRED-OR

A	B	C	D	F	$\bar{F}$
L	L	X	X	L	H
X	X	L	L	L	H
H	X	H	X	H	L
H	X	X	H	H	L
X	H	H	X	H	L
X	H	X	H	H	L

EXCLUSIVE OR/NOR



A	B	F	$\bar{F}$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	L	H

H = Most Positive Voltage — HIGH
L = Most Negative Voltage — LOW
X = Don't Care

Fig. 3-1 Positive and Negative Logic Symbols for Common ECL Gates

OR/NOR GATES

The most basic ECL circuit is the OR/NOR gate *(Figure 3-2)*. If the input voltages are more negative than the reference voltage V_{BB}, Q1 and Q2 are cut off and Q3 conducts, holding the collector of Q3 low. If either input is more positive than V_{BB}, Q1 or Q2 conducts and Q3 is cut off, raising its collector voltage. Because one or more transistors always conducts, there is a constant current drain, independent of frequency, that eliminates sharp switching transients and frequency dependent power dissipation effects.

Outputs of the circuit, emitter followers Q4 and Q5, provide low impedance drive to terminated lines and voltage shifting to levels compatible with the inputs. Because of the differential nature of the input circuit, the V_{EE} supply sees a constant current load, which minimizes noise on the supply line. A single circuit, shown as a block at the base of Q3 in *Figure 3-2,* is used to generate the reference voltages for all gates on the chip.

Since the basic gate simultaneously performs the positive logic OR and NOR functions, both True and Complement outputs are provided within the same delay period of a single gate. The outputs of several gates may be tied to provide a wired-OR function. An external load resistor is necessary in all cases.

Variations among ECL OR/NOR gates are the number of gate inputs, the common inputs, and the output polarities. Note from *Figure 3-1* that AND or NAND function can be obtained by complementing the inputs. When OR gate outputs are wired-OR, the effect is to widen the OR gate *(Figure 3-3)*. This wired-OR is a True, positive logic wired-OR and should not be confused with a DTL positive logic wired-AND or internal series gating used for some ECL functions.

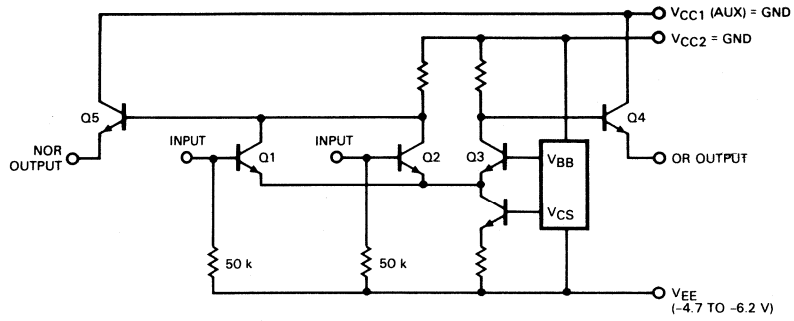


Fig. 3-2 Basic ECL Gate

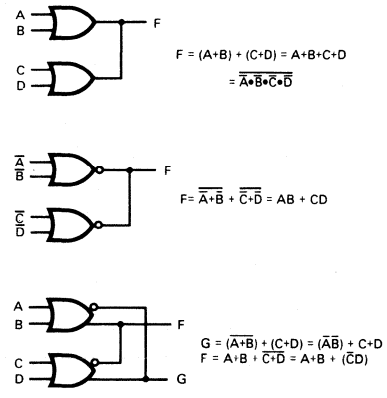


Fig. 3-3 OR/NOR Gates and the Wired-OR Connection

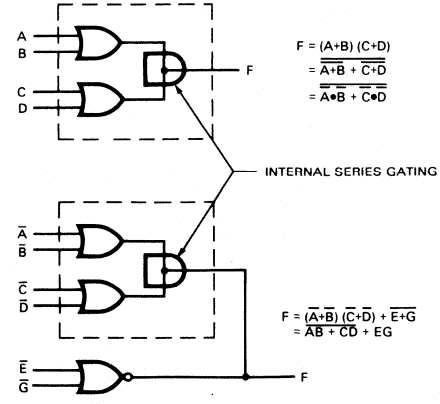


Fig. 3-4 OR/AND Gates and the Wired-OR

OR/AND, OR/AND/INVERT GATES

These gates utilize internal series AND gating to achieve a second gating level as described in Chapter 2. Note that this connection is internal to the device and cannot be modified by external connection *(Figure 3-4)*. The AND gating is obtained with minimum propagation delay and noise immunity penalty.

FLIP-FLOPS

ECL flip-flops are similar to conventional TTL flip-flops but there are fewer types available. *Figure 3-5* illustrates two workhorses — the 95029, a JK flip-flop with multiple $\overline{J}$, $\overline{K}$, and clock gating, and the F10131 dual D flip-flop containing two edge triggered master/slave flip-flops. Many gate functions are achieved internally without incurring a full gate delay. In the 95029, the $\overline{J}$ input is activated when all $\overline{J}$ inputs are LOW (or open); the $\overline{K}$ inputs operate in a similar manner. The three clock inputs allow data to be entered into the master when all clock inputs are LOW and loaded into the slave when any clock input goes HIGH.

The 10131 contains two master/slave, D flip-flops. The internal clock is the OR of two clock inputs, one common to both flip-flops. The OR clock permits the use of one input as a clock pulse and the other as an active LOW enable. While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times.

Each flip-flop has separate set and clear inputs which asynchronously determine the state of the output independent of the clock levels. Both have buffered outputs that can be wired-OR. Output voltage levels of a flip-flop are unpredictable if both set and clear signals are HIGH.

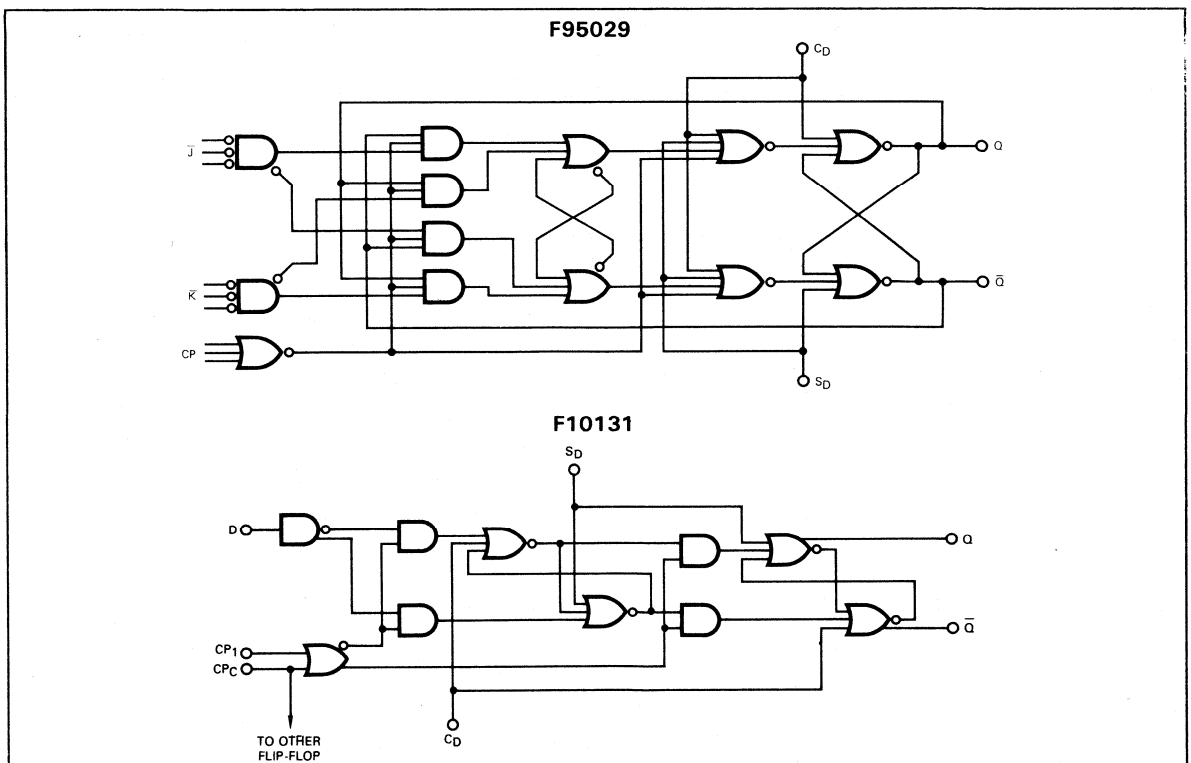


Fig. 3-5 Typical ECL Flip-Flops

When four D flip-flops with common clocks are required, the use of the 10000/95000 shift register, 10010/95010 decade counter or 10016/95016 binary counter should be considered. By holding the $\overline{PE}$ input LOW (or open), the circuits operate as four D flip-flops *(Figure 3-6)*.

MSI

ECL MSI logic is functionally similar to TTL. Designs are sometimes modified for an additional ground connection required for noise reasons and this means one less logic connection. Also, the active levels of the input and output are sometimes changed to optimize OR/NOR gate functions. The similarity of ECL flip-flops and MSI to TTL functions is illustrated in *Figure 3-7* (on the following page).

Counters

The 10010/95010 BCD decade counter and 10016/95016 4-bit binary counter provide the basis for most synchronous counter applications. They are similar in basic configuration and utilize synchronous parallel entry and asynchronous master reset. A Count Enable input and Terminal Count output provide for easy expansion to longer counters.

- Modulo n Counters — Synchronous parallel entry allows the 10016/95016 to divide by any modulo from 2 to 16 as shown in *Figure 3-8*. When the terminal count is reached, the parallel inputs are loaded synchronously. This in turn determines the number of clock pulses required before the $\overline{TC}$ output goes LOW again.

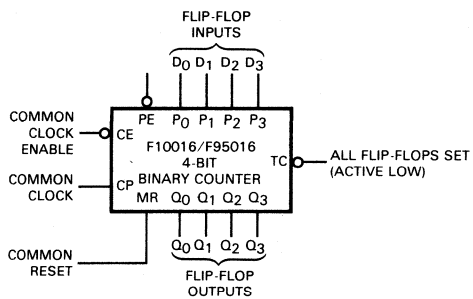
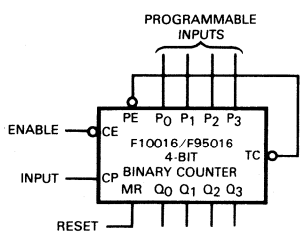


Fig. 3-6 10016/95016 used as Four D Flip Flops



DIVIDE RATIO	INPUT REQUIRED			
	P_0	P_1	P_2	P_3
2	L	H	H	H
3	H	L	H	H
4	L	L	H	H
5	H	H	L	H
6	L	H	L	H
7	H	L	L	H
8	L	L	L	H
9	H	H	H	L
10	L	H	H	L
11	H	L	H	L
12	L	L	H	L
13	H	H	L	L
14	L	H	L	L
15	H	L	L	L
16	L	L	L	L

Fig. 3-8 Programmable Divider

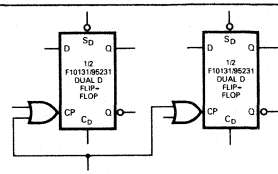
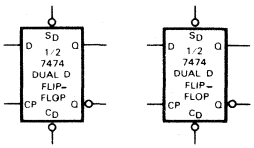
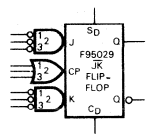
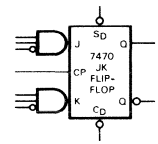
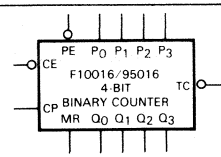
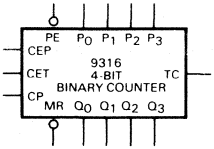
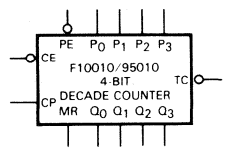
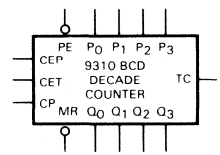
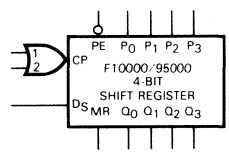
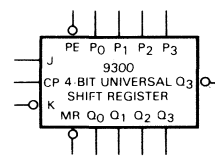
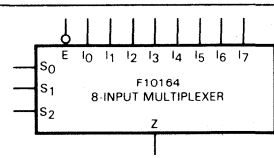
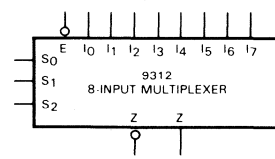
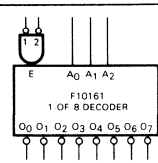
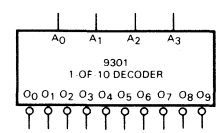
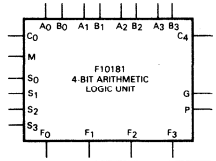
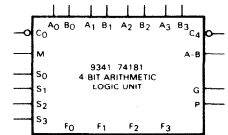
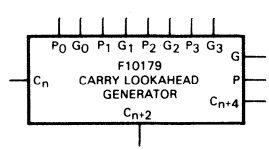
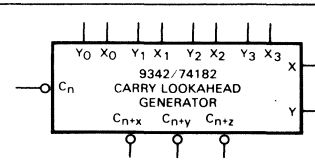
FUNCTION	ECL	TTL
Dual D Flip-Flop		
$\overline{JK}$ Flip-Flop		
4-Bit Binary Counter		
4-Bit Decade Counter		
4-Bit Shift Register		
8-Input Multiplexer		
1-of-8 Decoder		
4-Bit ALU		
Carry Lookahead Generator		

Fig. 3-7 ECL and TTL Function Similarity

- Expanding the Counters — The 10016/95016 can be expanded by adding flip-flops or more 10016/95016 stages. A divide-by-64 counter is shown in *Figure 3-9* utilizing a 10016 4-bit counter and 10131 dual D flip-flop. Two or more counters can be expanded synchronously as illustrated by the 4-decade counter in *Figure 3-10*. If the 10010 is replaced with 10016, the circuit becomes a 16-bit binary counter. An expanded modulo n counter (greater than four bits) can be implemented by using multiple 10016/95016 counters with OR gates driving all $\overline{CE}$ inputs. The gate inputs are the $\overline{TC}$ signals of all counters.

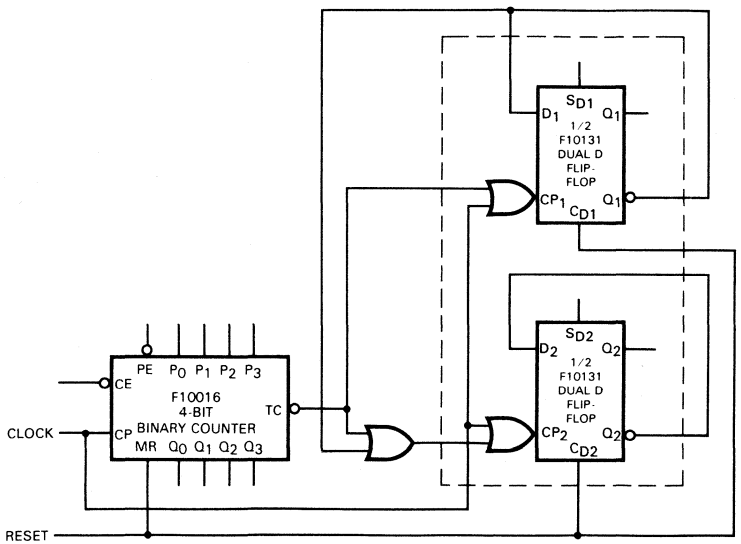


Fig. 3-9 Modulo 64 Counter

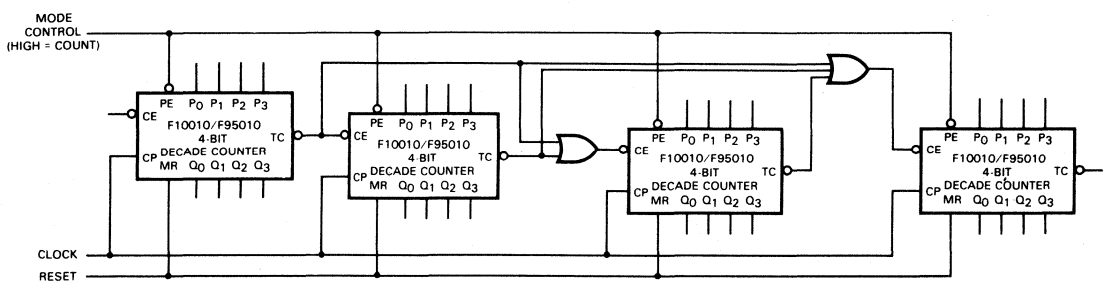


Fig. 3-10 4-Decade Synchronous Counter

- Quasi-Ripple Counters — To reduce gating and slightly increase operating frequency, the scheme of *Figure 3-11* can be used. The $\overline{TC}$ of one stage becomes the clock of another. Care must be taken that output skew does not introduce system hazards; parallel entry cannot be used.

- Modulo 10 Counter with 50% Duty Cycle—A special purpose decade counter with symmetric divide-by-10 output is shown in *Figure 3-12.* The diode resistor combination supplies a logic One; an unused gate can be used for the same purpose.

- Counter Shift Register — The synchronous parallel entry feature allows simple implementation of counters capable of shifting contents serially. The connection is shown in *Figure 3-13;* the $\overline{PE}$ becomes the shift/count (HIGH = count) mode control.

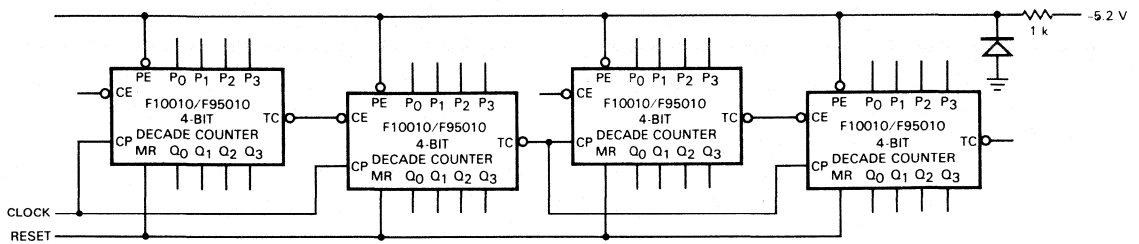
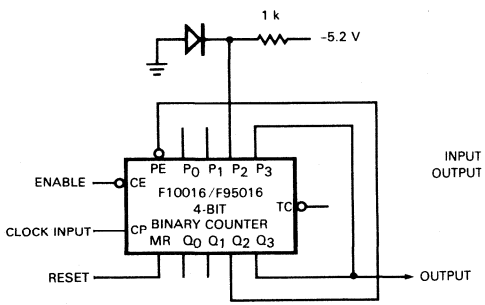
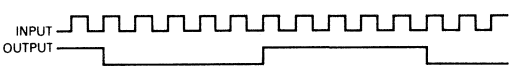


Fig. 3-11 Decade Counter with Ripple Between Decades 2 and 3





COUNT SEQUENCE

Q_0	Q_1	Q_2	Q_3
0	0	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	1

Fig. 3-12 Modulo 10 Counter with 50% Duty Cycle

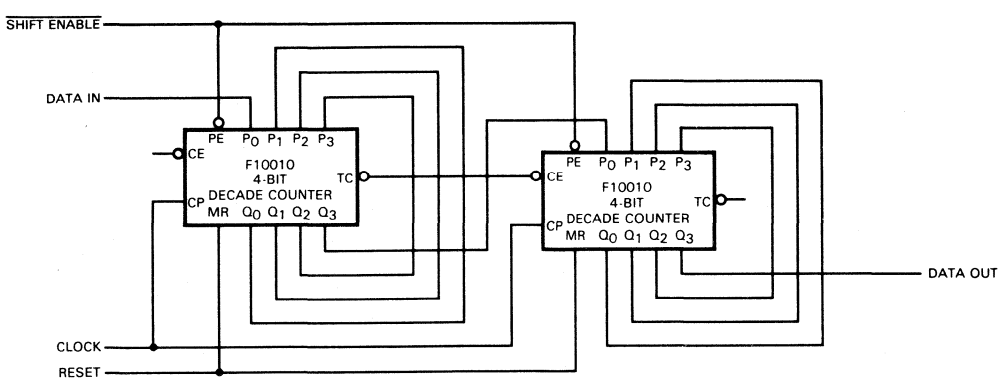


Fig. 3-13 Combination Counter/Serial Shift Register

Shift Registers

The 10000/95000 4-bit shift registers are ideal for most shift register applications.

- Parallel-To-Serial Converter with Control — The circuit of *Figure 3-14* accepts eight bits of parallel data, stores it and shifts it out serially. The addition of 1/2 of a dual flip-flop and 1/2 of a gate package supplies the control function. To analyze the operation, assume the parallel data has been loaded and is being shifted out. The output of the wired-OR (in effect a 7-input AND gate with active LOW inputs and outputs) is HIGH, introducing Ones into the 10131 flip-flop and Zeros into the 10000 shift registers. After seven pulses, the gate ouput goes LOW and loads new parallel data on the eighth clock, while setting the 10131 to Zero and introducing a timing bit. The entire operation can be controlled by an active LOW clock enable.

- Serial-To-Parallel Converter with Control — The same concept of combining control and data bits to simplify logic can be used for a serial-to-parallel converter. Two 10000/95000 shift registers are connected as 7-bit serial-to-parallel converter in *Figure 3-15*. To analyze the circuit, assume a Zero has appeared on the data ready line. On the next clock edge, data is entered into Q_0 and a Zero into Q_1 of the left register. All other positions are loaded with Ones. As more clock pulses occur, data is shifted in serially and the data ready line is HIGH until seven data bits are stored. At that point, the data ready line goes LOW, indicating parallel data is ready and the cycle repeats. The separate clock enable is active LOW. Note the use of a resistor and diode to obtain a non-saturating logic HIGH voltage level; this may also be obtained from the output of an unused gate.

- Shift Left/Shift Right Register — The 10000/95000 can be used as a shift left/shift right register by utilizing the parallel inputs to achieve the shift left mode. *Figure 3-16* shows a single 10000 connected in this mode; any length shift register can be obtained by adding more registers.

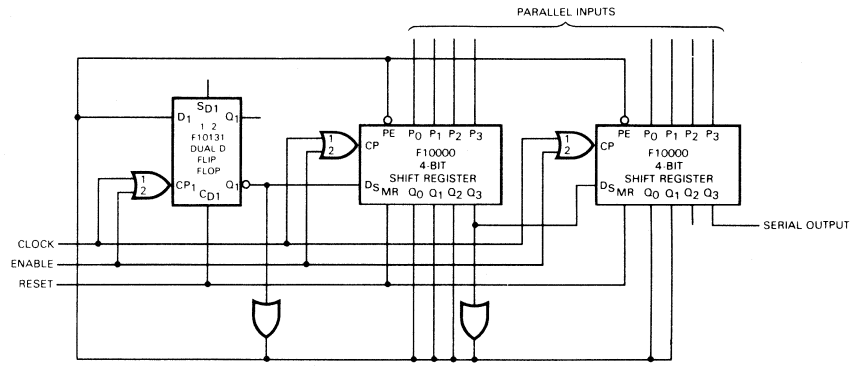


Fig. 3-14 8-Bit Parallel-to-Serial Converter with Control

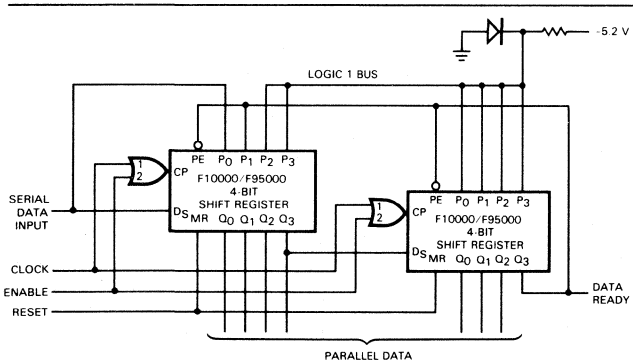


Fig. 3-15 7-Bit Serial-to-Parallel Converter

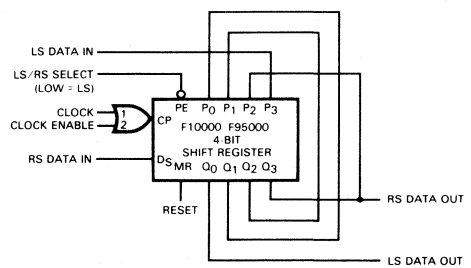


Fig. 3-16 Shift Left/Shift Right Register

- Shift Register with Two Inputs — If data is to be received and shifted into a register from one of two sources, the synchronous Parallel Enable can be used to save some gating. *Figure 3-17* shows the connection.

- Shift Register Counters — Shift registers are commonly used to implement a variety of high speed counters as shown in *Figure 3-18*. A ring counter has a single bit different than the rest of the bits and the output is returned to the input. To obtain a modulo n counter, n bits of shift register are used and no decoding is required. A Johnson counter employs feedback from the last stage back to the first such that the input is the opposite state of the output. A modulo n counter requires n/2 shift register stages; any state may be decoded with a 2-input gate. Feedback shift registers use a variety of logic gating to the first stage. An n-stage shift register provides a 2^n-1 modulo counter.

  All three shift counter methods require logic to insure against lock-up in unallowed states. More details on shift register counters may be found in the Fairchild TTL Applications Handbook.

Multiplexers

Multiplexers route one of several inputs to a single output. Multiplexer functions can be implemented with standard gates and the wired-OR connection. *Figure 3-19* illustrates a quad-2 input multiplexer implemented with NOR gates. Note that the gates can be physically located in different parts of the system, with lines Z_0 to Z_3 functioning as single-ended data busses, as long as wired-OR connection rules are met. The 10121 OR/AND gate can be used as a 4-input multiplexer as shown in *Figure 3-20.*

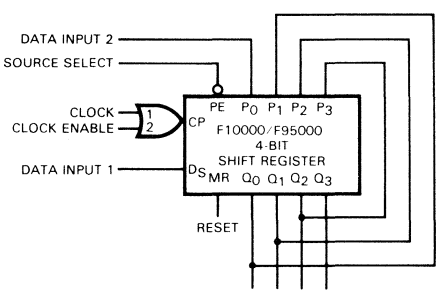


Fig. 3-17 Parallel Enable is used to Select One of Two Serial Inputs

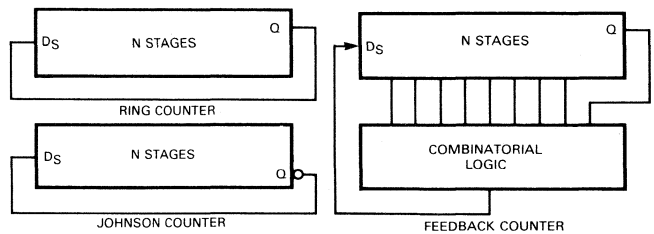


Fig. 3-18 Shift Registers used as Counters

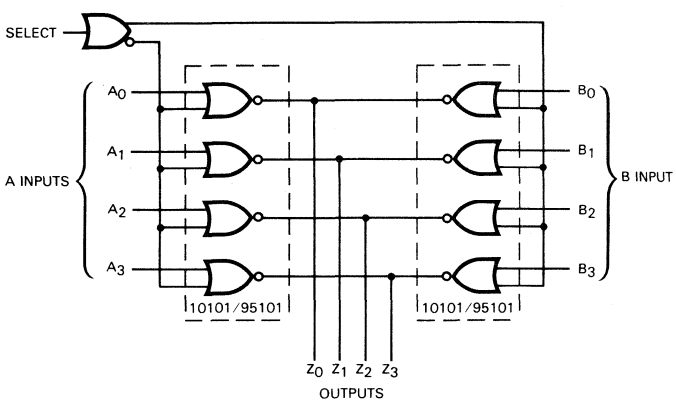


Fig. 3-19 Quad 2-Input Multiplexer using NOR Gates

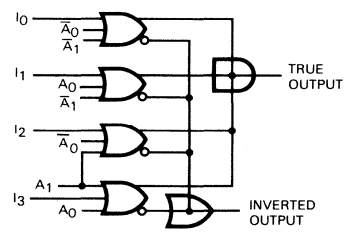


Fig. 3-20 4-Input Multiplexer using 10121

The 10164 is an 8-input multiplexer. The 10132 and 10174 are dual multiplexers. The 10173 is a quad 2-input multiplexer. They can be used for a variety of applications.

- Parallel-to-Serial Data Transmission — Two 10164 multiplexers are utilized to convert 16 channels of data to a single twisted pair transmission line *(Figure 3-21)*. If the 16 channels carry serial data at 5 MHz, the data is multiplexed and transmitted over a single line at an 80 MHz rate.

- Decade Demultiplexer—A decade demultiplexer controlled by a decade counter is shown in *Figure 3-22*. The Terminal Count output of the 10010 is used to simplify gating.

- Digital Function Generator — An 8-input multiplexer can be used to generate any function of four variables without additional logic. This concept is illustrated in *Figure 3-23* with a sample truth table and implementation for a desired 4-variable function F. Three of the variables are connected to the Select inputs while the fourth variable and its complement are connected to various Data inputs. In the example, A is connected to S_2, B to S_1 and C to S_0. Therefore, when A = B = C = 0, the I_0 input of the multiplexer is selected. The truth table indicates that this condition yields a Zero output when D is One or Zero; therefore, I_0 is designated a logic Zero, *i.e.*, open. When ABC = 001, I_1 is selected. From the truth table, the output is a One when D is logic Zero, and a Zero when D is logic One; therefore I_1 is connected to $\overline{D}$. Connections to the other inputs are determined in the same manner to complete the function. Note the use of a diode-resistor combination to obtain a HIGH logic One input. An unused gate can be used to achieve the same function.

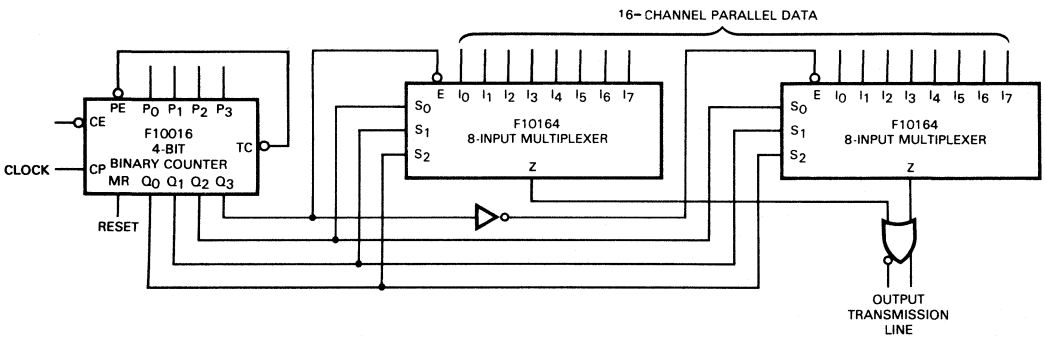


Fig. 3-21 16-Input Multiplexer

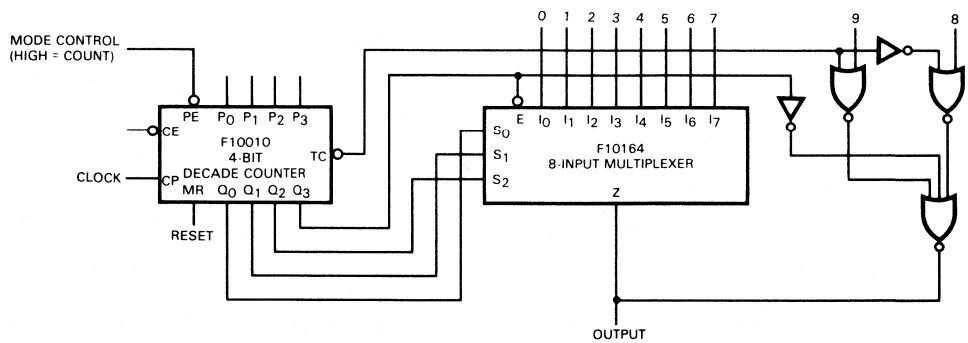
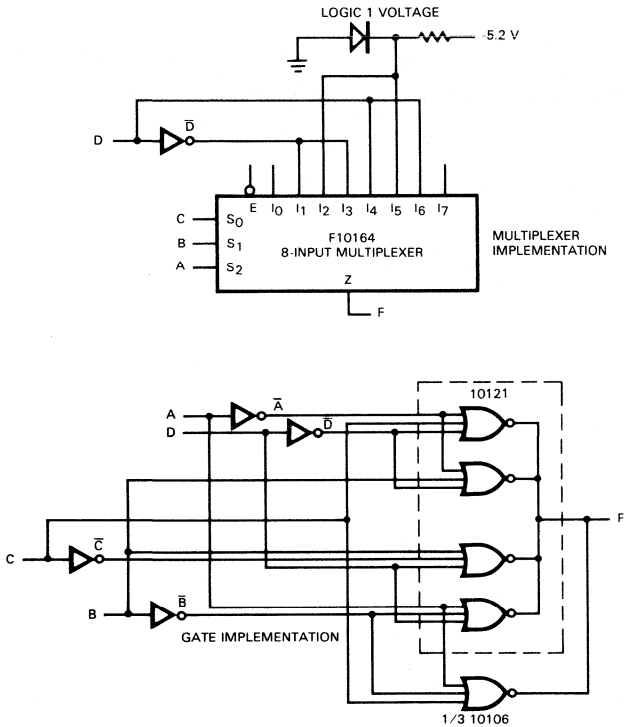


Fig. 3-22 Decade Counter and Demultiplexer

The function can also be implemented with 1 1/4 gate packages if both True and Complement inputs are available, or with 2 1/4 gate packages if only True inputs are available.

Decoders/Demultiplexers

For decoding or demultiplexing, the True and Complement outputs and the wired-OR feature of the basic gates can be used to make decoders with a single gate delay. For example, *Figure 3-24* is a 2 to 4-line, active LOW decoder. If added delay can be tolerated, the 2 to 4-line, active HIGH decoder of *Figure 3-25* can be used.



A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

DESIRED FUNCTION

$F = A\overline{C}D + A\overline{B}D + \overline{B}C\overline{D} + \overline{A}B\overline{D} + \overline{A}BC$

Fig. 3-23 Multiplexer Utilized as a Function Generator

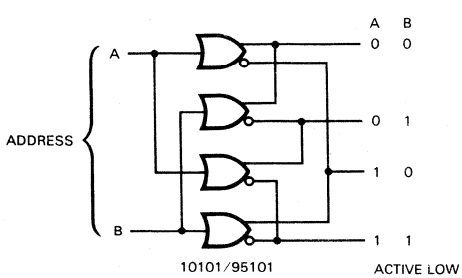


Fig. 3-24 2 to 4-Line Active Low Decoder

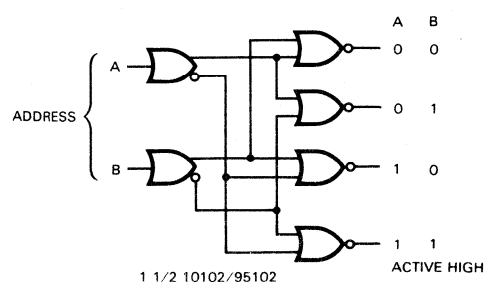
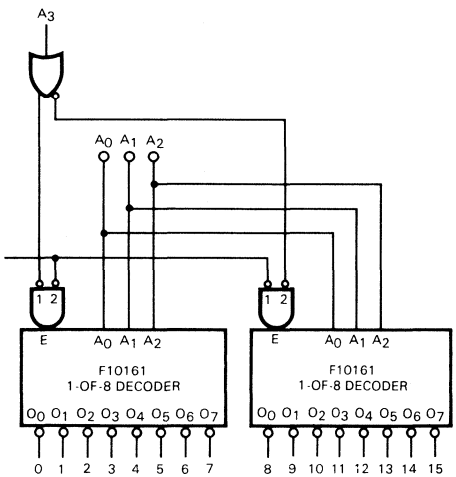


Fig. 3-25 2 to 4-Line Active High Decoder

The 10161 1-of-8 demultiplexer/decoder is designed to decode a 3-bit input word to one of eight active LOW outputs. Two Enable inputs force all outputs HIGH when either Enable input is HIGH. The 10162 1-of-8 demultiplexer/decoder is similar to the 10161 except that the selected output is HIGH; all others are LOW. The 10171 is a dual 1-of-4 demultiplexer/decoder with selected outputs LOW; the 10172 is similar with selected outputs HIGH. These demultiplexer/decoders can be used for a variety of applications.

- 4-Bit Code Decoding — The Enable inputs permit use of two 10161 or 10162 decoders to decode any 4-bit weighted or unweighted code by selecting the appropriate outputs in the required sequence. *Figure 3-26* shows the connection diagram and decode table for this application with active LOW outputs. The function is controlled by the other Enable input; propagation delay is typically 5 ns.

- Decade Decoder — While the universal 4-bit decoder method can be used for 1248 BCD, a more economical approach is shown in *Figure 3-27*. Note that no enable is provided for outputs 8 and 9.



OUTPUT SELECTION

DECIMAL DIGIT	BCD CODE				
	8421	5421	EXCESS 3	EXCESS 3 GRAY	2421
0	0	0	3	2	0
1	1	1	4	6	1
2	2	2	5	7	2
3	3	3	6	5	3
4	4	4	7	4	4
5	5	8	8	12	11
6	6	9	9	13	12
7	7	10	10	15	13
8	8	11	11	14	14
9	9	12	12	10	15

Fig. 3-26 Universal 4-Bit Decoder

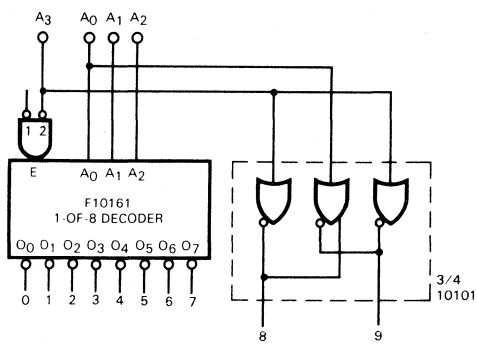


Fig. 3-27 1248 BCD Decade Decoder

- Memory Decoding — A major decoder application is in address decoding of high speed memory systems. The Enable inputs allow the use of several decoders to decode words of greater than four bits as illustrated in *Figure 3-28*. Four packages are used to select one of 32 active HIGH outputs in 6 to 9 ns from the time of application of the address at inputs A_0 through A_4. This technique can be extended to a 6-bit address by using the LOW output of the 10161 to select one decoder from a group decoders. *Figure 3-29* shows a 1-of-64 decoding scheme with typical propagation delays of 8 to 12 ns.

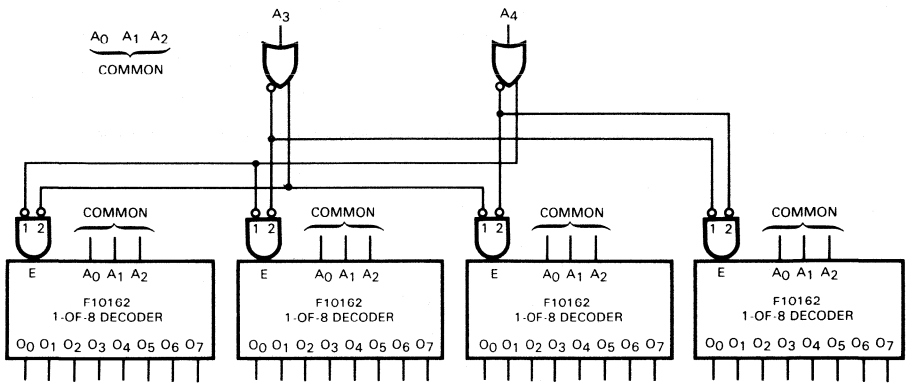


Fig. 3-28 1-of-32 Active HIGH Decoder

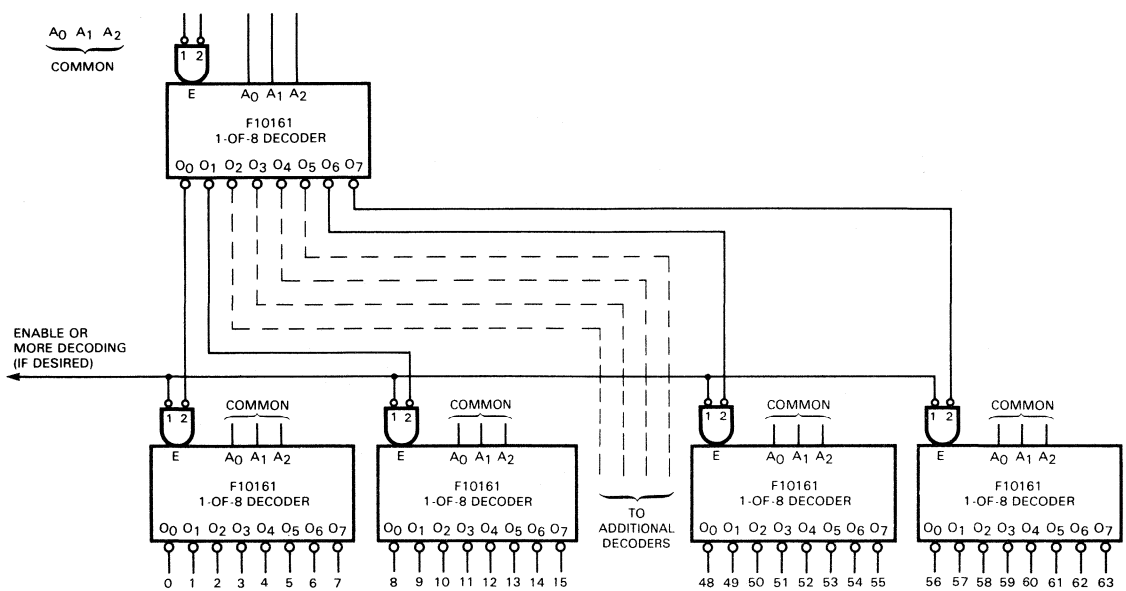


Fig. 3-29 1-of-64 Active LOW Decoder

The remaining Enable input can be used for overall control or wider decoding if desired. 1-of-8 decoders, *e.g.,* the 10161, can be used to demultiplex serial data to parallel outputs by connecting the serial data source to an Enable input *(Figure 3-30)*. The other Enable input functions as a data enable line, while inputs A_0, A_1 and A_2 determine which of the eight output lines receives the data. The data is not inverted through the demultiplexer since both the input and outputs are active LOW.

Comparators

A variety of high speed comparators can be defined using ECL gating structures. *Figure 3-31* illustrates a 4-bit identity comparatory utilizing two 10121 OR/AND gates.

A 6-bit identity comparator utilizing two 10107 Exclusive OR/NOR gates is shown in *Figure 3-32.* Only True inputs are required and equality is indicated by a LOW on the comparator output.

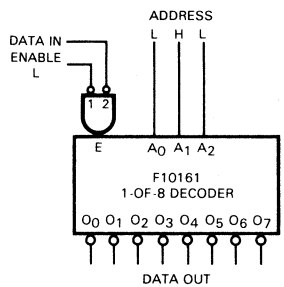


Fig. 3-30 8-Output Demultiplexer

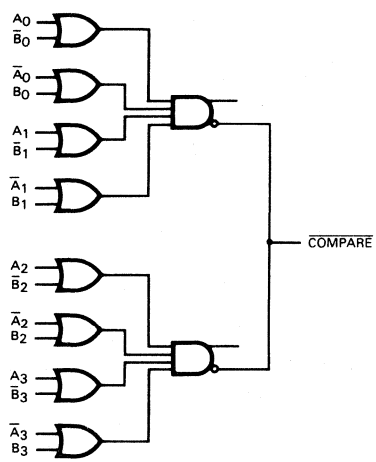


Fig. 3-31 4-Bit Identity Comparator Using Two 10121 OR/AND Devices

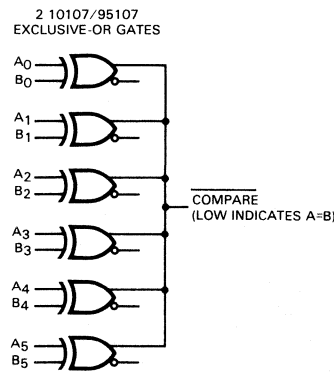


Fig. 3-32 6-Bit Identity Comparator Requiring True Inputs Only

Parity Generation and Checking

The 10160 typically provides 12-bit parity generation in 3 ns. Its output is HIGH if an odd number of inputs are HIGH. Figure 3-33 illustrates a 48-bit parity circuit using four 10160s and a 10107 Exclusive-OR gate; typical total delay is 7 ns.

CONVERTING A TTL DESIGN TO ECL

Conversion of TTL design to ECL is straightforward. The NAND gate is the most common TTL logic element, with NOR, OR, and AND gates also available. Clearly, OR and NOR functions are readily available with ECL. The NAND and AND functions are obtained from the ECL OR/NOR function by complementing the inputs as shown in *Figure 3-34a.* NAND gates of five or more inputs are formed by complementing the inputs to ECL OR gates and OR wiring *(Figure 3-34b).* The AND/OR function is obtained in ECL by using wired-OR NORs *(Figure 3-34c)*, the AND/OR/INVERT by using ECL OR/AND gates *(Figure 3-34d).*

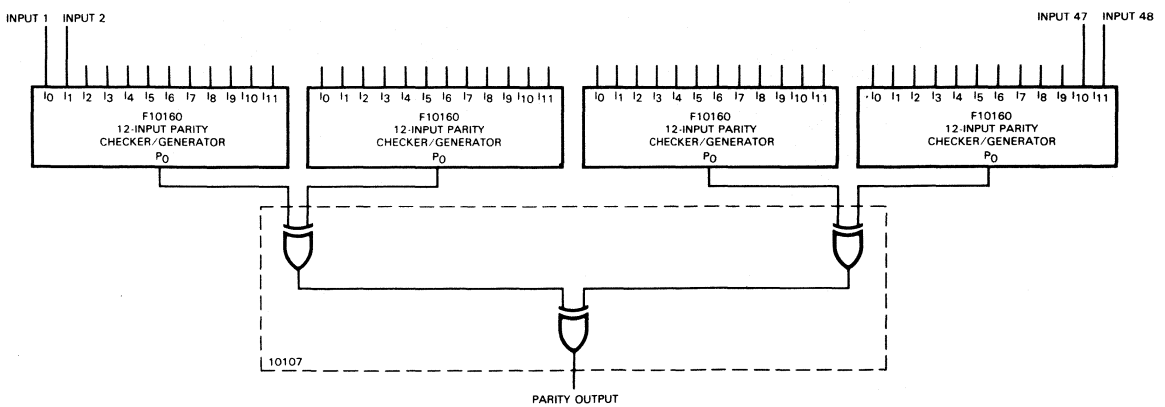
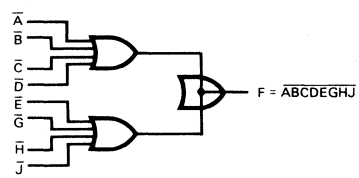


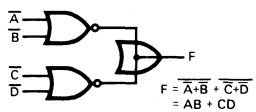
Fig. 3-33 48-Bit Parity Checker/Generator with Typical Delay of 10 ns



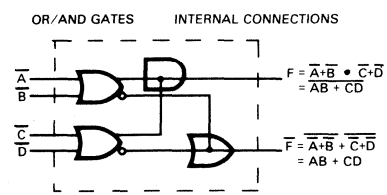
a. NAND Function Obtained by Complementing Inputs



b. Wide NAND Gates Obtained by Using Complemented Inputs and Wired-OR



c. NOR Gates Perform AND/OR Function

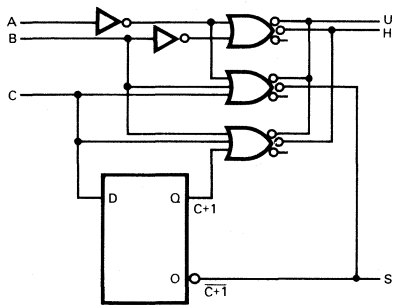


d. OR/AND Gates Perform AND/OR/INVERT Function

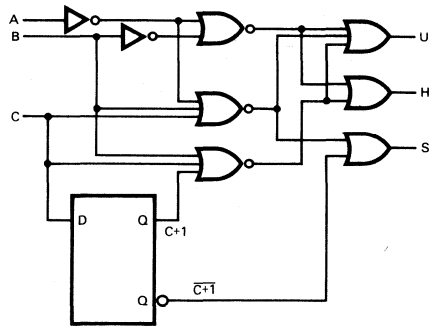
Fig. 3-34 Common ECL Logic Functions

From these examples, a simple rule can be determined. To convert from TTL to ECL, complement the ECL gate inputs and use True ECL outputs. However, this approach does not necessarily yield optimum designs because it does not take advantage of the ECL wired-OR capability.

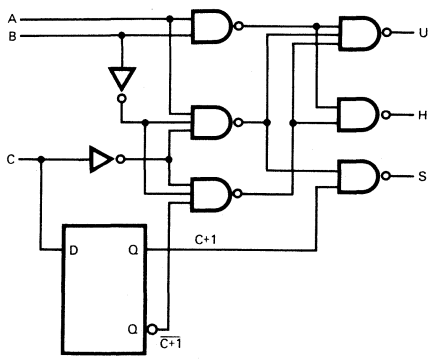
Figure 3-35 illustrates the conversion methods. In *Figure 3-35a*, a TTL circuit converted to ECL requires about 2-1/2 packages assuming no cost for unused functions. In other words, the cost of the D flip-flop is counted as half a package. A brute force conversion to ECL gates was used to generate the circuit of *Figure 3-35b*, cost went up to about three packages. When the wired-OR connection *(Figure 3-35c)* was utilized, the package count dropped back to 2 1/2 and a level of gate delay was eliminated. Sometimes, wiring constraints may limit the usefulness of the wired-OR connection; check wiring rules given in *Chapter 5*.



a. Original TTL Function, About 2-1/2 Packages

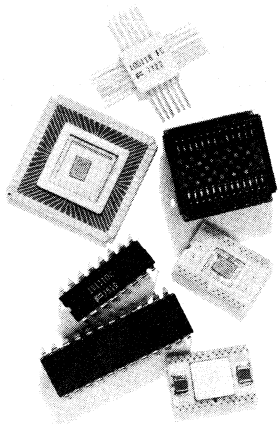


b. Brute Force Conversion to ECL, About 3 Packages



c. Conversion to ECL using Wired-OR, About 2-1/2 Packages

Fig. 3-35 Examples of Conversion of TTL to ECL



INTRODUCTION

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ECL CIRCUIT BASICS 2

ECL LOGIC DESIGN 3

TRANSMISSION LINE CONCEPTS 4

ECL INTERCONNECTIONS 5

POWER DISTRIBUTION AND THERMAL CONSIDERATIONS 6

F10K SERIES DATA SHEETS 7

F95K SERIES DATA SHEETS 8

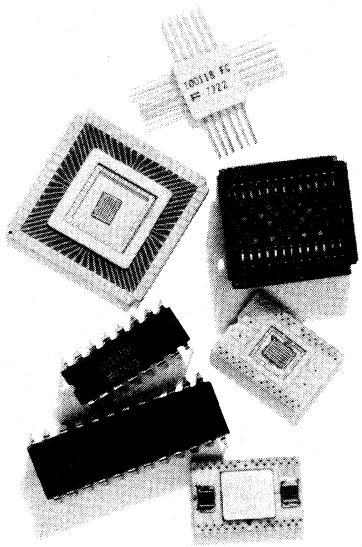
11C SERIES DATA SHEETS 9

F100K SERIES DATA SHEETS 10

ECL MEMORY DATA SHEETS 11

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CHAPTER 4

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- Simplifying Assumptions
- Characteristic Impedance
- Propagation Velocity
- Termination and Reflection
- Source Impedance, Multiple Reflections
- Lattice Diagram
- Shorted Line
- Series Termination
- Extra Delay with Termination Capacitance
- Distributed Loading Effects on Line Characteristics
- Mismatched Lines
- Rise Time Versus Line Delay
- Ringing
- Summary
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Chapter 4
TRANSMISSION LINE CONCEPTS

INTRODUCTION

The interactions between wiring and circuitry in high speed systems are more easily determined by treating the interconnections as transmission lines. A brief review of basic concepts is presented and simplified methods of analysis are used to examine situations commonly encountered in digital systems. Since the principles and methods apply to any type of logic circuits, normalized pulse amplitudes are used in sample waveforms and calculations.

SIMPLIFYING ASSUMPTIONS

For the great majority of interconnections in digital systems, the resistance of the conductors is much less than the input and output resistance of the circuits. Similarly, the insulating materials have very good dielectric properties. These circumstances allow such factors as attenuation, phase distortion, and bandwidth limitations to be ignored. With these simplifications, interconnections can be dealt with in terms of characteristic impedance and propagation delay.

CHARACTERISTIC IMPEDANCE

The two conductors that interconnect a pair of circuits have distributed series inductance and distributed capacitance between them, and thus constitute a transmission line. For any length in which these distributed parameters are constant, the pair of conductors have a characteristic impedance Z_0. Whereas quiescent conditions on the line are determined by the circuits and terminations, Z_0 is the ratio of transient voltage to transient current passing by a point on the line when a signal change or other electrical disturbance occurs. The relationship between transient voltage, transient current, characteristic impedance, and the distributed parameters is expressed as follows.

$$\frac{V}{I} = Z_0 = \sqrt{\frac{L_0}{C_0}} \tag{4-1}$$

where L_0 = inductance per unit length, C_0 = capacitance per unit length. Z_0 is in ohms, L_0 in henries, C_0 in farads.

PROPAGATION VELOCITY

Propagation velocity v and its reciprocal, delay per unit length δ, can also be expressed in terms of L_0 and C_0. A consistent set of units is nanoseconds, microhenries and picofarads, all having the same unit of length.

$$v = \frac{1}{\sqrt{L_0 C_0}} \qquad \delta = \sqrt{L_0 C_0} \tag{4-2}$$

Equations 4-1 and *4-2* provide a convenient means of determining the L_0 and C_0 of a line when delay, length and impedance are known. For a length l and delay T, δ is the ratio T/l. To determine L_0 and C_0, combine *Equations 4-1* and *4-2*.

$$L_0 = \delta Z_0 \tag{4-3}$$

$$C_0 = \frac{\delta}{Z_0} \tag{4-4}$$

More formal treatments of transmission line characteristics, including loss effects, are available from many sources.[1-3]

TERMINATION AND REFLECTION

A transmission line with a terminating resistor is shown in *Figure 4-1*. As indicated, a positive step function voltage travels from left to right. To keep track of reflection polarities, it is convenient to consider the lower conductor as the voltage reference and to think in terms of current flow in the top conductor only. The generator is assumed to have zero internal impedance. The initial current I_1 is determined by V_1 and Z_0.

If the terminating resistor matches the line impedance, the ratio of voltage to current traveling along the line is matched by the ratio of voltage to current which must, by Ohm's law, always prevail at R_T. From the viewpoint of the voltage step generator, no adjustment of output current is ever required; the situation is as though the transmission line never existed and R_T had been connected directly across the terminals of the generator. From the R_T viewpoint, the only thing the line did was delay the arrival of the voltage step by the amount of time T.

When R_T is not equal to Z_0, the initial current starting down the line is still determined by V_1 and Z_0 but the final steady state current, after all reflections have died out, is determined by V_1 and R_T (ohmic resistance of the line is assumed to be negligible). The ratio of voltage to current in the initial wave is not equal to the ratio of voltage to current demanded by R_T. Therefore, at the instant the initial wave arrives at R_T, another voltage and current wave must be generated so that Ohm's law is satisfied at the line-load interface. This *reflected* wave, indicated, by V_r and I_r in *Figure 4-1*, starts to return toward the generator. Applying Kirchoff's laws to the end of the line at the instant the initial wave arrives, results in the following.

$$I_1 + I_r = I_T = \text{current into } R_T \tag{4-5}$$

Since only one voltage can exist at the end of the line at this instant of time, the following is true.

$$V_1 + V_r = V_T$$

$$\text{thus} \qquad I_T = \frac{V_T}{R_T} = \frac{V_1 + V_r}{R_T} \tag{4-6}$$

$$\text{also} \qquad I_1 = \frac{V_1}{Z_0} \text{ and } I_r = -\frac{V_r}{Z_0}$$

with the minus sign indicating that V_r is moving toward the generator.

Combining the foregoing relationships algebraically and solving for V_r yields a simplified expression in terms of V_1, Z_0 and R_T.

$$\frac{V_1}{Z_0} - \frac{V_r}{Z_0} = \frac{V_1 + V_r}{R_T} = \frac{V_1}{R_T} + \frac{V_r}{R_T}$$

$$V_1 \left(\frac{1}{Z_0} - \frac{1}{R_T}\right) = V_r \left(\frac{1}{R_T} + \frac{1}{Z_0}\right) \tag{4-7}$$

$$V_r = V_1 \left(\frac{R_T - Z_0}{R_T + Z_0}\right) = \rho_L V_1$$

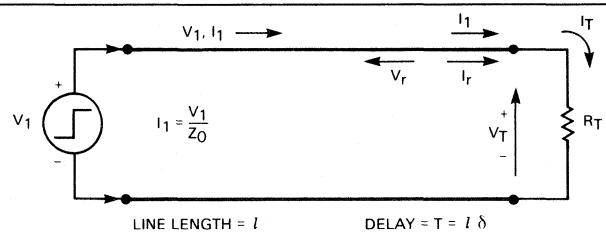


Fig. 4-1 Assigned Polarities and Directions for Determining Reflections

The term in parenthesis is called the coefficient of reflection ρ. With R_T ranging between zero (shorted line) and infinity (open line), the coefficient ranges between −1 and +1 respectively. The subscript L indicates that ρ refers to the coefficient at the load end of the line.

Equation 4-7 expresses the amount of voltage sent back down the line, and since

$$V_T = V_I + V_r$$

$$\text{then} \qquad V_T = V_I\,(1 + \rho_L) \tag{4-8}$$

V_T can also be determined from an expression which does not require the preliminary step of calculating ρ_L. Manipulating $(1 + \rho_L)$ results in

$$1 + \rho_L = 1 + \frac{R_T - Z_0}{R_T + Z_0} = 2\left(\frac{R_T}{R_T + Z_0}\right)$$

Substituting in *Equation 4-8* gives

$$V_T = 2\left(\frac{R_T}{R_T + Z_0}\right) V_1 \tag{4-9}$$

The foregoing has the same form as a simple voltage divider involving a generator V_1 with internal impedance Z_0 driving a load R_T, except that the amplitude of V_T is doubled.

The arrow indicating the direction of V_r in *Figure 4-1*, correctly indicates the V_r direction of travel, but the direction of I_r flow depends on the V_r polarity. If V_r is positive, I_r flows toward the generator, opposing I_1. This relationship between the polarity of V_r and the direction of I_r can be deduced by noting in *Equation 4-7* that if V_r is positive it is because R_T is greater than Z_0. In turn, this means that the initial current I_r is larger than the final quiescent current, dictated by V_1 and R_T. Hence I_r must oppose I_1 to reduce the line current to the final quiescent value. Similar reasoning shows that if V_r is negative, I_r flows in the same direction as I_1.

It is sometimes easier to determine the effect of V_r on line conditions by thinking of it as an independent voltage generator in series with R_T. With this concept, the direction of I_r is immediately apparent; its magnitude, however, is the ratio of V_r to Z_0, *i.e.*, R_T is already accounted for in the magnitude of V_r. The relationships between incident and reflected signals are represented in *Figure 4-2* for both cases of mismatch between R_T and Z_0.

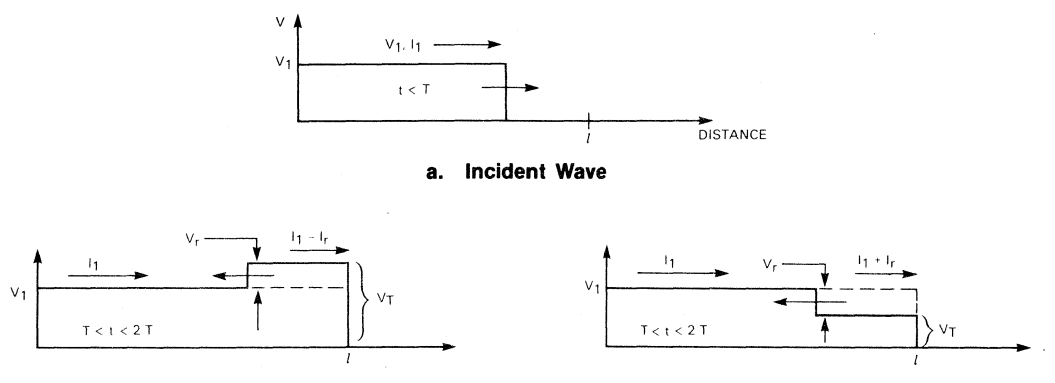


Fig. 4-2 Reflections for $R_T \neq Z_0$

The incident wave is shown in *Figure 4-2a*, before it has reached the end of the line. In *Figure 4-2b*, a positive V_r is returning to the generator. To the left of V_r the current is still I_1, flowing to the right, while to the right of V_r the net current in the line is the difference between I_1 and I_r. In *Figure 4-2c*, the reflection coefficient is negative, producing a negative V_r. This, in turn, causes an increase in the amount of current flowing to the right behind the V_r wave.

SOURCE IMPEDANCE, MULTIPLE REFLECTIONS

When a reflected voltage arrives back at the source (generator), the reflection coefficient at the source determines the response to V_r. The coefficient of reflection at the source is governed by Z_0 and the source resistance R_S.

$$\rho_S = \frac{R_S - Z_0}{R_S + Z_0} \tag{4-10}$$

If the source impedance matches the line impedance, a reflected voltage arriving at the source is not reflected back toward the load end. Voltage and current on the line are stable with the following values.

$$V_T = V_1 + V_r \text{ and } I_T = I_1 - I_r \tag{4-11}$$

If neither source impedance nor terminating impedance matches Z_0, multiple reflections occur; the voltage at each end of the line comes closer to the final steady state value with each succeeding reflection. An example of a line mismatched on both ends is shown in *Figure 4-3*. The source is a step function of 1 V amplitude occurring at time t_0. The initial value of V_1 starting down the line is 0.75 V due to the voltage divider action of Z_0 and R_S. The time scale in the photograph shows that the line delay is approximately 6 ns. Since neither end of the line is terminated in its characteristic impedance, multiple reflections occur.

The amplitude and persistence of the ringing shown in *Figure 4-3* becomes greater with increasing mismatch between the line impedance and source and load impedances. Reducing R_S *(Figure 4-3)* to 13 Ω increases ρ_S to −0.75, and the effects are illustrated in *Figure 4-4*. The initial value of V_T is 1.8 V with a reflection of 0.9 V from the open end. When this reflection reaches the source, a reflection of 0.9 × −0.75 V

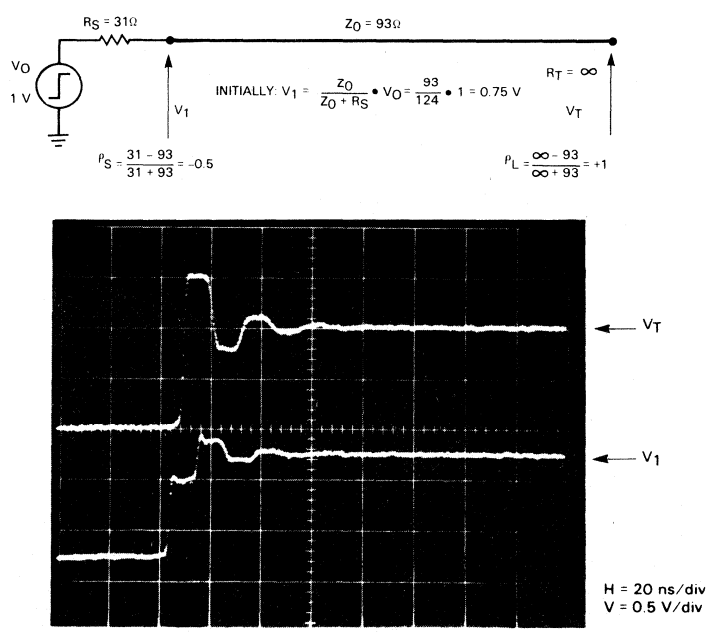


Fig. 4-3 Multiple Reflections Due to Mismatch at Load and Source

starts back toward the open end. Thus, the second increment of voltage arriving at the open end is negative going. In turn, a negative-going reflection of 0.9 × −0.75 V starts back toward the source. This negative increment is again multiplied by −0.75 at the source and returned toward the open end. It can be deduced that the difference in amplitude between the first two positive peaks observed at the open end is

$$V_T - V_T' = (1 + \rho_L)\, V_1 - (1 + \rho_L)\, V_1\, \rho_L^2\, \rho_S^2$$
$$= (1 + \rho_L)\, V_1\, (1 - \rho_L^2\, \rho_S^2) \qquad (4\text{-}12)$$

The factor $(1 - \rho_L^2\, \rho_S^2)$ is similar to the damping factor associated with lumped constant circuitry. It expresses the attenuation of successive positive or negative peaks of ringing.

LATTICE DIAGRAM

In the presence of multiple reflections, keeping track of the incremental waves on the line and the net voltage at the ends becomes a bookkeeping chore. A convenient and systematic method of indicating line conditions which combines magnitude, polarity and time utilizes a graphic construction called a lattice diagram.[4] A lattice diagram for the line conditions of *Figure 4-3* is shown in *Figure 4-5.*

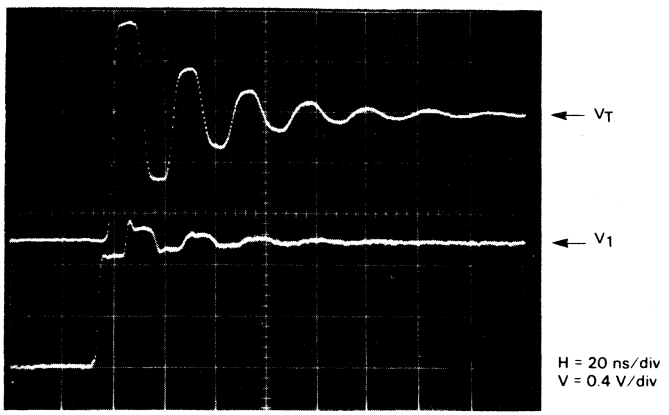


Fig. 4-4 Extended Ringing when R_S of Figure 4-3 is Reduced to 13 Ω

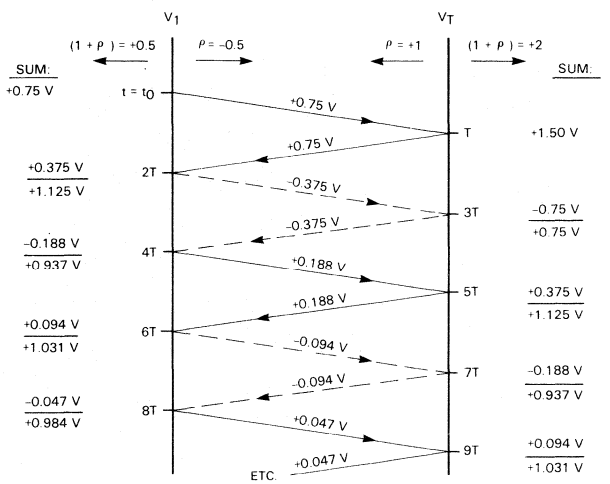


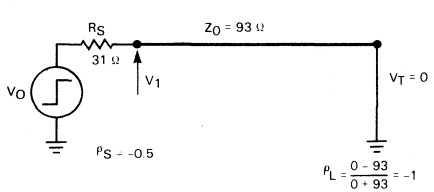
Fig. 4-5 Lattice Diagram for the Circuit of Figure 4-3

The vertical lines symbolize the discontinuity points, in this case the ends of the line. A time scale is marked off on each line in increments of 2T, starting at t_0 for V_1 and T for V_T. The diagonal lines indicate the incremental voltages traveling between the ends of the line; solid lines are used for positive voltages and dashed lines for negative. It is helpful to write the reflection and transmission multipliers ρ and $(1 + \rho)$ at each vertical line, and to tabulate the incremental and net voltages in columns alongside the vertical lines. Both the lattice diagram and the waveform photograph show that V_1 and V_T asymptotically approach 1 V, as they must with a 1 V source driving an open-ended line.

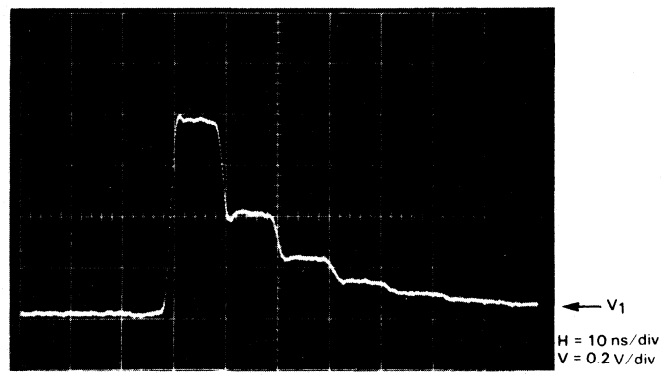
SHORTED LINE

The open-ended line in *Figure 4-3* has a reflection coefficient of +1 and the successive reflections tend toward the steady state conditions of zero line current and a line voltage equal to the source voltage. In contrast, a shorted line has a reflection coefficient of −1 and successive reflections must cause the line conditions to approach the steady state conditions of zero voltage and a line current determined by the source voltage and resistance.

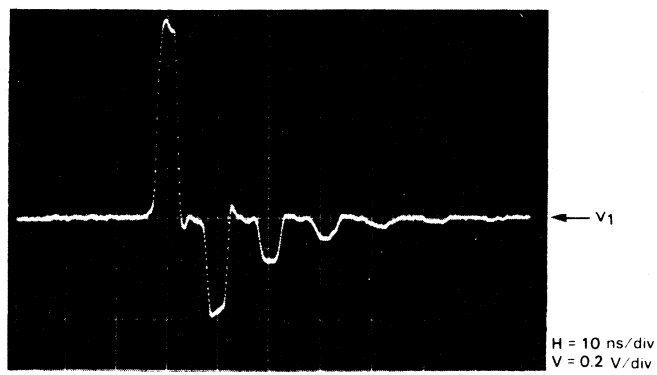
Shorted line conditions are shown in *Figure 4-6a* with the reflection coefficient at the source end of the line also negative. A negative coefficient at both ends of the line means that any voltage approaching either end of the line is reflected in the opposite polarity. *Figure 4-6b* shows the response to an input step-function with a duration much longer than the line delay. The initial voltage starting down the line is



a. Reflection Coefficients for Shorted Line



b. Input Pulse Duration ≫ Line Delay



c. Input Pulse Duration < Line Delay

Fig. 4-6 Reflections of Long and Short Pulses on a Shorted Line

about +0.75 V, which is inverted at the shorted end and returned toward the source as −0.75 V. Arriving back at the source end of the line, this voltage is multiplied by $(1 + \rho_S)$, causing a −0.37 V net change in V_1. Concurrently, a reflected voltage of +0.37 V (−0.75 V times ρ_S of −0.5) starts back toward the shorted end of the line. The voltage at V_1 is reduced by 50% with each successive round trip of reflections, thus leading to the final condition of zero volts on the line.

When the duration of the input pulse is less than the delay of the line, the reflections observed at the source end of the line constitute a train of negative pulses, as shown in *Figure 4-6c*. The amplitude decreases by 50% with each successive occurrence as it also did in *Figure 4-6b*.

SERIES TERMINATION

Driving an open-ended line through a source resistance equal to the line impedance is called series termination. It is particularly useful when transmitting signals which originate on a PC board and travel through the backplane to another board, with the attendant discontinuities, since reflections coming back to the source are absorbed and ringing thereby controlled. *Figure 4-7* shows a 93 Ω line driven from a 1 V generator through a source impedance of 93 Ω. The photograph illustrates that the amplitude of the initial signal sent down the line is only half of the generator voltage, while the voltage at the open end of the line is doubled to full amplitude $(1 + \rho_L = 2)$. The reflected voltage arriving back at the source raises V_1 to the full amplitude of the generator signal. Since the reflection coefficient at the source is zero, no further changes occur and the line voltage is equal to the generator voltage. Because the initial signal on the line is only half the normal signal swing, the loads must be connected at or near the end of the line to avoid receiving a 2-step input signal.

An ECL output driving a series terminated line requires a pull down resistor to V_{EE}, as indicated in *Figure 4-8*. The resistor R_0 shown in *Figure 4-8* symbolizes the output resistance of the ECL gate. The relationships between R_0, R_S, R_E and Z_0 are discussed in Chapter 5.

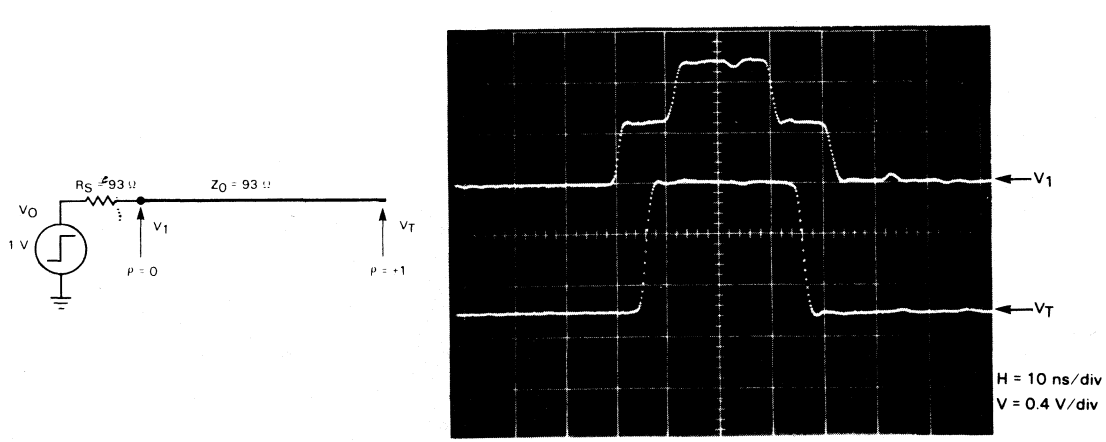


Fig. 4-7 Series Terminated Line and Waveforms

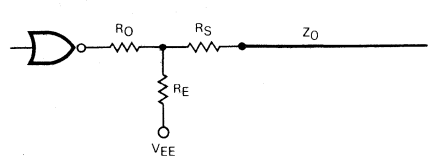


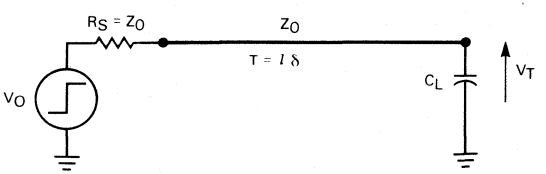
Fig. 4-8 ECL Element Driving a Series Terminated Line

EXTRA DELAY WITH TERMINATION CAPACITANCE

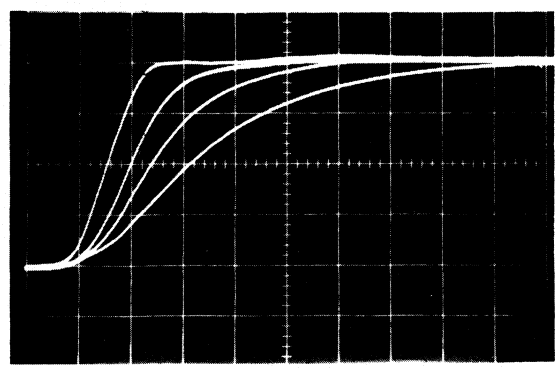
Designers should consider the effect of the load capacitance at the end of the line when using series termination. *Figure 4-9* shows how the output waveform changes with increasing load capacitance. *Figure 4-9b* shows the effect of load capacitances of 0, 12, 24, 48 pF. With no load, the delay between the 50% points of the input and output is just the line delay T. A capacitive load at the end of the line causes an extra delay Δ T due to the increase in rise time of the output signal. The midpoint of the output is used as a criterion because the propagation delay of an ECL circuit is measured between the 50% points of the input and output signals.

The increase in propagation delay can be calculated by using a ramp approximation for the incident voltage and characterizing the circuit as a fixed impedance in series with the load capacitance, as shown in *Figure 4-10*. One general solution serves both series and parallel termination cases by using an impedance Z′ and a time constant τ, defined in *Figure 4-10a* and *4-10b*. Calculated and observed increases in delay time to the 50% point show close agreement when τ is less than half the ramp time. At large ratios of τ/a (where a = ramp time), measured delays exceed calculated values by approximately 7%. *Figure 4-11*, based on measured values, shows the increase in delay to the 50% point as a function of the Z′C time constant, both normalized to the 10% to 90% rise time of the input signal. As an example of using the graph, consider a 100 Ω series terminated line with 30 pF load capacitance at the end of the line and a no-load rise time of 3 ns for the input signal. From *Figure 4-10a*, Z′ is equal to 100 Ω; the ratio Z′C/t_r is 1. From the graph, the ratio Δ T/t_r is 0.8. Thus the increase in the delay to the 50% point of the output waveform is 0.8 t_r, or 2.4 ns, which is then added to the no-load line delay T to determine the total delay.

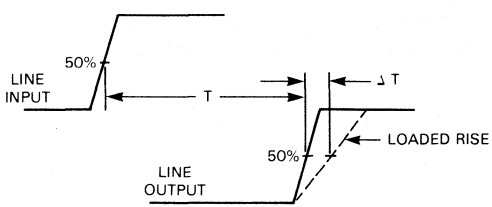
Had the 100 Ω line in the foregoing example been parallel rather than series terminated at the end of the line, Z′ would be 50 Ω. The added delay would be only 1.35 ns with the same 30 pF loading at the end. The added delay would be only 0.75 ns if the line were 50 Ω and parallel terminated. The various trade-offs involving type of termination, line impedance, and loading are important considerations for critical delay paths.



a. Series Terminated Line with Load Capacitance

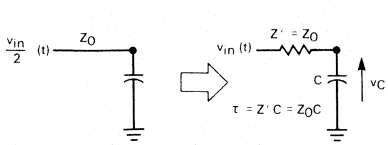


b. Output Rise Time Increase with Increasing Load Capacitance

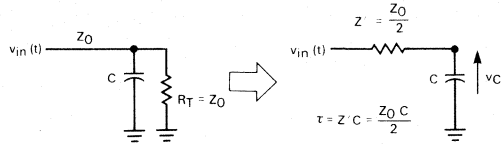


c. Extra Delay Δ T Due to Rise Time Increase

Fig. 4-9 Extra Delay with Termination Capacitance

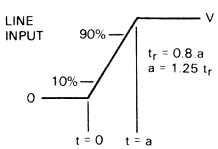


a. Thevenin Equivalent for Series Terminated Case



b. Thevenin Equivalent for Parallel Terminated Case

$$v_{in}(t) = \frac{V}{a}\,[tu(t) - (t-a)u(t-a)]$$



$$u(t) = \begin{array}{l} 0 \text{ for } t < o \\ 1 \text{ for } t > o \end{array}$$

$$u(t-a) = \begin{array}{l} 0 \text{ for } t < a, \\ 1 \text{ for } t > a \end{array}$$

$$V_{IN}(S) = \frac{V}{as^2}\,(1 - e^{-as})$$

$$V_C(S) = \frac{V}{a\tau} \cdot \frac{1}{s^2\,(s + 1/\tau)}\,(1 - e^{-as})$$

$$v_c(t) = \frac{V}{a}\,[t - \tau(1 - e^{-t/\tau})]\,u(t) - \frac{V}{a}\,[(t-a) - \tau(1 - e^{-\frac{t-a}{\tau}})]\,u(t-a)$$

c. Equations for Input and Output Voltages

Fig. 4-10 Determining the Effect of End-of-line Capacitance

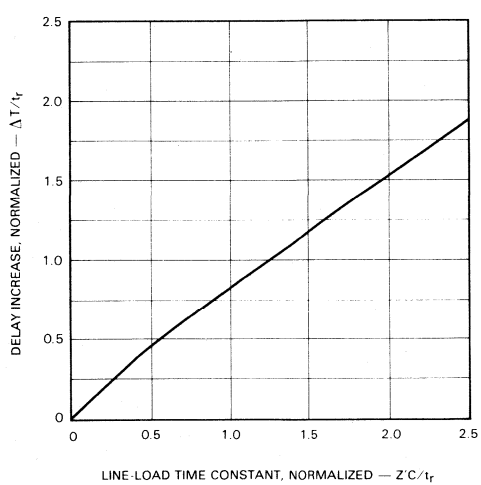


Fig. 4-11 Increase in 50% Point Delay Due to Capacitive Loading at the End of the Line, Normalized to t_r

DISTRIBUTED LOADING EFFECTS ON LINE CHARACTERISTICS

When capacitive loads such as ECL inputs are connected along a transmission line, each one causes a reflection with a polarity opposite to that of the incident wave. Reflections from two adjacent loads tend to overlap if the time required for the incident wave to travel from one load to the next is equal to or less than the signal rise time.[5] *Figure 4-12a* illustrates an arrangement for observing the effects of capacitive loading, while *Figure 4-12b* shows an incident wave followed by reflections from two capacitive loads. The two capacitors causing the reflections are separated by a distance requiring a travel time of 1 ns. The two reflections return to the source 2 ns apart, since it takes 1 ns longer for the incident wave to reach the second capacitor and an additional 1 ns for the second reflection to travel back to the source. In the upper trace of *Figure 4-12b,* the input signal rise time is 1 ns and there are two distinct reflections, although the trailing edge of the first overlaps the leading edge of the second. The input rise time is longer in the middle trace, causing a greater overlap. In the lower trace, the 2 ns input rise time causes the two reflections to merge and appear as a single reflection which is relatively constant (at ≈ −10%) for half its duration. This is about the same reflection that would occur if the 93 Ω line had a middle section with an impedance reduced to 75 Ω.

With a number of capacitors distributed all along the line of *Figure 4-12a,* the combined reflections modify the observed input waveform as shown in the top trace of *Figure 4-12c*. The reflections persist for a time equal to the 2-way line delay (15 ns), after which the line voltage attains its final value. The waveform suggests a line terminated with a resistance greater than its characteristic impedance ($R_T > Z_0$). This analogy is strengthened by observing the effect of reducing R_T from 93 Ω to 75 Ω, which leads to the middle waveform of *Figure 4-12c*. Note that the final (steady state) value of the line voltage is reduced by about the same amount as that caused by the capacitive reflections. In the lower trace of *Figure 4-12c* the source resistance R_S is reduced from 93 Ω to 75 Ω, restoring both the intial and final line voltage values to the same amplitude as the final value in the upper trace. From the standpoint of providing a desired signal voltage on the line and impedance matching at either end, the effect of distributed capacitive loading can be treated as a reduction in line impedance.

The reduced line impedance can be calculated by considering the load capacitance C_L as an increase in the intrinsic line capacitance C_0 along that portion of the line where the loads are connected.[6] Denoting this length of line as l, the distributed value C_D of the load capacitance is as follows.

$$C_D = \frac{C_L}{l}$$

C_D is then added to C_0 in *Equation 4-1* to determine the reduced line impedance Z_0.

$$Z_0' = \sqrt{\frac{L_0}{C_0 + C_D}} = \sqrt{\frac{L_0}{C_0\left(1 + \frac{C_D}{C_0}\right)}} \qquad (4\text{-}13)$$

$$Z_0' = \frac{\sqrt{\frac{L_0}{C_0}}}{\sqrt{1 + \frac{C_D}{C_0}}} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}}$$

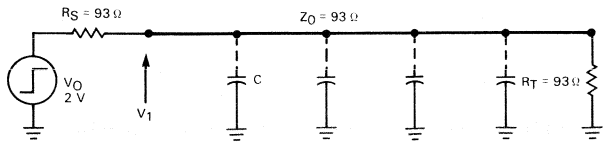
In the example of *Figure 4-12c*, the total load capacitance is 33 pF while the total intrinsic line capacitance C_0 is 60 pF (note that the ratio C_D/C_0 is the same as C_L/C_0). The calculated value of the reduced impedance is thus.

$$Z_0' = \frac{93}{\sqrt{1 + \frac{33}{60}}} = \frac{93}{\sqrt{1.55}} = 75\ \Omega \qquad (4\text{-}14)$$

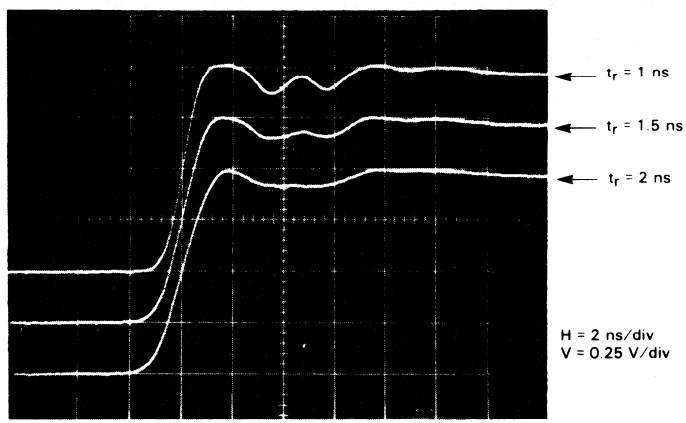
This correlates with the results observed in *Figure 4-12c* when R_T and R_S are reduced to 75 Ω.

The distributed load capacitance also increases the line delay, which can be calculated from *Equation 4-2.*

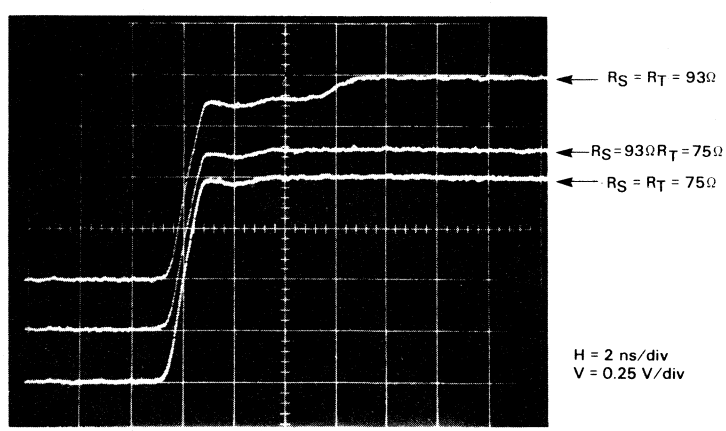
$$\delta' = \sqrt{L_0(C_0 + C_D)} = \sqrt{L_0 C_0}\ \sqrt{1 + \frac{C_D}{C_0}} = \delta \sqrt{1 + \frac{C_D}{C_0}} \quad (4\text{-}15)$$



a. Arrangement for Observing Capacitive Loading Effects



b. Capacitive Reflections Merging as Rise Time Increases



c. Matching the Altered Impedance of a Capacitively Loaded Line

Fig. 4-12 Capacitive Reflections and Effects on Line Characteristics

The line used in the example of *Figure 4-12c* has an intrinsic delay of 6 ns and a loaded delay of 7.5 ns which checks with *Equation 4-15*.

$$l\delta' = l\delta\sqrt{1.55} = 6\sqrt{1.55} = 7.5\ ns \tag{4-16}$$

Equation 4-15 can be used to predict the delay for a given line and load. The ratio C_D/C_0 (hence the loading effect) can be minimized for a given loading by using a line with a high intrinsic capacitance C_0.

Worst case reflections from a capacitvely loaded section of transmission line can be accurately predicted by using the modified impedance of *Equation 4-9*.[6] When a signal originates on an unloaded section of line, the effective reflection coefficient is as follows.

$$\rho = \frac{Z_0' - Z_0}{Z_0' + Z_0} \tag{4-17}$$

MISMATCHED LINES

Reflections occur not only from mismatched load and source impedances but also from changes in line impedance. These changes could be caused by bends in coaxial cable, unshielded twisted pair in contact with metal, or mismatch between PC board traces and backplane wiring. With the coax or twisted pair, line impedance changes run about 5 to 10% and reflections are usually no problem since the percent reflection is roughly half the percent change in impedance. However, between PC board and backplane wiring, the mismatch can be 2 or 3 to 1. This is illustrated in *Figure 4-13* and analyzed in the lattice diagram of *Figure 4-14*. Line 1 is driven in the series terminated mode so that reflections coming back to the source are absorbed.

The reflection and transmission at the point where impedances differ is determined by treating the downstream line as though it were a terminating resistor. For the example of *Figure 4-13*, the reflection coefficient at the intersection of lines 1 and 2 for a signal traveling to the right is as follows.

$$\rho_{12} = \frac{Z_2 - Z_1}{Z_2 + Z_1} = \frac{93 - 50}{143} = +0.3 \tag{4-18}$$

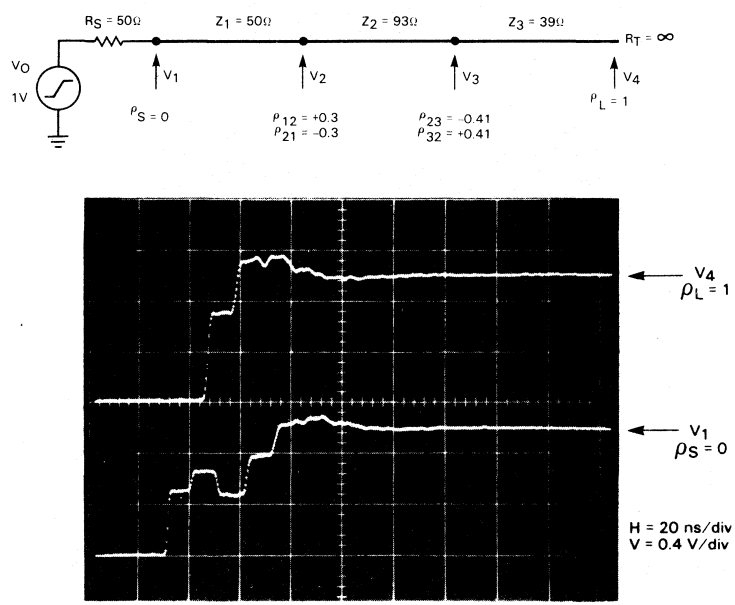


Fig. 4-13 Reflections from Mismatched Lines

Thus the signal reflected back toward the source and the signal continuing along line 2 are, respectively, as follows.

$$V_{1r} = \rho_{12} V_1 = +0.3\, V_1 \tag{4-19a}$$

$$V_2 = (1 + \rho_{12}) V_1 = +1.3\, V_1 \tag{4-19b}$$

At the intersection of lines 2 and 3, the reflection coefficient for signals traveling to the right is determined by treating Z_3 as a terminating resistor.

$$\rho_{23} = \frac{Z_3 - Z_2}{Z_3 + Z_2} = \frac{39 - 93}{132} = -0.41 \tag{4-20}$$

When V_2 arrives at this point, the reflected and transmitted signals are as follows.

$$V_{2r} = \rho_{23} V_2 = -0.41\, V_2 = (-0.41)(1.3)\, V_1 = -0.53\, V_1$$
$$V_3 = (1 + \rho_{23}) V_2 = 0.59\, V_2 = (0.59)(1.3)\, V_1 = 0.77\, V_1 \tag{4-21a,b}$$

Voltage V_3 is doubled in magnitude when it arrives at the open-ended output, since ρ_L is +1. This effectively cancels the voltage divider action between R_S and Z_1.

$$\begin{aligned} V_4 &= (1 + \rho_L) V_3 = (1 + \rho_L)(1 + \rho_{23}) V_2 \\ &= (1 + \rho_L)(1 + \rho_{23})(1 + \rho_{12}) V_1 \\ &= (1 + \rho_L)(1 + \rho_{23})(1 + \rho_{12}) \frac{V_O}{2} \\ V_4 &= (1 + \rho_{23})(1 + \rho_{12}) V_O \end{aligned} \tag{4-22}$$

Thus, *Equation 4-22* is the general expression for the intial step of output voltage for three lines when the input is series terminated and the output is open-ended.

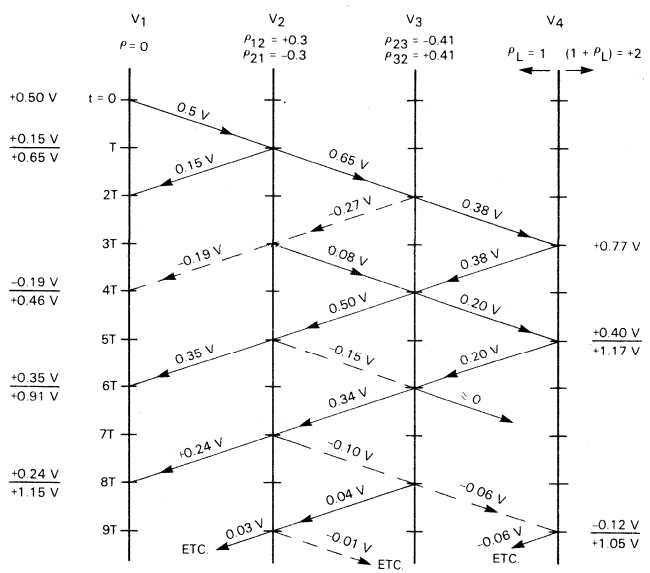


Fig. 4-14 Lattice Diagram for the Circuit of Figure 4-13

Note that the reflection coefficients at the intersections of lines 1 and 2 and lines 2 and 3 in *Figure 4-13* have reversed signs for signals traveling to the left. Thus the voltage reflected from the open output and the signal reflecting back and forth on line 2 both contribute additional increments of output voltage in the same polarity as V_0. Lines 2 and 3 have the same delay time, therefore the two aforementioned increments arrive at the output simultaneously at time 5T on the lattice diagram *(Figure 4-14).*

In the general case of series lines with different delay times, the vertical lines on the lattice diagram should be spaced apart in the ratio of the respective delays. *Figure 4-15* shows this for a hypothetical case with delay ratios 1:2:3. For a sequence of transmission lines with the highest impedance line in the middle, at least three output voltage increments with the same polarity as V_0 occur before one can occur of opposite polarity. On the other hand, if the middle line has the lowest impedance, the polarity of the second increment of output voltage is the opposite of V_0. The third increment of output voltage has the opposite polarity, for the time delay ratios of *Figure 4-15*.

When transmitting logic signals, it is important that the initial step of line output voltage pass through the threshold region of the receiving circuit, and that the next two increments of output voltage augment the initial step. Thus in a series terminated sequence of three mismatched lines, the middle line should have the highest impedance.

RISE TIME VERSUS LINE DELAY

When the 2-way line delay is less than the rise time of the input wave, any reflections generated at the end of the line are returned to the source before the input transition is completed. Assuming that the generator has a finite source resistance, the reflected wave adds algebraically to the input wave while it is still in transition, thereby changing the shape of the input. This effect is illustrated in *Figure 4-16,* which shows input and output voltages for several comparative values of rise time and line delay.

In *Figure 4-16b* where the rise time is much shorter than the line delay, V_1 rises to an initial value of 1 V. At time T later, V_T rises to 0.5 V. *i.e.,* $1 + \rho_L = 0.5$. The negative reflection arrives back at the source at time 2T, causing a net change of −0.4 V, *i.e.,* $(1 + \rho_S)\ (-0.5) = -0.4$.

The negative coefficient at the source changes the polarity of the other 0.1 V of the reflection and returns it to the end of the line, causing V_T to go positive by another 50 mV at time 3T. The remaining 50 mV is inverted and reflected back to the source, where its effect is barely distinguishable as a small negative change at time 4T.

In *Figure 4-16c*, the input rise time (0 to 100%) is increased to such an extent that the input ramp ends just as the negative reflection arrives back at the source end. Thus the input rise time is equal to 2T.

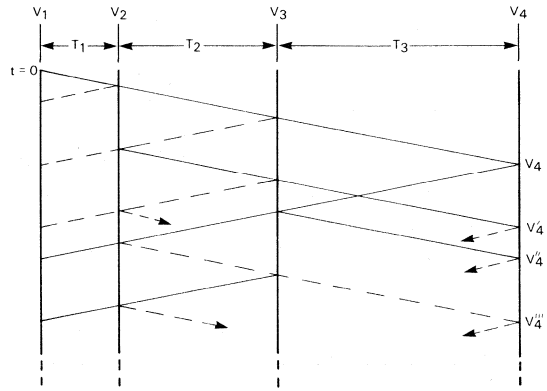
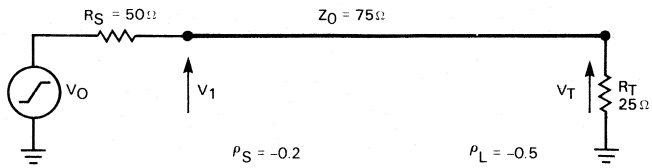
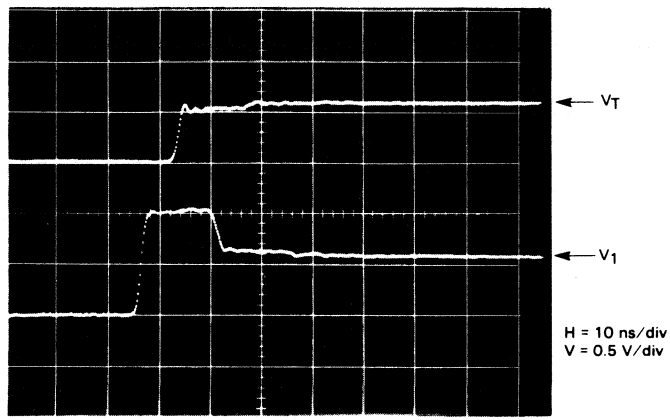


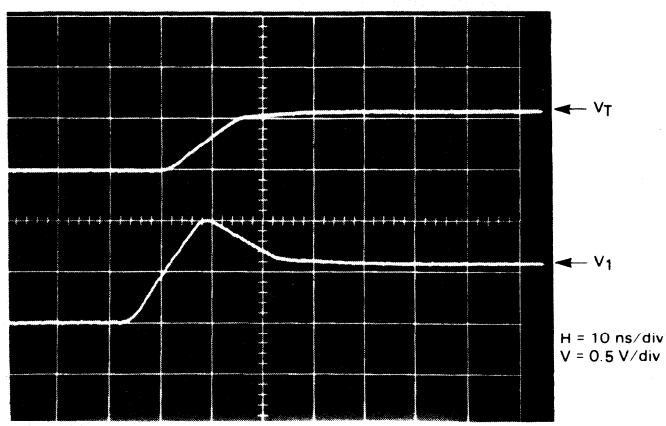
Fig. 4-15 Lattice Diagram for Three Lines with Delay Ratios 1:2:3



a. Test Arrangement for Rise Time Analysis



b. Line Voltages for $t_r \ll T$



c. Line Voltages for $t_r = 2T$

Fig. 4-16 Line Voltages for Various Ratios of Rise Time to Line Delay

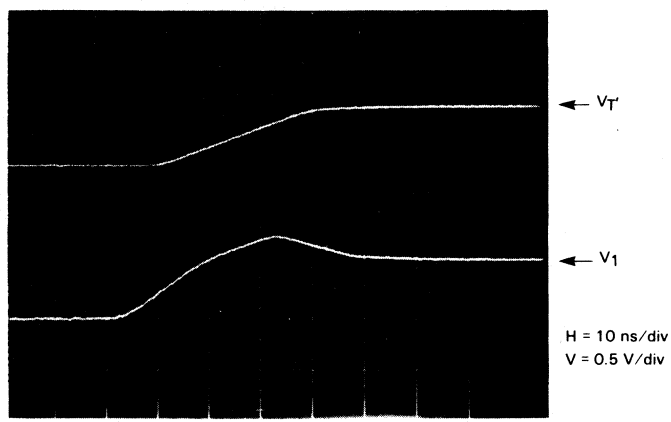
The input rise time is increased to 4T in *Figure 4-16d,* with the negative reflection causing a noticeable change in input slope at about its midpoint. This change in slope is more visible in the double exposure photo of *Figure 4-16e,* which shows V_1 (t_r still set for 4T) with and without the negative reflection. The reflection was eliminated by terminating the line in its characteristic impedance.

The net input voltage at any particular time is determined by adding the reflection to the otherwise unaffected input. It must be remembered that the reflection arriving back at the input at a given time is proportional to the input voltage at a time 2T earlier. The value of V_1 in *Figure 4-16d* can be calculated by starting with the 1 V input ramp.

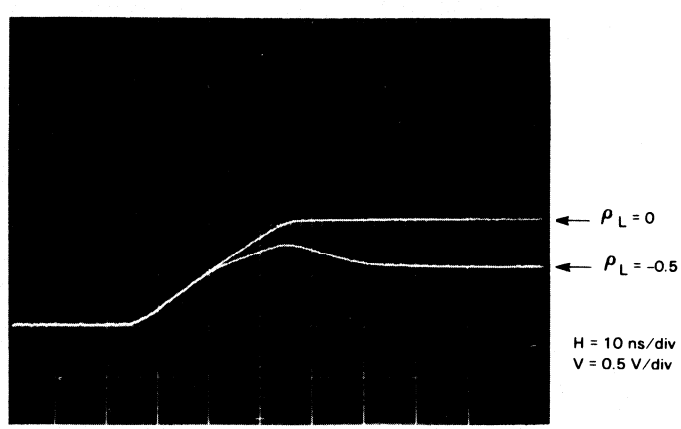
$$V_1 = \frac{1}{t_r} \cdot t \quad for\ 0 \leqslant t \leqslant 4T$$
$$= 1\ V \quad for\ t \geqslant 4T \qquad (4\text{-}23)$$

the reflection from the end of the line is

$$V_r = \frac{\rho_L\ (t - 2T)}{t_r} \qquad (4\text{-}24)$$



d. Line Voltages for t_r = 4T



e. Input Voltage With and Without Reflection

Fig. 4-16. Line Voltages for Various Ratios of Rise Time to Line Delay

the portion of the reflection that appears at the input is

$$V_r' = \frac{(1 + \rho_S)\,\rho_L\,(t - 2T)}{t_r} \tag{4-25}$$

the net value of the input voltage is the sum.

$$V_1' = \frac{t}{t_r} + \frac{(1 + \rho_S)\,\rho_L\,(t - 2T)}{t_r} \tag{4-26}$$

The peak value of the input voltage in *Figure 4-16d* is determined by substituting values and letting t equal 4T.

$$\begin{aligned} V_1' &= 1 + \frac{(0.8)\,(-0.5)\,(4T - 2T)}{t_r} \\ &= 1 - 0.4\,(0.5) = 0.8\ V \end{aligned} \tag{4-27}$$

After this peak point, the input ramp is no longer increasing but the reflection is still arriving. Hence the net value of the input voltage decreases. In this example, the later reflections are too small to be detected and the input voltage is thus stable after time 6T. For the general case of repeated reflections, the net voltage $V_{1(t)}$ seen at the driven end of the line can be expressed as follows, where the signal caused by the generator is $V_{1(t)}$.

4

$$V'_{1(t)} = V_{1(t)} \qquad \text{for } 0 < t < 2T$$

$$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L V_{1(t-2T)} \qquad \text{for } 2T < t < 4T$$

$$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L V_{1(t-2T)} + (1 + \rho_S)\,\rho_S \rho_L{}^2 V_{1(t-4T)} \qquad \text{for } 4T < t < 6T$$

$$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L V_{1(t-2T)} + (1 + \rho_S)\,\rho_S \rho_L{}^2 V_{1(t-4T)} + (1 + \rho_S)\,\rho_S{}^2 \rho_L{}^3 V_{1(t-6T)} \qquad \text{for } 6T < t < 8T$$

$$\textit{etc.} \tag{4-28}$$

The voltage at the output end of the line is expressed in a similar manner.

$$V_{T(t)} = 0 \qquad \text{for } 0 < t < T$$

$$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} \qquad \text{for } T < t < 3T$$

$$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} + (1 + \rho_L)\,\rho_S \rho_L V_{1(t-3T)} \qquad \text{for } 3T < t < 5T$$

$$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} + (1 + \rho_L)\,\rho_S \rho_L V_{1(t-3T)} + (1 + \rho_L)\,\rho_S{}^2 \rho_L{}^2 V_{1(t-5T)} \qquad \text{for } 5T < t < 7T$$

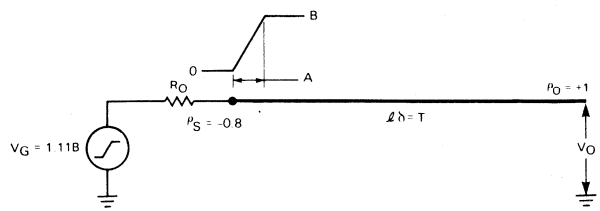
$$\textit{etc.} \tag{4-29}$$

RINGING

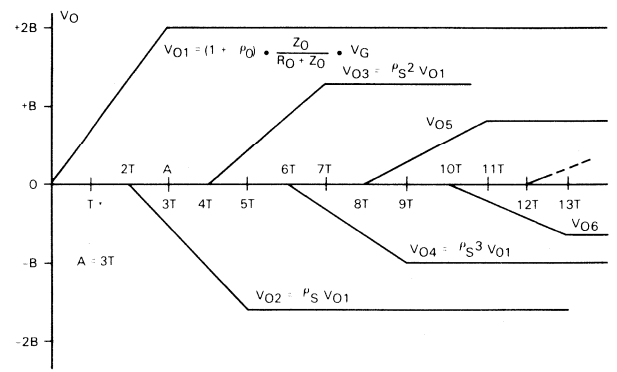
Multiple reflections occur on a transmission line when neither the signal source impedance nor the termination (load) impedance matches the line impedance. When the source reflection coefficient ρ_S and the load reflection coefficient ρ_L are of opposite polarity, the reflections alternate in polarity. This causes the signal voltage to oscillate about the final steady state value, commonly recognized as ringing.

When the signal rise time is long compared to the line delay, the signal shape is distorted because the individual reflections overlap in time. The basic relationships among rise time, line delay, overshoot and undershoot are shown in a simplified diagram, *Figure 4-17*. The incident wave is a ramp of amplitude B and rise duration A. The reflection coefficient at the open-ended line ouput is +1 and the source reflection coefficient is assumed to be -0.8, *i.e.*, $R_O = Z_O/9$.

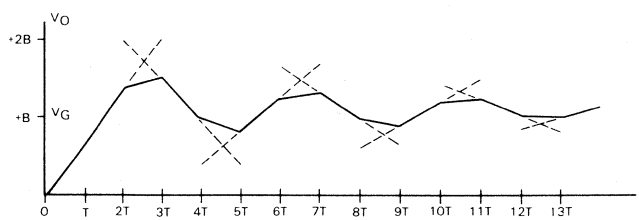
Figure 4-17b shows the individual reflections treated separately. Rise time A is assumed to be three times the line delay T. The time scale reference is the line output and the first increment of output voltage V_{O1} rises to 2B in the time interval A. Simultaneously, a positive reflection (not shown) of amplitude B is generated and travels to the source, whereupon it is multiplied by -0.8 and returns toward the end of the line. This negative-going ramp starts at time 2T (twice the line delay) and doubles to -1.6B at time 2T+A.



a. Ramp Generator Driving Open-ended Line



b. Increments of Output Voltage Treated Individually



c. Net Output Signal Determined by Superposition

Fig. 4-17 Basic Relationships Involved in Ringing

The negative-going increment also generates a reflection of amplitude −0.8B which makes the round trip to the source and back, appearing at time 4T as a positive ramp rising to +1.28B at time 4T+A. The process of reflection and re-reflection continues, and each successive increment changes in polarity and has an amplitude of 80% of the preceding increment.

In *Figure 4-17c,* the output increments are added algebraically by superposition. The starting point of each increment is shifted upward to a voltage value equal to the algebraic sum of the quiescent levels of all the preceding increments (*i.e.,* 0, 2B, 0.4B, 1.68B, etc.). For time intervals when two ramps occur simultaneously, the two linear functions add to produce a third ramp that prevails during the overlap time of the two increments.

It is apparent from the geometric relationships, that if the ramp time A is less than twice the line delay, the first output increment has time to rise to the full 2B amplitude and the second increment reduces the net output voltage to 0.4B. Conversely, if the line delay is very short compared to the ramp time, the excursions about the final value V_G are small.

Figure 4-17c shows that the peak of each excursion is reached when the earlier of the two constituent ramps reaches its maximum value, with the result that the first peak occurs at time A. This is because the earlier ramp has a greater slope (absolute value) than the one that follows.

Actual waveforms such as produced by ECL or TTL do not have a constant slope and do not start and stop as abruptly as the ramp used in the example of *Figure 4-17.* Predicting the time at which the peaks of overshoot and undershoot occur is not as simple as with ramp excitation. A more rigorous treatment is required, including an expression for the driving waveform which closely simulates its actual shape. In the general case, a peak occurs when the sum of the slopes of the individual signal increment is zero.

SUMMARY

The foregoing discussions are by no means an exhaustive treatment of transmission line characteristics. Rather, they are intended to focus attention on the general methods used to determine the interactions between high speed logic circuits and their interconnections. Considering an interconnection in terms of distributed rather than lumped inductance and capacitance leads to the line impedance concept. Mismatch between this characteristic impedance and the terminations causes reflections and ringing.

Series termination provides a means of absorbing reflections when it is likely that discontinuities and/or line impedance changes will be encountered. A disadvantage is that the incident wave is only one-half the signal swing, which limits load placement to the end of the line. ECL input capacitance increases the rise time at the end of the line, thus increasing the effective delay. With parallel termination, *i.e.,* at the end of the line, loads can be distributed along the line. ECL input capacitance modifies the line characteristics and should be taken into account when determining line delay.

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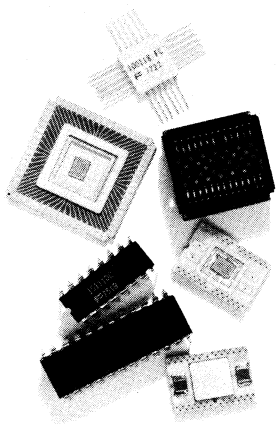
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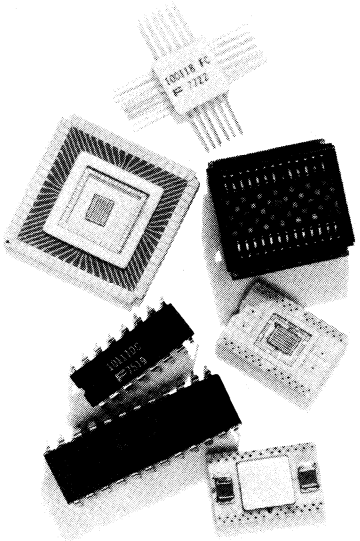
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Chapter 5
ECL INTERCONNECTIONS

INTRODUCTION

All of Fairchild's ECL input and output impedances are designed to accomodate various methods of driving and terminating interconnections. Controlled wiring impedance makes it possible to use simplified equivalent circuits to determine limiting conditions. Guidelines and recommendations are intended to help the designer achieve good system performance, consistent with conservative design practice.

PC BOARD TRANSMISSION LINES

Strictly speaking, transmission lines are not required with the relatively slow edge speeds of F10K and F95K ECL, and are not always required for F100K ECL with faster edge speeds, but when used, they provide the advantages of predictable interconnect delays as well as reflection and ringing control through impedance matching. Two common types of PC board transmission lines are microstrip and stripline, *Figure 5-1*. Stripline requires multilayer construction techniques, while microstrip uses ordinary double-clad boards.

Stripline is used where packing density is a high priority because increasing the interconnect layers provides short signal paths. Boards with as many as 14 layers have been used in ECL systems.

Microstrip offers easier fabrication and higher propagation velocity than stripline, but the routing for a complex system may require more design effort. In *Figure 5-1a,* the ground plane can be a part of the V_{EE} distribution as long as adequate bypassing from V_{EE} to V_{CC} (ground) is provided. Also, signal routing is simplified and an extra voltage plane is obtained by bonding two microstrip structures back to back, *Figure 5-1c.*

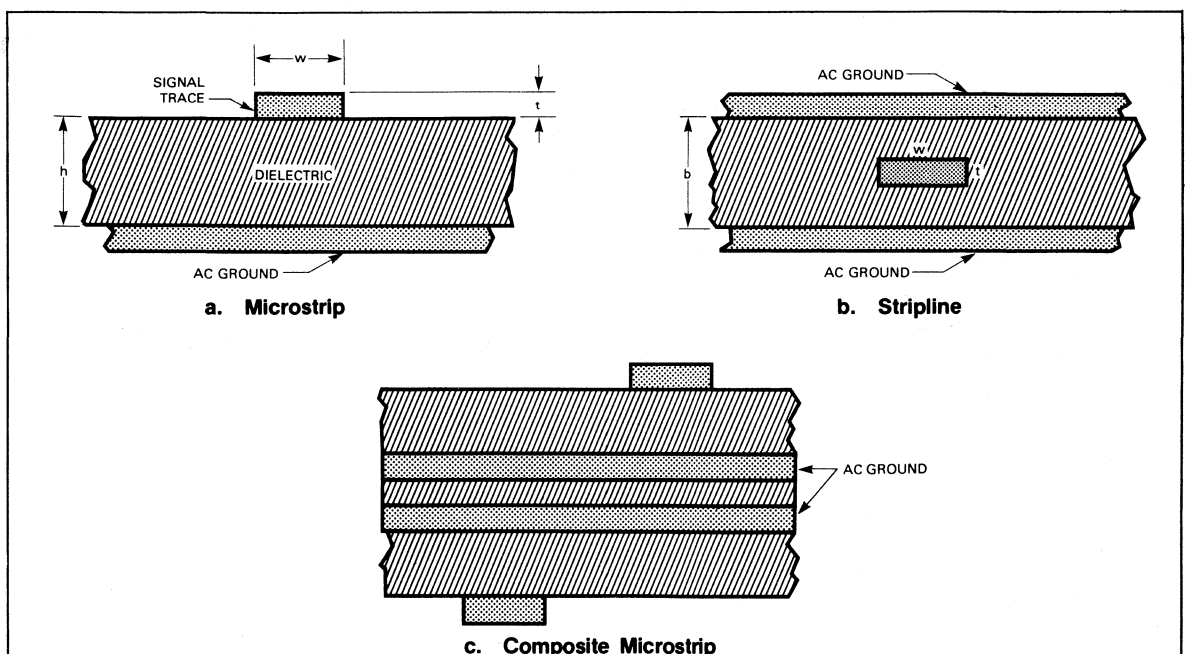


Fig. 5-1 Transmission Lines on Circuit Boards

Microstrip

Equation 5-1 relates microstrip characteristic impedance, dielectric constant and dimensions.[1] Electric field fringing requires that the ground extend beyond each edge of the signal trace by a distance no less than the trace width.

$$Z_0 = \left(\frac{60}{\sqrt{0.475\ \epsilon_r + 0.67}}\right) \quad ln \quad \left(\frac{4\,h}{0.67\,(0.8\,w + t)}\right)$$

$$= \left(\frac{87}{\sqrt{\epsilon_r + 1.41}}\right) \quad ln \quad \left(\frac{5.98\,h}{0.8\,w + t}\right) \qquad (5\text{-}1)$$

where h = dielectric thickness, w = trace width, t = trace thickness, ϵ_r = board material dielectric constant relative to air

Equation 5-1 was developed from the impedance formula for a wire over ground plane transmission line, *Equation 5-2.*

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}}\right) \quad ln \quad \left(\frac{4\,h}{d}\right) \qquad (5\text{-}2)$$

where d = wire diameter, h = distance from ground to wire center

Comparing *Equations 5-1* and *5-2,* the term 0.67 (0.8w + t) shows the equivalence between a round wire and a rectangular conductor. The term 0.475 ϵ_r + 0.67 is the *effective* dielectric constant for microstrip, considering that a microstrip line has a compound dielectric consisting of the board material and air. The effective dielectric constant is determined by measuring propagation delay per unit of line length and using the following relationship.

$$\delta = 1.016 \bullet \sqrt{\epsilon_r} \quad ns/ft \qquad (5\text{-}3)$$

where δ = propagation delay, ns/ft.

Propagation delay is a property of the dielectric material rather than line width or spacing. The coefficient 1.016 is the reciprocal of the velocity of light in free space. Propagation delay for microstrip lines on glass-filled G-10 epoxy boards is typically 1.77 ns/ft, yielding an effective dielectric constant of 3.04. Using this value in *Equation 5-1, Figure 5-2* provides microstrip line impedance as a function of width for several G-10 epoxy board thicknesses. *Figure 5-3* shows the related C_0 values, useful for determining capacitive loading effects on line characteristics, (*Equation 4-15*).

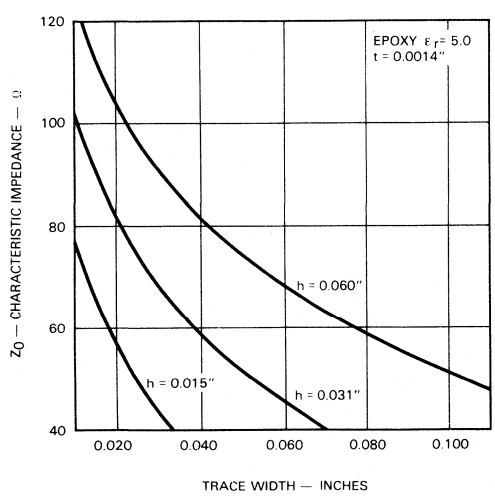


Fig. 5-2 Microstrip Impedance Versus Trace Width, G-10 Epoxy

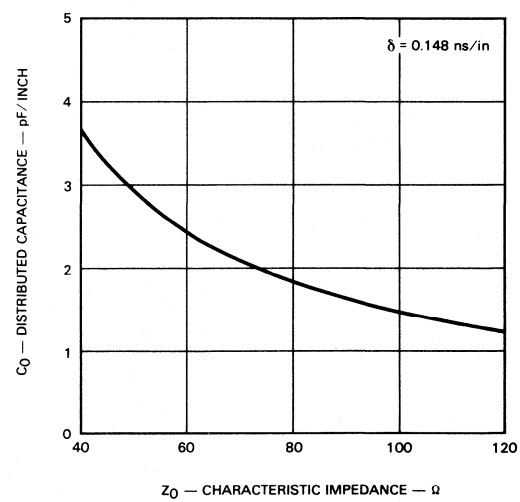


Fig. 5-3 Microstrip Distributed Capacitance Versus Impedance, G-10 Epoxy

System designers should ascertain tolerances on board dimensions, dielectric constant and trace width etching in order to determine impedance variations. If conformal coating is used the effective dielectric constant of microstrip is increased, depending on the coating material and thickness.

Stripline

Stripline conductors are totally imbedded. As a result, the board material determines the dielectric constant. G-10 epoxy boards have a typical propagation delay of 2.26 ns/ft. *Equation 5-4* is used to calculate stripline impedances.[1-2]

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}}\right) \quad ln \quad \left(\frac{4b}{0.67\,(0.8\,w + t)}\right) \qquad (5\text{-}4)$$

where b = distance between ground planes, w = trace width, t = trace thickness, $w/(t\text{-}b) < 0.35$ and $t/b < 0.25$.

Figure 5-4 shows stripline impedance as a function of trace width, using *Equation 5-4* and various ground plane separations for G-10 glass-filled epoxy boards. Related values of C_0 are plotted in *Figure 5-5*.

PARALLEL TERMINATION

Terminating a line at the receiving end with a resistance equal to the characteristic line impedance is called parallel termination, *Figure 5-6a.* F10K, F100K and F95K circuits do not have internal pull down

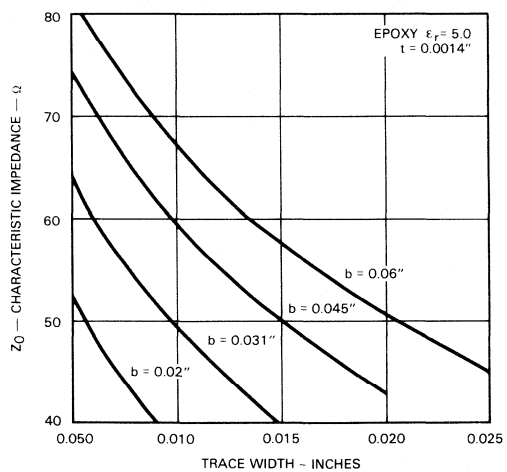


Fig. 5-4 Stripline Impedance Versus Trace Width, G-10 Epoxy

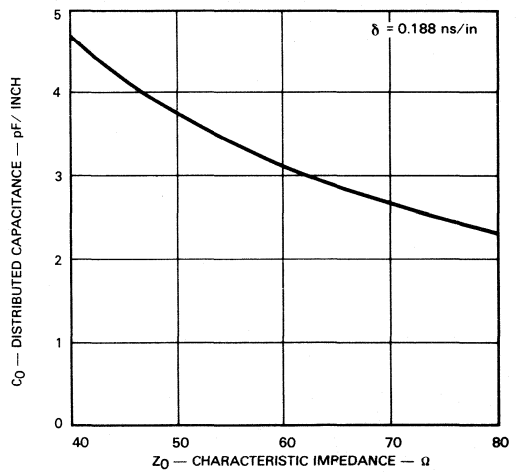
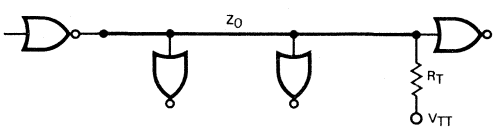
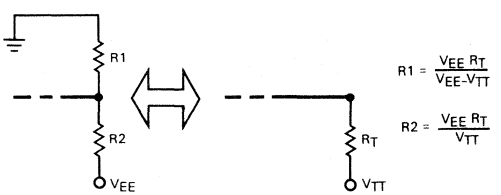


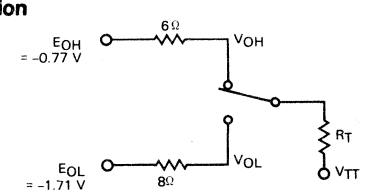
Fig. 5-5 Stripline Distributed Capacitance Versus Impedance, G-10 Epoxy



a. Parallel Termination



b. Thevenin Equivalent of R_T and V_{TT}



c. Equivalent Circuit for Determining Approximate V_{OH} and V_{OL} Levels

Fig. 5-6. Parallel Termination

resistors on outputs, so the terminating resistor must be returned to a voltage more negative than V_{OL} to establish the LOW-state output voltage from the emitter follower. A -2 V termination return supply is commonly used. This minimizes power consumption and correlates with standard test specifications for ECL circuits. A pair of resistors connected in series between ground (V_{CC}) and the V_{EE} supply can provide the Thevenin equivalent of a single resistor to -2 V if a separate termination supply is not available, *Figure 5-6b.* The average power dissipation in the Thevenin equivalent resistors is about 10 times the dissipation in the single resistor returned to -2 V, as shown in *Figure 6-14.* For either parallel termination method, decoupling capacitors are required between the supply and ground (Chapter 6).

F10K, F100K and F95K output transistors are designed to drive low impedance loads and have a maximum output current rating of 50 mA. The circuits are specified and tested with a 50 Ω load returned to -2 V. This gives nominal output levels of -0.9 V at 22 mA and -1.75 V at 5 mA. Output levels will be different with other load currents because of the transistor output resistance. This resistance is nonlinear with load current since it is due, in part, to the base emitter voltage of the emitter follower, which is logarithmic with output current. With the standard 50 Ω load, the effective source resistance is approximately 6 Ω in the HIGH state and 8 Ω in the LOW state.

The foregoing values of output voltage, output current, and output resistance are used to estimate quiescent output levels with different loads. An equivalent circuit is shown in *Figure 5-6c.* The ECL circuit is assumed to contain two internal voltage sources E_{OH} and E_{OL} with series resistances of 6 Ω and 8 Ω respectively. The values shown for E_{OH} and E_{OL} are determined as follows.

$$E_{OH} = V_{OH} + I_{OH} R_O = -0.90 + (22\ mA)\ (6\ \Omega) = -0.77\ V$$

$$E_{OL} = V_{OL} + I_{OL} R_O = -1.75 + (5\ mA)\ (8\ \Omega) = -1.71\ V$$

using 25°C values of V_{OH} and V_{OL}

An ECL output can drive two or more lines in parallel, provide the maximum rated current is not exceeded. Another consideration is the effect of various loads on noise margins. For example, two parallel 75 Ω terminations to -2 V (*Figure 5-6c*) give output levels of approximately -0.94 V and -1.76 V. Noise margins are thus 40 mV less in the HIGH state and 10 mV more in the LOW state, compared to 50 Ω load conditions. Conversely, a single 75 Ω load to -2 V causes noise margins 40 mV greater in the HIGH state and 10 mV less in the LOW state, compared to a 50 Ω load.

The magnitude of reflections from the terminated end of the line depends on how well the termination resistance R_T matches the line impedance Z_0. The ratio of the reflected voltage to the incident voltage V_i is the reflection coefficient ρ

$$\frac{V_r}{V_i} = \rho = \frac{R_T - Z_0}{R_T + Z_0} \qquad (5\text{-}5)$$

The initial signal swing at the termination is the sum of the incident and reflected voltages. The ratio of termination signal to incident signal is thus:

$$\frac{V_T}{V_i} = 1 + \rho = \frac{2\ R_T}{R_T + Z_0} \qquad (5\text{-}6)$$

The degree of reflections which can be tolerated varies in different situations, but to allow for worst case circuits, a good rule of thumb is to limit reflections to 15% to prevent excursions into the threshold region of the ECL inputs connected along the line. The range of permissible values of R_T as a function of Z_0 and the reflection coefficient limitations can be determined by rearranging *Equation 5-5.*

$$R_T = Z_0 \frac{1 + \rho}{1 - \rho} \qquad (5\text{-}7)$$

Using 15% reflection limits as examples, the range of R_T/Z_0 ratio is as follows.

$$\frac{1.15}{0.85} > \frac{R_T}{Z_0} > \frac{0.85}{1.15} \qquad 1.35 > \frac{R_T}{Z_0} > 0.74 \tag{5-8}$$

The permissible range of the R_T/Z_0 ratio determines the tolerance ranges for R_T and Z_0. For example, using the foregoing ratio limits, R_T tolerances of ±10% allow Z_0 tolerance limits of +22% and -19%; R_T tolerances of ±5% allow Z_0 tolerance limits of +28% and -23%.

An additional requirement on the maximum value of R_T is related to the value of quiescent I_{OH} current needed to insure sufficient negative-going signal swing when the ECL driver switches from the HIGH state to the LOW state. The npn emitter follower output of the ECL circuit cannot act as a voltage source driver for negative-going transitions. When the voltage at the base of the emitter follower starts going negative as a result of an internal state change, the output current of the emitter follower starts to decrease. The transmission line responds to the decrease in current by producing a negative-going change in voltage. The ratio of the voltage change to the current change is, of course, the characteristic impedance Z_0. Since the maximum decrease in current that the line can experience is from I_{OH} to zero, the maximum negative-going transition which can be produced is the product I_{OH} Z_0.

If the I_{OH} Z_0 product is greater than the normal negative-going signal swing, the emitter follower responds by limiting the current change, thereby controlling the signal swing. If, however, the I_{OH} Z_0 product is too small, the emitter follower is momentarily turned off due to insufficient forward bias of its base-emitter junctions, causing a discontinuous negative-going edge such as the one shown in *Figure 5-17*. In the output LOW state the emitter follower is essentially non-conducting for V_{OL} values more positive than about -1.6 V. Using this value as a criterion and expressing I_{OH} and V_{OH} in terms of the equivalent circuit of *Figure 5-6c,* an upper limit on the value of R_T can be developed.

$$\Delta V = I_{OH} Z_O > 1.6 - |V_{OH}|$$

$$\left(\frac{E_{OH} - V_{TT}}{R_O + R_T}\right) Z_0 > 1.6 - \left|\frac{V_{TT} R_O + E_{OH} R_T}{R_O + R_T}\right| \tag{5-9}$$

$$R_T < \frac{(E_{OH} - V_{TT})\, Z_0 - (1.6 - |V_{TT}|)\, R_O}{1.6 - |E_{OH}|}$$

For a V_{TT} of -2 V, R_0 of 6 Ω and E_{OH} of -0.77 V, *Equation 5-9* reduces to

$$R_T < 1.48\, Z_0 + 2.9\ \Omega$$

For Z_0 = 50 Ω, the emitter follower cuts off during a negative-going transition if R_T exceeds 77 Ω. Changing the voltage level criteria to -1.65 V to insure continuous conduction in the emitter follower gives an upper limit of 72 Ω for a 50 Ω line. For a line terminated at the receiving end with a resistance to -2 V, a rough rule-of-thumb is that termination resistance should not exceed line impedance by more than 40%. This insures a satisfactory negative-going signal swing to ECL inputs connected along the line. The quiescent V_{OL} level, after all reflections have damped out, is determined by R_T and the ECL output characteristic.

The input impedance of ECL circuits is predominately capacitive. A single-function input has an effective value of 2.75 pF for F10K and F95K and about 1.5 pF for F100K, as determined by its effect on reflected and transmitted signals on transmission lines. In practical calculations, a value of 3 pF is used for F10K and F95K, and a value of 2 pF should be used for F100K. In F11C calculations the value to be used could be either 2 pF or 3 pF depending on the circuit used. Approximately two-thirds of this capacitance is attributed to the internal circuitry and one-third to the package lead and internal bonding.

An input lead connected to several internal functions exhibits more than 3 pF for F10K and F95K circuits. For F100K circuits multiple input lines may appear to have up to 3-4 pF but never more. For example, the F10101 and F95101 quad OR/NOR gates have a Common Enable input connected internally to four gates. The capacitance for this type of input can be determined by assuming 1 pF for the package lead and 2 pF for each gate input, for a total of 9 pF. In the case of the F100102, there is an input connected internally to all five gates, but because of the philosophy of buffering these types of inputs in the F100K family this input appears as a unit load with a capacitance of approximately 2 pF. For applications such as a data bus, with two or more outputs connected to the same line, the capacitance of a passive LOW output can be taken as 2 pF.

Capacitive loads connected along a transmission line increase the propagation delay of a signal along the line. The modified delay can be determined by treating the load capacitance as an increase in the intrinsic distributed capacitance of the line, discussed in Chapter 4. The intrinsic capacitance of any stubs which connect the inputs to the line should be included in the load capacitance. The intrinsic capacitance per unit length for G-10 epoxy boards is shown in *Figures 5-3* and *5-5* for microstrip and stripline respectively. For other dielectric materials, the intrinsic capacitance C_0 can be determined by dividing the intrinsic delay δ *(Equation 5-3)* by the line impedance Z_0.

The length of a stub branching off the line to connect an input should be limited to insure that the signal continuing along the line past the stub has a continuous rise, as opposed to a rise (or fall) with several partial steps. The point where a stub branches off the line is a low impedance point. This creates a negative coefficient of reflection, which in turn reduces the amplitude of the incident wave as it continues beyond the branch point. If the stub length is short enough however, the first reflection returning from the end of the stub adds to the attenuated incident wave while it is still rising. The sum of the attenuated incident wave and the first stub reflection provides a step-free signal, although its rise time will be longer than that of the original signal. Satisfactory signal transitions can be assured by restricting stub lengths according to the recommendations for unterminated lines *(Figures 5-10, 5-11, 5-12, 5-13).* The same considerations apply when the termination resistance is not connected at the end of the line; a section of line continuing beyond the termination resistance should be treated as an unterminated line and its length restricted accordingly.

SERIES TERMINATION

Series termination requires a resistor between the driver and transmission line, *Figure 5-7.* The receiving end of the line has no termination resistance. The series resistor value should be selected so that when added to the driver source resistance, the total resistance equals the line impedance. The voltage divider action between the net series resistance and the line impedance causes an incident wave of half amplitude to start down the line. When the signal arrives at the unterminated end of the line, it doubles and is thus restored to full amplitude. Any reflections returning to the source are absorbed without further reflection since the line and source impedance match. This feature, source absorption, makes series termination attractive for interconnection paths involving impedance discontinuities, such as occur in backplane wiring.

A disadvantage of series termination is that driven inputs must be near the end of the line to avoid receiving a 2-step signal. The initial signal at the driver end is half amplitude, rising to full amplitude only after the reflection returns from the open end of the line. In *Figure 5-7*, one load is shown connected at point D, away from the line end. This input receives a full amplitude signal with a continuous edge if the distance l to the open end of the line is within recommended lengths for unterminated lines *(Figures 5-10, 5-11, 5-12,* and *5-13).*

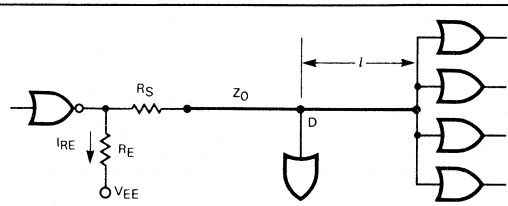


Fig. 5-7 Series Termination

The signal at the end has a slower rise time than the incident wave because of capacitive loading. The increase in rise time to the 50% point effectively increases the line propagation delay, since the 50% point of the signal swing is the input signal timing reference point. This added delay as a function of the product of line impedance and load capacitance is discussed in Chapter 4.

Quiescent V_{OH} and V_{OL} levels are established by resistor R_E *(Figure 5-7)*, which also acts with V_{EE} to provide the negative-going drive into R_S and Z_0 when the driver output goes to the LOW state. To determine the appropriate R_E value, the driver output can be treated as a simple mechanical switch which opens to initiate the negative-going swing. At this instant, Z_0 acts as a linear resistor returned to V_{OH}. Thus the components form a simple circuit of R_E, R_S and Z_0 in a series, connected between V_{EE} and V_{OH}. The initial current in this series circuit must be sufficient to introduce a 0.4 V transient into the line, which then doubles at the load end to give 0.8 V swing.

$$I_{RE} = \frac{V_{OH} - V_{EE}}{R_E + R_S + Z_0} \geq \frac{0.4}{Z_0} \tag{5-10}$$

Any I_{OH} current flowing in the line before the switch opens helps to generate the negative swing. This current may be quite small, however, and should therefore be ignored when calculating R_E.

Increasing the minimum signal swing into the line 30% to 0.52 V insures sufficient pull down current to handle reflection currents caused by impedance discontinuities and load capacitance. The appropriate R_E value is determined from the following relationship.

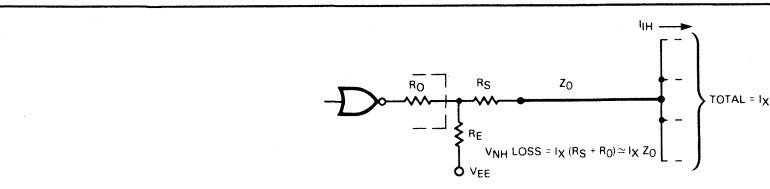
$$\frac{V_{OH} - V_{EE}}{R_E + R_S + Z_0} \geq \frac{0.52}{Z_0} \tag{5-11}$$

For the R_E range normally used, quiescent V_{OH} averages approximately 0.82 V. The value of R_S is equal to Z_0 minus R_O (R_O averages 7 Ω). Inserting these values and rearranging *Equation 5-11* gives the following.

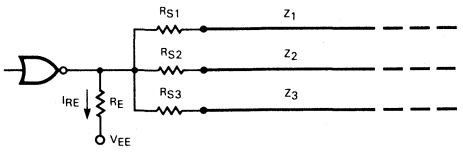
$$R_E \leq 6.4\,Z_0 + 7\,\Omega \tag{5-12}$$

Power dissipation in R_E is listed in *Figure 6-15*, which shows that dissipation in R_E is greater than in R_T of a parallel termination to -2 V, but less than in the two resistors of the Thevenin equivalent parallel termination.

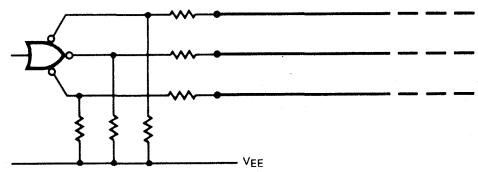
The number of driven inputs on a series terminated line is limited by the voltage drop across R_S in the quiescent HIGH state, caused by the finite input currents of the ECL loads. I_{IH} values are specified on data sheets for various types of inputs, with a 265 μA worst-case value for simple gate input. The voltage drop subtacts from the HIGH state noise margin as outlined in *Figure 5-8a*.



a. Noise Margin Loss Due to Load Input Current



b. Driving Several Lines from One Output



c. Using Multiple Output Element for Load Sharing

Fig. 5-8 Loading Considerations for Series Termination

However, there is more HIGH state noise margin initially, because there is less I_{OH} with the R_E load than with the standard 50 Ω load to -2 V. This makes V_{OH} more positive; the increase ranges from 60 mV for a 50 Ω line to 100 mV for a 100 Ω line. Using this V_{OH} increase as a limit on the voltage drop across R_S assures that the HIGH state noise margin is as good as in the parallel terminated case. Dividing the V_{OH} increase by $R_S + R_O$ (= Z_0) gives the allowed load input current (I_X in *Figure 5-8a*). This works out to 1.2 mA for a 50 Ω line, 1.1 mA for a 75 Ω line, and 1 mA for a 100 Ω line. Load input current greater than these values can be tolerated at some sacrifice in noise margin. If, for example, an additional 50 mV loss is feasible, the maximum values of current become 2.2 mA, 1.73 mA, and 1.5 mA for 50 Ω, 75 Ω, and 100 Ω lines respectively.

An ECL output can drive more than one series terminated line, as suggested in *Figure 5-8b,* if the maximum rated output current of 50 mA is not exceeded. Also, driving two or more lines requires a lower R_E value. This makes the quiescent I_{OH} higher and consequently V_{OH} lower, due to the voltage drop across R_O. This voltage drop decreases the HIGH state noise margin, which may become the limiting factor (rather than the maximum rated current), depending on the particular application. The appropriate R_E value can be determined using *Equation 5-13.*

$$\frac{1}{R_E} \geq \frac{1}{7.4\,Z_1 - R_{S1}} + \frac{1}{7.4\,Z_2 - R_{S2}} + \frac{1}{7.4\,Z_3 - R_{S3}} \qquad (5\text{-}13)$$

Circuits with multiple outputs (100112, 10110, 10111, 95110, 95111) provide an alternate means of driving several lines simultaneously *(Figure 5-8c).* Each output should be treated individually when assigning load distribution, line impedance, and R_E value.

UNTERMINATED LINES

Lines can be used without series or parallel termination if the line delay is short compared to the signal rise time. Ringing occurs because the reflection coefficient at the open (receiving) end of the line is positive (nominally +1) while the reflection coefficient at the driving end is negative (approximately -0.8). These opposite polarity reflection coefficients cause any change in signal voltage to be reflected back and forth, with a polarity change each time the signal is reflected from the driver. Net voltage change on the line is thus a succession of increments with alternating polarity and decreasing magnitude. The algebraic sum of these increments is the observed ringing. The general relationships among rise time, line delay, overshoot and undershoot are discussed in Chapter 4, using simple waveforms for clarity.

Excessive overshoot on the positive-going edge of the signal drives input transistors into saturation. Although this does not damage an ECL input, it does cause excessive recovery times and makes propagation delays unpredictable. Undershoot (following the overshoot) must also be limited to prevent signal excursions into the threshold region of the loads. Such excursions could cause exaggerated transition times at the driven circuit outputs, and could also cause multiple triggering of sequential circuits. Signal swing, exclusive of ringing, is slightly greater on unterminated lines than on parallel terminated lines; I_{OH} is less and I_{OL} is greater with the R_E load, *(Figure 5-9a)* making V_{OH} higher and V_{OL} lower.

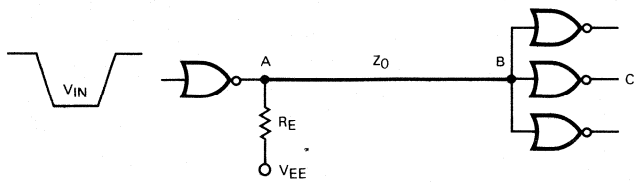
For worst case combinations of driver output and load input characteristics, a 35% overshoot limit insures that system speed is not compromised either by saturating an input on overshoot or extending into the threshold region on the following undershoot.

For distributed loading, ringing is satisfactorily controlled if the 2-way modified line delay does not exceed the 20% to 80% rise time of the driver output. This relationship can be expressed as follows, using the symbols from Chapter 4 and incorporating the effects of load capacitance on line delay.

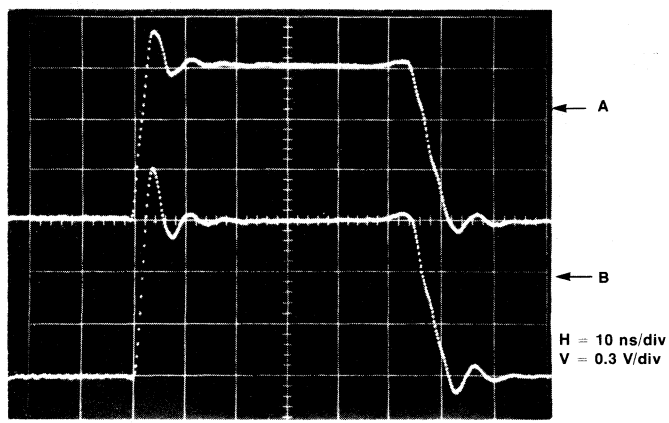
$$t_r = 2T' = 2l\delta' = 2l\delta \sqrt{1 + \frac{C_L}{lC_O}}$$

Solving this expression for the line length:

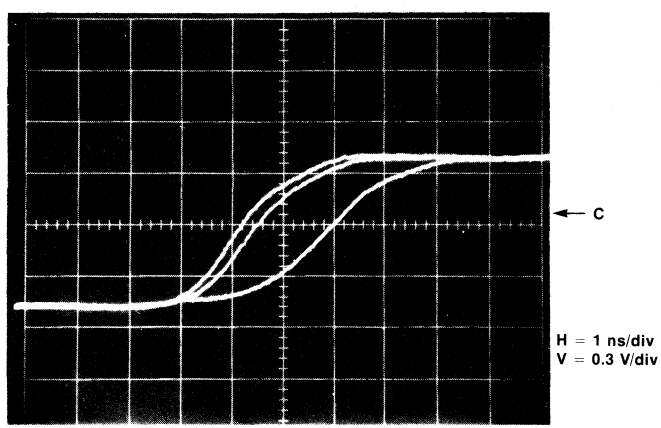
$$l_{max} = \frac{1}{2}\sqrt{\left(\frac{C_L}{C_O}\right)^2 + \left(\frac{t_r}{\delta}\right)^2} - \frac{C_L}{2C_O} \qquad (5\text{-}14)$$



a. Unterminated Line



b. Line Voltages Showing Stair-Step Trailing Edges



c. Load Gate Output Showing Net Propagation Increase for Increasing Values of R_E: 330 Ω, 510 Ω, 1 k Ω

Fig. 5-9 Effect of R_E Value on Trailing Edge Propagation

The shorter the rise time, the shorter the permissible line length. For F10K and F95K ECL, the minimum rise time from 20% to 80% is specified as 1.5 ns. Using this rise time and 3 pF per fan out load, calculated minimum line lengths for G-10 epoxy microstrip are listed in *Figure 5-10.* Similar line lengths for epoxy stripline are tabulated in *Figure 5-11.* For other combinations of rise time, impedance, fan out or line characteristics (δ and C_0), maximum lengths are calculated using *Equation 5-14.*

A load capacitance concentrated at the end of the line restricts line length more than a distributed load does. Maximum recommended lengths for fiberglass epoxy dielectric and a 1.5 ns rise time are listed in *Figure 5-12* for microstrip and in *Figure 5-13* for stripline. For line impedances not listed, linear interpolation can be used to determine appropriate line legnths. Appropriate line lengths for dielectric materials with a different propagation constant δ can be determined by multiplying the listed values by the fiberglass epoxy δ and then dividing by the δ of the other material. For example, a line length for a material which has a microstrip δ of 0.1 ns/in. is determined by multiplying the length given in the microstrip table (for a desired impedance and load) by 0.148 and dividing by 0.1.

When using F100K subnanosecond ECL, a 0.5 ns rise time must be considered in any calculation for unterminated lines. The maximum worst-case line length for unterminated Micro Strip when using F100K is given in *Figure 5-14*. In this figure the cases for fanouts of 6 and 8 have not been considered and it is not reasonable to expect that a fanout of six is possible within less than one inch. It should be noted, however, that with the buffered F100K inputs each appearing as a fanout of one, that a fanout condition of four could represent an effective fanout of 20.

The case described in *Figure 5-14* is the only one calculated since all others are approximately the same. The minimum rise time of 0.5 ns was used for the calculation in *Figure 5-14*. Unlike F10K where the minimum rise time of 1.5 ns is frequently observed, the minimum rise time is seldom observed in F100K. Therefore, for most applications a minimum rise time of 0.7 ns is reasonable to some, and if used allows unterminated microstrip lines to be approximately 50% longer than those given in *Figure 5-14*.

Z_0	Number of Fan Out Loads				
	2	3	4	6	8
50	4.15*	3.75	3.45	2.85	2.45
62	3.95	3.50	3.15	2.55	2.10
75	3.75	3.25	2.85	2.25	1.85
90	3.55	3.00	2.60	2.00	1.60
100	3.45	2.85	2.45	1.85	1.45

*length in inches.
Unit load = 3 pF; δ = 0.148 ns/in., distributed loading.

Fig. 5-10 Maximum Worst-case Line Lengths for Unterminated Microstrip for F10K, F95K.

Z_0	Number of Fan Out Loads				
	2	3	4	6	8
50	3.30*	3.00	2.70	2.25	1.90
62	3.15	2.80	2.50	2.00	1.65
75	3.00	2.60	2.25	1.80	1.45
90	2.80	2.40	2.05	1.55	1.25

*length in inches
Unit load = 3 pF; δ = 0.188 ns/in., distributed loading.

Fig. 5-11 Maximum Worst-case Line Lengths for Unterminated Stripline for F10K, F95K.

Z_0	Number of Fan Out Loads				
	1	2	4	6	8
50	4.40*	3.65	2.60	1.90	1.40
62	4.30	3.45	2.30	1.60	1.15
75	4.20	3.20	2.05	1.40	0.95
90	4.05	2.95	1.75	1.05	0.65
100	3.90	2.80	1.60	0.90	0.50

*length in inches.
Unit load = 3 pF; δ = 0.148 ns/in., concentrated loading.

Fig. 5-12 Maximum Worst-case Line Lengths for Unterminated Microstrip for F10K, F95K.

Z_0	Number of Fan Out Loads				
	1	2	4	6	8
50	3.45*	2.85	2.00	1.50	1.10
62	3.40	2.70	1.80	1.30	0.90
75	3.30	2.55	1.60	1.10	0.75
90	3.15	2.35	1.40	0.85	0.50
100	3.10	2.20	1.25	0.70	0.40

*length in inches.
Unit load = 3 pF; δ = 0.188 ns/in., concentrated loading

Fig. 5-13 Maximum Worst-case Line Lengths for Unterminated Stripline for F10K, F95K.

Resistor R_E must provide the current for the negative-going signal at the driver output. The relationships are similar to those for series termination. Line input and output waveforms are noticeably affected if R_E is too large, as shown in *Figure 5-9b*. The negative-going edge of the signal falls in stair-step fashion, with three distinct steps visible at point A. The waveform at point B shows a step in the middle of the negative-going swing. The effect of different R_E values on the net propagation time through the line and the driven loads is evident in *Figure 5-9c* which shows the output signal of one driven gate in a multiple exposure photograph. The horizontal sweep (time axis) was held constant with respect to the input signal of the driver. The earliest of the three output signals occurs with an R_E value of 330 Ω. Changing R_E to 510 Ω increases the net propagation delay by 0.3 ns, the horizontal offset between the first and second signals. Changing R_E to 1 k Ω produces a much greater increase in net propagation delay, indicating that the negative-going signal at B contains several steps. In practice, a satisfactory negative-going signal results when the R_E value is chosen to give an initial negative-going step of 0.6 V at the driving end of the line. This gives an upper limit on the value of R_E, as follows.

$$\text{initial step} = \Delta I \bullet Z_0 = \frac{(V_{OH} - V_{EE})\, Z_0}{R_E + Z_0} \geq 0.6$$

$$R_E = \leq 6.25\, Z_0 \qquad (5\text{-}15)$$

An ECL output can drive two or more unterminated lines, provided each line length and loading combination is within the recommended constraints. The appropriate R_E value is determined from *Equation 5-15*, using the parallel impedance of the two or more lines for Z_0.

An ECL output can simultaneously drive terminated and unterminated lines, although the negative-going edge of the signal shows two or more distinct steps when the stubs are long unless some extra pull-down current is provided. *Figure 5-15a* shows an ECL circuit driving a parallel terminated line, with provision for connecting two worst-case unterminated lines to the driver output. Waveforms at the termination resistor (point A) are shown in the multiple exposure photograph of *Figure 5-15b*. The upper trace shows a normal signal without stubs connected to the driver. The middle trace shows the effect of connecting one stub to the driver. The step in the negative-going edge indicates that the quiescent I_{OH} current through R_T is not sufficient to cause a full signal for both lines. The relationship between the quiescent I_{OH} current (through R_T) and the negative-going signal swing was discussed earlier in connection with parallel termination.

Number of Fanout Loads

20	1	2	4
50	1.37*	1.13	0.95
62	1.33	1.07	0.87
75	1.25	0.95	0.75
90	1.18	0.85	0.52
100	1.15	0.82	0.49

*Length in inches

Unit load = 2 pF, δ = 0.148 ns/inch, distributed load

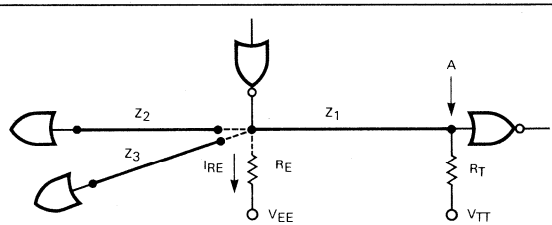
Figure 5-14 Maximum Worst-Case Line Lengths for Unterminated Microstrip - F100K

The bottom trace in *Figure 5-15b* shows the effect of connecting two stubs to the driver output. The steps in the trailing edge are smaller and more pronounced. The deteriorated trailing edge of either the middle or lower waveform increases the switching time of the circuit connected to point A. If this extra delay cannot be tolerated, additional pull-down current must be provided. One method uses a resistor to V_{EE} as suggested in *Figure 5-15a*. The initial negative-going step at point A should be about 0.7 to insure a good fall rate through the threshold region of the driven gate. The initial step at the driver output should also be 0.7 V. If the driver output is treated as a switch that opens to initiate the negative-going signal, the equivalent circuit of *Figure 5-15c* can be used to determine the initial voltage step at the driver output (point X). The value of the current source I_{RT} is the quiescent I_{OH} current through R_T. Using Z to denote the parallel impedance of the transmission lines and Δ V for the desired voltage step at X, the appropriate value of R_E can be determined from the following equation, using absolute values to avoid polarity confusion.

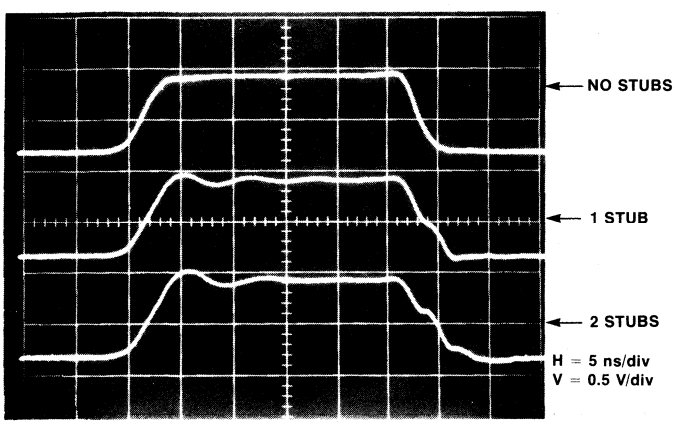
$$R_E = (|V_{EE}| - |V_{OH}| - |\Delta V|) \bullet \left(\frac{Z'}{|\Delta V| - |I_{RT}| Z'} \right) \qquad (5\text{-}16)$$

For a sample calculation, assume that R_T and the line impedances are each 100 Ω, V_{OH} is -0.9 V, ΔV is 0.7 and V_{TT} is -2 V. I_{RT} is thus 11 mA and the calculated value of R_E is 366 Ω. In practice, this value is on the conservative side and can be increased to the next larger (10%) standard value with no appreciable sacrifice in propagation through the gate at point A.

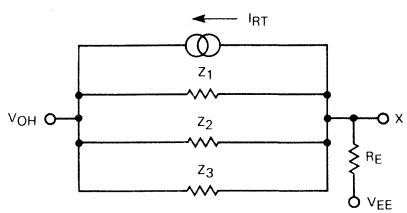
Again, the foregoing example is based on worst-case stub lengths (the longest permissible). with shorter stubs, the effects are less pronounced and a point is reached where extra pull-down current is not required because the reflection from the end of the stub arrives back at the driver while the original signal is still falling. Since the reflection is also negative going, it combines with and reinforces the falling signal at the driver, eliminating the steps. The net result is a smoothly falling signal but with increased fall time compared to the stubless condition.



a. Multiple Lines



b. Waveforms at Termination Point A



c. Equivalent Circuit for Determining Initial Negative Voltage Step at the Driver Output

Fig. 5-15 Driving Terminated and Unterminated Lines in Parallel

The many combinations of line impedance and load make it practically impossible to define just what stub length begins to cause noticeable steps in the falling signal. A rough rule-of-thumb would be to limit the stub length to one-third of the values given in *Figures 5-10, 5-11, 5-12, 5-13, and 5-14.*

DATA BUSSING

Data bussing involves connecting two or more outputs and one or more inputs to the same signal line, *(Figure 5-16)*. Any one of the several drivers can be enabled and can apply data to the line. Load inputs connected to the line thus receive data from the selected source. This method of steering data from place to place simplifies wiring and tends to minimize package count. Only one of the drivers can be enabled at a given time; all other driver outputs must be in the LOW state. Termination resistors matching the line impedance are connected to both ends of the line to prevent reflections. For calculating the modified delay of the line (Chapter 4) the capacitance of a LOW (unselected) driver output should be taken as 2 pF.

An output driving the line sees an impedance equal to half the line impedance. Similarly, the quiescent I_{OH} current is higher than with a single termination. For line impedance less than 100 Ω, the I_{OH} current is greater than the data sheet test value, with a consequent reduction of HIGH state noise margin. This loss can be eliminated if necessary by using multiple output gates (10110, 10111, 95110, 95111, 100112) and paralleling two outputs for each driver. In the quiescent LOW state, termination current is shared among all the output transistors on the line. This sharing makes V_{OL} more positive than if only one output were conducting all of the current. For example, a 100 Ω line terminated at both ends represents a net 50 Ω dc load, which is the same as the data sheet condition for V_{OL}. If one worst-case output were conducting all the current, the V_{OL} would be −1.65 V. If another output with identical dc characteristics shares the load current equally the V_{OL} level shifts upward by about 25 mV. Connecting two additional outputs for a total of four with the same characteristics shifts V_{OL} upward another 22 mV. Connecting four more identical outputs shifts V_{OL} upward another 20 mV. Thus the V_{OL} shift for eight outputs having identical worst-case V_{OL} characteristics is approximately 67 mV. In practice, the probability of having eight circuits with worst-case V_{OL} characteristics is quite low. The output with the highest V_{OL} tends to conduct most of the current. This limits the upward shift to much less than the theoretical worst-case value. In addition, the LOW state noise margin is specified greater than the HIGH state margin to allow for V_{OL} shift when outputs are paralleled.

In some instances a single termination is satisfactory for a data bus, provided certain conditions are fulfilled. The single termination is connected in the middle of the line. This requires that for each half of the line, from the termination to the end, the line length and loading must comply with the same restrictions as unterminated lines to limit overshoot and undershoot to acceptable levels. The termination should be connected as near as possible to the electrical mid-point of the line, in terms of the modified line delay from the termination to either end. Another restriction is that the time between successive transitions, *i.e.*, the nominal bit time, should not be less than 15 ns. This allows time for the major reflections to damp out and limits additive reflections to a minor level.

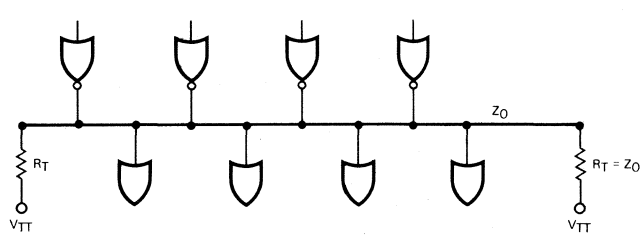


Fig. 5-16 Data Bus or Party Line

WIRED-OR

In general purpose wired-OR logic connections, where two or more driver outputs are expected to be in the HIGH state simultaneously, it is important to minimize the line length between the participating driver outputs, and to place the termination as close as possible to the mid-point between the two most widely separated sources. This minimizes the negative-going disturbances which occur when one HIGH output turns off while other outputs remain HIGH. The driver output going off represents a sudden decrease in line current, which in turn generates a negative-going voltage on the line. A finite time is required for the other driver outputs (quiescently HIGH) to supply the extra current. The net result is a "V" shaped negative glitch whose amplitude and duration depend on three factors; current that the off-going output was conducting, the line impedance, and the line length between outputs. If the separation between outputs is kept within about one inch, the transient will not propagate through the driven load circuits.

If a wired-OR connection cannot be short, it may be necessary to design the logic so that the signal on the line is not sampled for some time after the normal propagation delay (output going negative) of the element being switched. Normal propagation delay is defined as the case where the element being switched is the only one on the line in the HIGH state, resulting in the line going LOW when the element switches. In this case, the propagation delay is measured from the 50% point on the input signal of the off-going element to the 50% point of the signal at the input farthest away from the output being switched. The extra waiting time required in the case of a severe negative glitch is, in a worst-case physical arrangement, twice the line delay between the off-going output and the nearest quiescently HIGH output, plus 2 ns.

An idea of how the extra waiting time varies with physical arrangement can be obtained by qualitatively comparing the signal paths in *Figure 5-17*. With the outputs at A and B quiescently HIGH, the duration of the transient observed at C is longer if B is the off-going output than if A is the off-going element. This is because the negative-going voltage generated at B must travel to A, whereupon the corrective signal is generated, which subsequently propagates back toward C. Thus the corrective signal lags behind the initial transient, as observed at C, by twice the line delay between A and B. On the other hand, if the output at A generates the negative-going transient, the corrective response starts when the transient reaches point B. Consequently, the transient duration observed at C is shorter by twice the line delay from A to B.

BACKPLANE INTERCONNECTIONS

Several types of interconnections can be used to transmit a signal between logic boards. The factors to be considered when selecting a particular interconnection for a given application are cost, impedance discontinuities, predictability of propagation delay, noise environment and bandwidth. Single-ended transmission over an ordinary wire is the most economical but has the least predictable impedance and propagation delay. At the opposite end of the scale, coaxial cable is the most costly but has the best electrical characteristics. Twisted pair and similar parallel wire interconnection cost and quality fall in between.

For single-wire transmission through the backplane, a ground plane or ground screen (Chapter 6) should be provided to establish a controlled impedance. A wire over a ground plane or screen has a typical impedance of 150 Ω with variations on the order of ±33%, depending primarily on the distance from ground and the configuration of the ground. *Figure 5-18* illustrates the effects of impedance variations

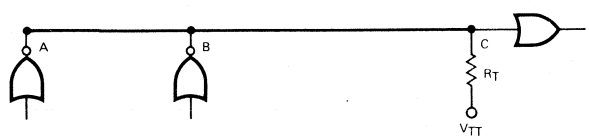
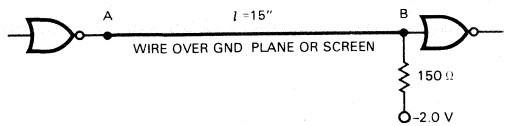


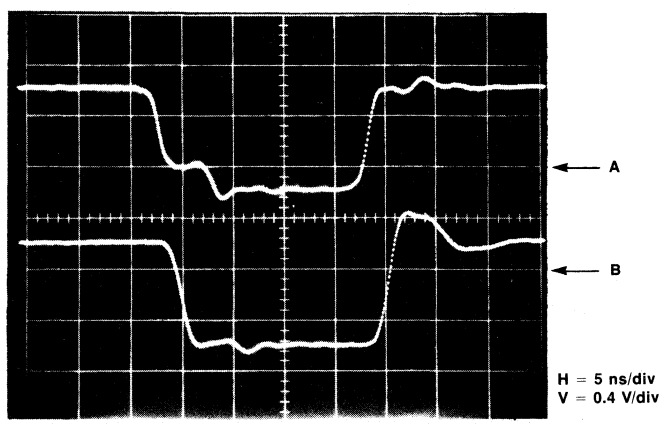
Fig. 5-17 Relative to Wired-OR Propagation

with a 15-inch wire parallel terminated with 150 Ω to −2 V. *Figure 5-18b* shows source and receiver waveforms when the wire is in contact with a continuous ground plane. The negative-going signal at the source shows an initial step of only 80% of a full signal swing. This occurs because the quiescent HIGH state current I_{OH} (about 7 mA) multiplied by the impedance of the wire (approximately 90 Ω) is less than the normal signal swing, and this condition allows the driver emitter follower to turn off. The negative-going signal at the receiving end is greater by 25% ($1 + \rho = 1.25$). The receiving end mismatch causes a negative-going reflection which returns to the source and establishes the V_{OL} level. The positive-going signal at the source shows a normal signal swing, with the receiving end exhibiting approximately 25% overshoot.

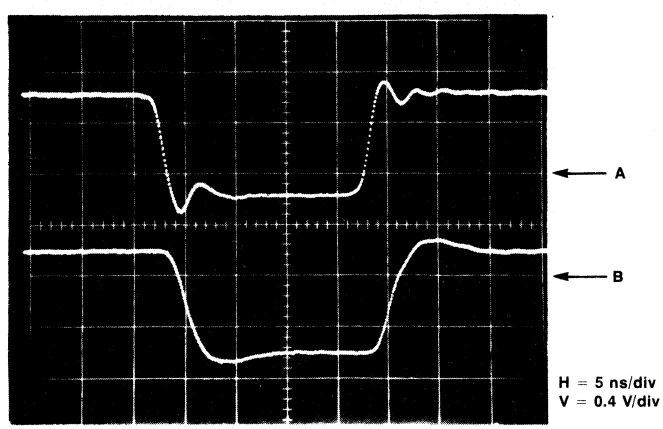
Figure 5-18c shows waveforms for a similar arrangement, but with the wire about 1/8 inch from a ground screen. The impedance of the wire is greater than the 150 Ω termination, but small variations in impedance along the wire cause intermediate reflections which tend to lengthen the rise and fall times of the signal. As a result, the received signal does not exhibit pronounced changes in slope as would be expected if a 200 Ω constant impedance line were terminated with 150 Ω.



a. Wire over Ground Plane or Screen



b. Wire in Contact with Ground Plane

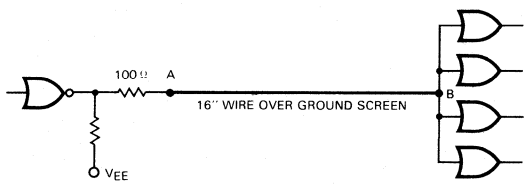


c. Wire Spaced 1/8" from Ground Screen

Fig. 5-18 Parallel Terminated Backplane Wire

Series source resistance can also be used with single wire interconnections to absorb reflections. *Figure 5-19* shows a 16-inch wire with a ground screen driven through a source resistance of 100 Ω. The waveforms show that although reflections are generated, they are largely absorbed by the series resistor, and the signal received at the load exhibits only slight changes and overshoot. Series termination techniques can also be used when the signal into the wire comes from a PC board transmission line. *Figure 5-20a* illustrates a 12-inch wire over a ground screen, with 12-inch microstrip lines at either end of the wire. The output is heavily loaded (fan out of 8) and the combination of impedances produces a variety of reflections at the input to the first microstrip line, shown in the upper trace of *Figure 5-20b*. The lower trace shows the final output; a comparison between the two traces shows the effectiveness of damping in maintaining an acceptable signal at the output. *Figure 5-20c* shows the signals at the input to the driving gate and at the output of the load gate, with a net through-put time of 8.5 ns. The circuit in *Figure 5-20a* is a case of mismatched transmission lines, discussed in Chapter 4.

Signal propagation along a single wire tends to be fast because the dielectric medium is mostly air. However, impedance variations along a wire cause intermediate reflections which tend to increase rise and fall times, effectively increasing propagation delay. Effective propagation delays are in the range of 1.5 to 2.0 ns per foot of wire. Load capacitance at the receiving end also increases rise and fall times (Chapter 4) further increasing the effective propagation delay.



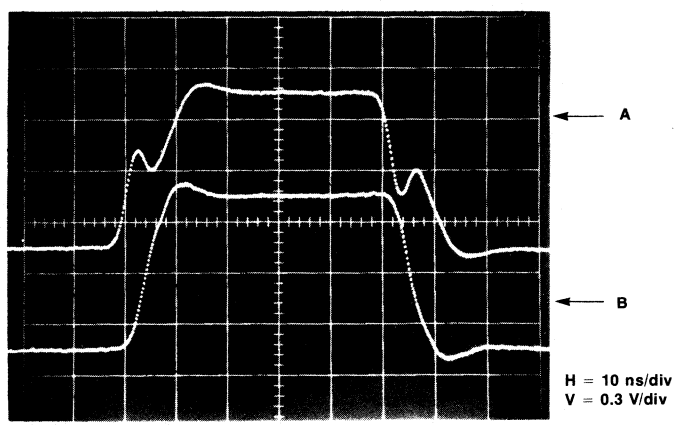
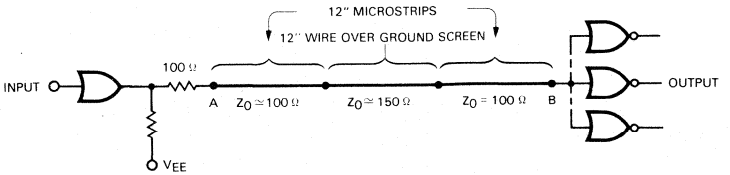
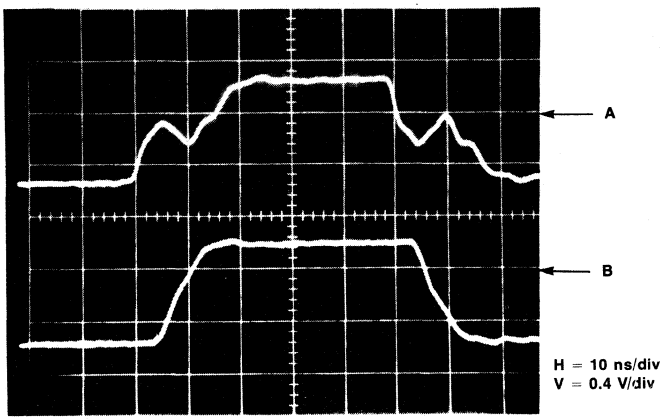


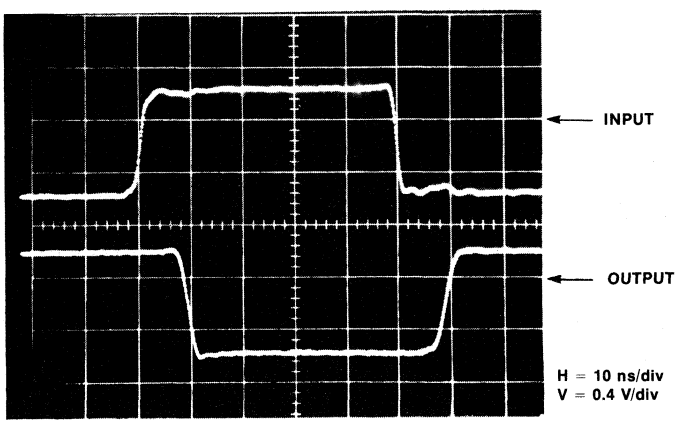
Fig. 5-19 Series Terminated Backplane Wire



a. Backplane Wire Interconnecting PC Board Lines



b. Signals into the First Microstrip and at the Loads



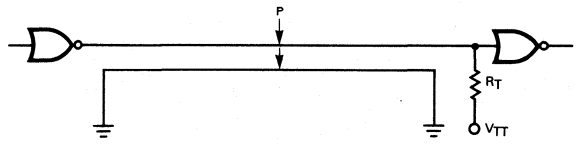
c. Input to Driving Gate and Output of Load Gate

Fig. 5-20 Signal Path with Sequence of Microstrip, Wire, Microstrip

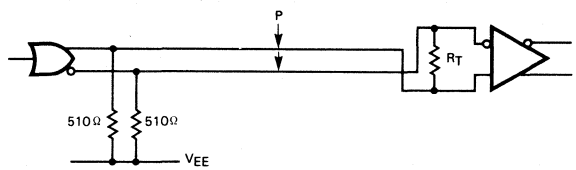
Better control of line impedance and faster propagation can be achieved with a twisted pair. A twisted pair of AWG 26 Teflon* insulated wires, two twists per inch, exhibits a propagation delay of 1.33 ns/ft and an impedance of 115 Ω. Twisted pair lines are available in a variety of sizes, impedances and multiple-pair cables. *Figure 5-21a* illustrates single-ended driving and receiving. In addition to improved propagation velocity, the magnetic fields of the two conductors tend to cancel, minimizing noise coupled into adjacent wiring.

Differential line driving and receiving with a complementary gate as the driver and an F95116 or F10116 line receiver is illustrated in *Figure 21b.* Differential operation provides high noise immunity, since common mode input voltage between −0.55 V and −3.0 are rejected. The differential mode is recommended for communication between different parts of a system, because it effectively nullifies ground voltage differences. For long runs between cabinets or near high power transients, shielded twisted pair is recommended.

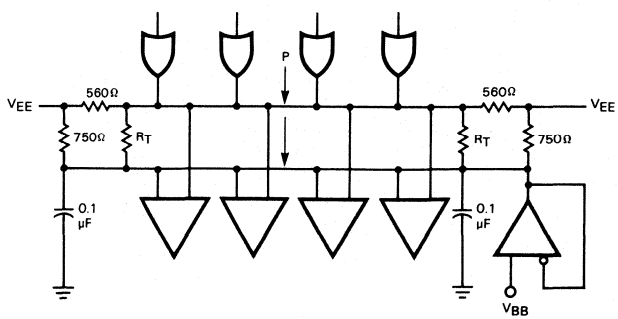
Twisted pair lines can be used to implement party line type data transfer in the backplane, as indicated in *Figure 21c.* Only one driver should be enabled at a given time; the other outputs must be in the V_{OL} state. The V_{BB} reference voltage is available on lead 9 or lead 11 of the quad and triple line receivers, respectively.



a. Single-Ended Twisted Pair



b. Differential Transmission Reception

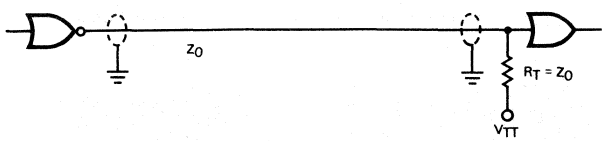


c. Backplane Data Bus

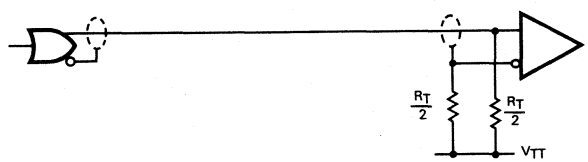
Fig. 5-21 Twisted Pair Connections

In the differential mode, a twisted pair can send high frequency symmetrical signals, such as clock pulses, of 100 MHz over distances of 50 to 100 feet. For random data, however, bit rate capability is reduced by a factor of four or five due to line rise time effects on time jitter.[3]

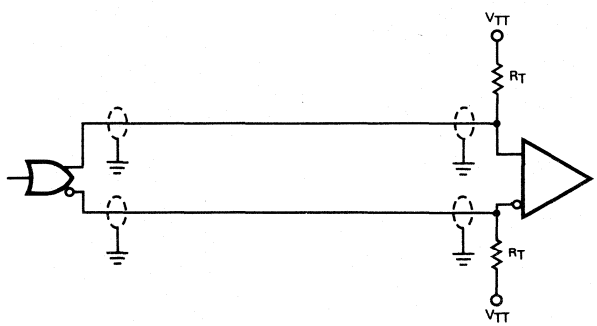
Coaxial cable offers the highest frequency capability. In addition, the outer conductor acts as a shield against noise, while the uniformity of characteristics simplifies the task of matching time delays between different parts of the system. In the single-ended mode, *Figure 5-22a,* 50 MHz signals can be transferred over distances of 100 feet. For 100 MHz operation, lengths should be 50 feet or less. In the differential mode, *Figures 5-22b,c,* the line receiver can recover smaller signals, allowing 100 MHz signals to be transferred up to 100 feet. The dual cable arrangement of *Figure 5-22c* provides maximum noise immunity. The delay of coaxial cables depends on the type of dielectric material, with typical delays of 1.52 ns/ft for polyethylene and 1.36 ns/ft for cellular polyethylene.



a. Single-Ended Coaxial Transmission



b. Differential Coaxial Transmission



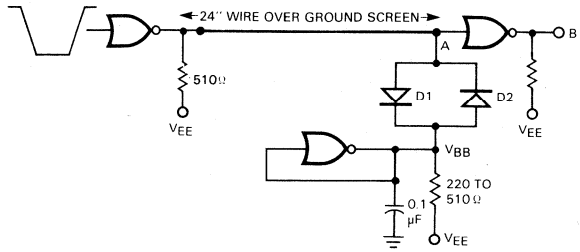
c. Differential Transmission with Grounded Shields

Fig. 5-22 Coaxial Cable Connections

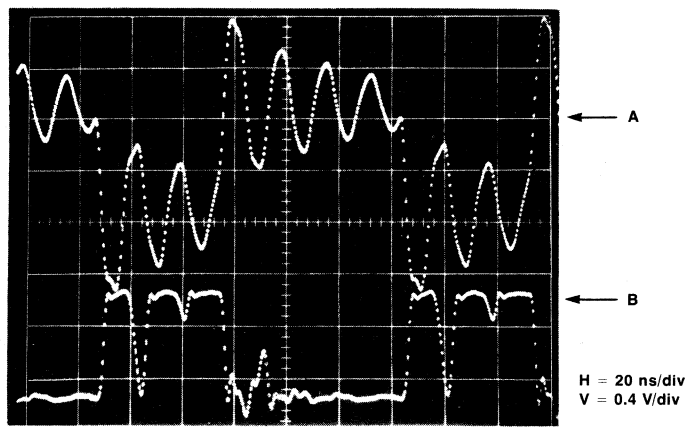
*Teflon is a registered trademark of E. I. du Pont de Nemours Company

SCHOTTKY DIODE CLAMPING

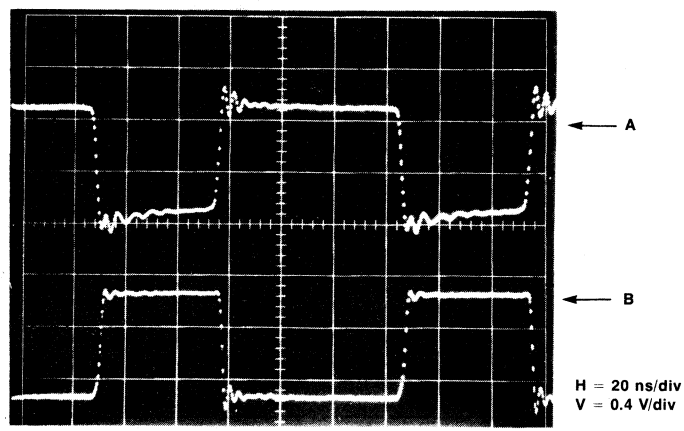
One method of minimizing ringing at the end of a line involves the use of clamping diodes to limit overshoot, *(Figure 5-23).* Two diodes are required to limit overshoot on both the positive-going and negative-going edges of the signal. In theory, any type of high speed switching diode could be used, provided each diode is returned to an appropriate reference voltage. Schottky diode forward characteristics (Figure 5-24)



a. Wire over Ground Screen



b. Without Clamp Diodes



c. With Clamp Diodes

Fig. 5-23 Limiting Ringing by Clamp Diode Termination

allow both diodes of a clamping pair to return to the same reference voltage. The required reference voltage is the average of V_{OH} and V_{OL}, which is V_{BB}. This voltage is readily obtained from any ECL gate by connecting its input and output together, since the only voltage which will satisfy both the input and output is the internal reference voltage V_{BB}. In this input-to-output connection, good RF wiring practice and a bypass capacitor are required to establish current flow in the output transistor and to sink the steady state current (approximately 1 mA) from D1 when the signal is at the V_{OH} level. A resistor value in the range of 220 to 510 Ω is normally required. If the V_{BB} source is at a distance from the diodes, a bypass capacitor is required at the reference end of the diodes to absorb the transient currents.

The effectiveness of clamping diode termination can be judged by the waveforms in *Figure 5-23*. Without the diodes, ringing at the input and the effect on the output of the load gate were severe, *(Figure 5-22b)*. With the diodes connected, changes in line current are absorbed by the diodes and ringing is controlled.

REFERENCES

1. Kaupp, H. R., "Characteristics of Microstrip Transmission Lines," IEEE Transaction on Electronic Computers, Vol. EC-16 (April, 1967).

2. Harper, C. A., Handbook of Wiring, Cabling and Interconnections for Electronics. New York: McGraw-Hill, 1972.

3. True, K. M., "Transmission Line Interface Elements," The TTL Applications Handbook, Chapter 14 (AUGUST, 1973), pp. 14-1 — 14-14.

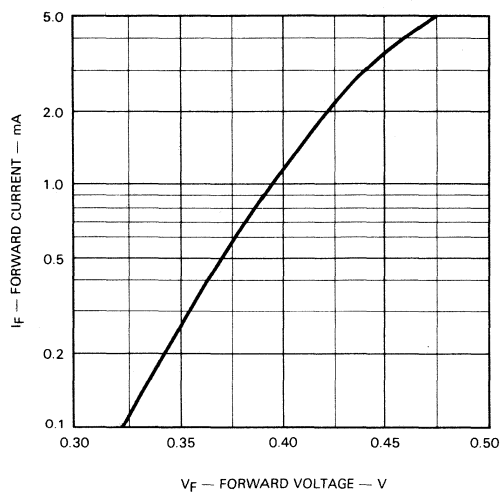
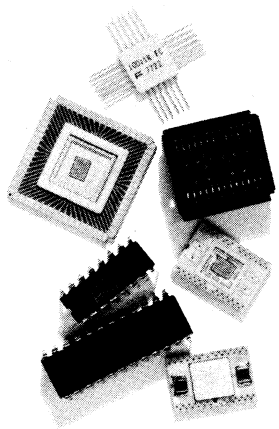


Fig. 5-24 Typical Schottky Diode Forward Characteristics



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F95K SERIES DATA SHEETS 8

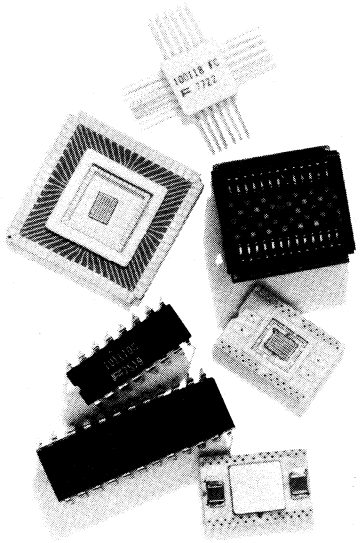
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CHAPTER 6

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- Temperature Coefficient
- Distribution Impedance
- Ground on PC Cards
- Backplane Signal Ground
- Termination Supply V_{TT}
- V_{EE} Supply
- Thermal Considerations
- Reference

Chapter 6
POWER DISTRIBUTION AND THERMAL CONSIDERATIONS

INTRODUCTION

High speed circuits generally consume more power than similar low speed counterparts. At the system level, this means that the supply distribution system must handle a greater magnitude of current flow, while the larger heat load places greater demands on the cooling system. Direct current voltage drops along ground busses affect noise margins for all types of ECL circuits. Voltage drops along V_{EE} busses have only a slight effect on F10K, F95K, and F100K circuits, but they require careful consideration with conventional 10,000 series ECL. Similarly, temperature gradients are not of concern with F95 and F100K circuits, but with F10K or conventional 10,000 circuits, they degrade noise margins for single-ended interconnections.

LOGIC CIRCUIT GROUND, V_{CC}

The positive potential V_{CC} in ECL circuits is the reference voltage for output voltages and input thresholds and should therefore be the ground potential. When two circuits are connected in a single-ended mode, any difference in ground potentials decreases the noise margins, as discussed in Chapter 2. This effect for TTL/DTL circuits as well as for ECL circuits is illustrated in *Figure 6-1*. The following analysis assumes some average value of current flowing through the distributed resistance along the ground path between two circuits. For the indicated direction of I_G, the shift in ground potential *decreases* the LOW state noise margin of the TTL/DTL circuits and the HIGH state noise margin of the ECL circuits. If I_G is flowing in the opposite direction, it *increases* these noise margins, but *decreases* the noise margins when the drivers are in the opposite state. Tabulations of ground currents in ECL designs must include termination currents as well as operating currents I_{EE}. ECL logic boards which use microstrip or stripline techniques generally have large areas of ground metal. This causes the ground resistance to be quite low and thus minimizes noise margin loss between pairs of circuits on the same board.

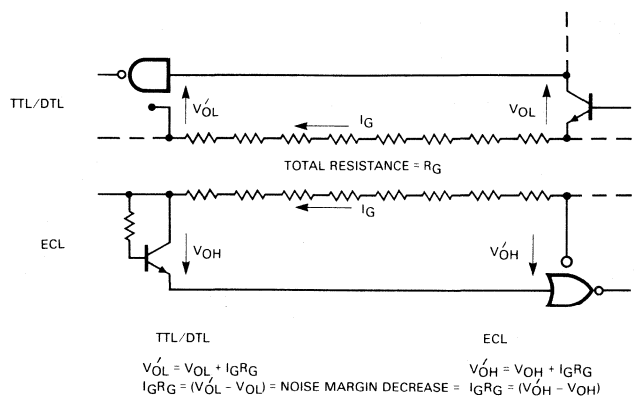


Fig. 6-1 Effect of Ground Resistance on Noise Margins

In practice, two communicating circuits might be located on widely separated PC cards with other PC cards in between. The net resistance then includes the incremental resistance of the ground distribution bus from card to card, while the ground current is successively increased by the contribution from each card. *Figure 6-2* illustrates a distribution bus for a row of cards with incremental resistances along the bus.

The ground shift can be estimated by first determining an average value of current per card based on the number of packages, the mix of SSI and MSI, and the number and types of terminations. With n cards in the row, an average ground current i per card, and an incremental bus resistance r between card positions, the bus voltage drops between the various positions can be determined by proceeding as follows.

between positions 1 and 2: $v_{1\text{-}2} = (n-1)\,ir$

between positions 1 and 3: $v_{1\text{-}3} = (n-1)\,ir + (n-2)\,ir$

between positions 1 and 4: $v_{1\text{-}4} = (n-1)\,ir + (n-2)\,ir + (n-3)\,ir$

between 1 and n:

$$v_{1\text{-}n} = ir\ \{(n-1) + (n-2) + (n-3) + \ldots + [n-(n-1)]\}$$

$$= ir\ [1 + 2 + 3 + \ldots + (n-1)]$$

$$v_{1\text{-}n} = ir \sum_{1}^{n-1} n$$

For a row of 15 cards, for example, the total ground shift between positions 1 and 15 is expressed as in *Equation 6-1.*

$$v_{1\text{-}15} = ir \sum_{1}^{14} n = ir\,(1 + 2 + 3 + \ldots + 13 + 14) = 105\,ir \qquad (6\text{-}1)$$

The ground shift between any two card positions j and k can be determined as follows for the general case.

$$v_{j\text{-}k} = (n-j)ir + [n-(j+1)]ir + [n-(j+2)]ir + \ldots + \{n-[j+(k\text{-}j\text{-}1)]\}\ ir$$

$$= (k-j)nir - ir\ \{j + (j+1) + (j+2) + \ldots + [j+(k\text{-}j\text{-}1)]\} \qquad (6\text{-}2)$$

$$v_{j\text{-}k} = (k-j)nir - ir \sum_{j}^{k-1} n = ir\,[(k-j)n - \sum_{j}^{k-1} n]$$

In a row of 15 cards, the ground shift between positions four and nine, for example, is determined as follows.

$$v_{j\text{-}k} = ir\,[(9-4)15 - (4+5+6+7+8)]$$

$$= ir\,(75-30) = 45\,ir \qquad (6\text{-}3)$$

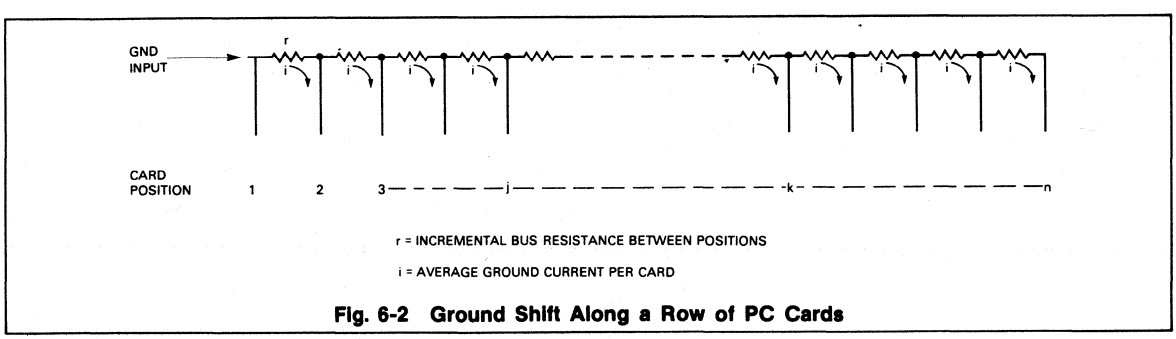


Fig. 6-2 Ground Shift Along a Row of PC Cards

The ground shift between the same number of positions further down the row is less because of the decreasing current along the row. Consider the ground shift between card positions 10 and 15.

$$v_{10\text{-}15} = ir[(15-10)15-(10+11+12+13+14)] = ir(75-60) = 15ir \quad (6\text{-}4)$$

These examples illustrate several principles the designer should consider regarding the ground distribution bus and assignment of card positions. The bus resistance should be kept as low as possible by making the cross sectional areas as large as practical. Logic cards which represent the heaviest current drain should be located nearest the end where ground comes into the row of cards. Cards with single-ended logic wiring between them should be assigned to positions as close together as possible. Conversely, if the ground shift between two card positions represents an unacceptable loss of noise margin, then the differential, *i.e.*, twisted pair, transmission and reception method should be used for logic wiring between them, thereby eliminating ground shift as a noise margin factor.

CONDUCTOR RESISTANCES

Conductors with large cross-sectional areas are required to maintain low voltage drops along power busses. For convenience, *Figure 6-3* lists the resistance per foot and the cross-sectional area for more common sizes of annealed copper wire. Other characteristics and a complete list of sizes can be found in standard wire tables. A useful rule-of-thumb regarding resistances and hence areas is; as gauge numbers increase, resistance doubles with every third gauge number; *e.g.*, the resistance per foot of #10 wire is 1 mΩ; for #13 wire it is 2 mΩ. Similarly, the resistance per foot of #0 wire is 0.078 mΩ, which is half that of #2 wire.

For calculations involving conductors having rectangular cross sections, it is often convenient to work with sheet resistance, particularly for power distribution on PC cards. Copper resistivity is usually given in ohm-centimeters, indicating the resistance between opposing faces of a 1 cm cube. The sheet resistance of a conductor is obtained by dividing the resistivity by the conductor thickness. These relationships appear as follows.

$$\text{Copper resistivity} = \rho = 1.724 \times 10^{-6}\ \Omega - cm\ @\ 20^{\circ}C$$

$$\text{Resistance of a conductor} = \rho\frac{l}{A} = \rho\frac{l}{tw}$$

where: l = length t = thickness w = width

$$\text{Sheet resistance} = \rho_S = \frac{\rho}{t}\ \Omega\ per\ \frac{l}{w}$$

AWG B&S Gauge	Resistance mΩ per foot	Cross-sectional Area square inches
#2	0.156	5.213×10^{-2}
#6	0.395	2.062×10^{-2}
#10	0.999	8.155×10^{-3}
#12	1.588	5.129×10^{-3}
#18	6.385	1.276×10^{-3}
#22	16.14	5.046×10^{-4}
#26	40.81	1.996×10^{-4}
#30	103.2	7.894×10^{-5}

Fig. 6-3 Resistance and Cross-sectional Area of Several Sizes of Annealed Copper Wire

The length/width ratio l/w is dimensionless; therefore the resistance of a length of conductor of uniform thickness can be calculated by first determining the number of "squares", then multiplying by the sheet resistance. For example, a conductor one-eighth inch wide and three inches long has 24 squares; its resistance is 24 times the sheet resistance. Since many thickness dimensions are given in inches, it is convenient to express the resistivity in ohm-inch, as follows.

$$\rho(\Omega\text{-in.}) = \rho(\Omega\text{-cm}) \div 2.54 = 6.788 \times 10^{-7}\ \Omega\text{-in.}$$

The use of sheet resistance and the "squares" concept is illustrated by calculating the resistance of the conductor shown in *Figure 6-4*. Assume the conductor is a 1 oz. copper cladding with a 0.0012 inch minimum thickness on a PC card.

$$\text{Sheet resistance } \rho_S = \frac{\rho}{t} = 5.657 \times 10^{-4}\ \Omega \text{ per square}$$

The number of squares S for the rectangular sections are as follows.

$$S_1 = \frac{l_1}{w_1} = 8 \qquad S_3 = \frac{l_3}{w_2} = 3$$

The middle average segment of the conductor has a trapezoidal shape. The average of w_1 and w_2 can be used as the effective width, within 1% accuracy, if the w_2/w_1 ratio is 1.5 or less. Otherwise, a more exact result is obtained as follows.

$$S_2 = \frac{l_2}{w_2 - w_1} \ln\left(\frac{w_2}{w_1}\right) = 4 \ln 2 = 2.77 \text{ squares} \qquad (6\text{-}5)$$

$$\text{Total } R = R_1 + R_2 + R_3 = \rho_S (S_1 + S_2 + S_3) = 7.51\ m\Omega$$

As another example, assume that a 1 oz. trace must carry a 200 mA current 6 inches with a voltage drop less than 10 mV.

$$R_{max} = \frac{V_{max}}{I} = \frac{0.01}{0.2} = 0.05\ \Omega$$

$$0.05 = \rho_S \frac{l}{w} \qquad (6\text{-}6)$$

$$\frac{w}{l} = 20\ \rho_S$$

$$w = 120\ \rho_S = (120)\ 5.657 \times 10^{-4} = 67.9 \times 10^{-3}$$

$$\therefore \text{minimum trace width, } w = 68 \text{ mils}$$

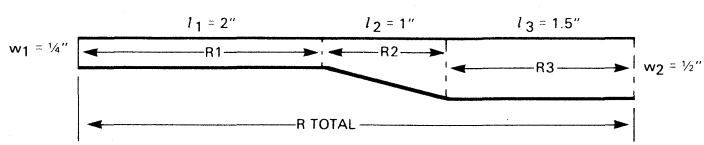


Fig. 6-4 Conductor of Uniform Thickness but Non-uniform Cross-section

At a higher current level, consider the voltage drop in a conductor 20 mils thick, 1.25 inches wide and 3 feet long carrying a 50 A current.

$$\rho_S = \frac{6.788 \times 10^{-7}}{2 \times 10^{-2}} = 3.364 \times 10^{-5}\ \Omega \text{ per square} \qquad (6\text{-}7)$$

$$V = IR = (50)(3.364 \times 10^{-5})\frac{36}{1.25} = 0.0484 = 48.4\ mV$$

Sheet resistances for various copper thicknesses are listed in *Figure 6-5.* Standard thicknesses and tolerances for copper cladding are tabulated in *Figure 6-6* and resistance per foot as a function of width is shown in *Figure 6-7.*

TEMPERATURE COEFFICIENT

The resistances in *Figures 6-3, 6-5,* and *6-7,* as well as those used in the sample calculations, are 20° C values. Since copper resistivity has a temperature coefficient of approximately 0.4%/° C, the resistance at a temperature T can be determined as follows.

$$R_T = R_{20^\circ}\,[1 + 0.004\,(T - 20^\circ)] \qquad (6\text{-}8)$$

At 55° C:

$$R = R_{20^\circ}\,[1 + 0.004\,(55^\circ - 20^\circ)] = 1.14\,R_{20^\circ}$$

Weight or Thickness	Sheet Resistance Ω per square	Thickness	Sheet Resistance Ω per square
2 oz.	2.715×10^{-4}	0.02 in.	3.364×10^{-5}
3 oz.	1.886×10^{-4}	0.05 in.	1.358×10^{-5}
5 oz.	1.077×10^{-4}	1/16 in.	1.086×10^{-5}
0.01 in.	6.788×10^{-5}	1/4 in.	2.715×10^{-6}

Fig. 6-5 Sheet Resistance for Various Thicknesses of Copper

Nominal Thickness		Nominal Weight	Tolerances By	
in.	mm	oz/ft²	weight, %	in.
0.0007	0.0178	1/2	+10	+0.0002
0.0014	0.0355	1	+10	+0.0004 −0.0002
0.0028	0.0715	2	+10	+0.0007 −0.0003
0.0042	0.1065	3	+10	+0.0006
0.0056	0.1432	4	+10	+0.0006
0.0070	0.1780	5	+10	+0.0007
0.0084	0.2130	6	+10	+0.0008
0.0098	0.2460	7	+10	+0.001
0.014	0.3530	10	+10	+0.0014
0.0196	0.4920	14	+10	+0.002

Fig. 6-6 Thicknesses and Tolerances for Copper Cladding

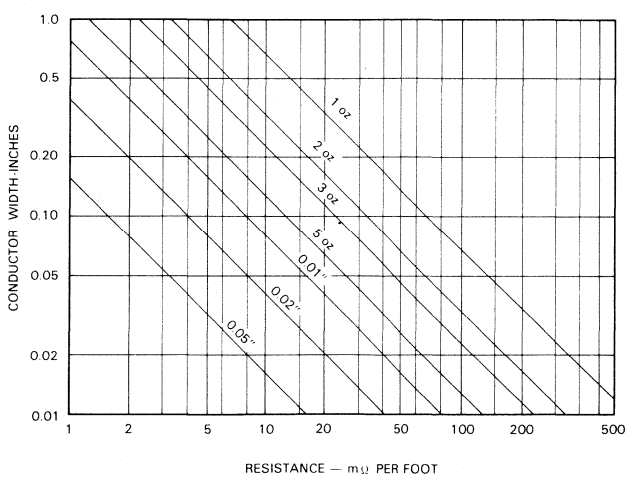


Fig. 6-7 Conductor Resistance Versus Thickness and Width

When specifying power bus dimensions for PC cards containing many IC packages, designers should bear in mind that excessive current densities can cause the copper temperature to rise appreciably. *Figure 6-8* illustrates the ohmic heating effect of various current densities.[1]

DISTRIBUTION IMPEDANCE

Power busses should have low ac impedance, as well as low dc resistance, to prevent propagation of extraneous disturbances along the distribution system. As far as current or voltage changes are concerned, power and ground busses appear as transmission lines; thus their impedances can be affected by shape, spacing and dielectric. The effect of geometry on impedance is illustrated in the two arrangements of *Figure 6-9*. The same cross-sectional area of copper is used, but the two round wires have an impedance of about 75 Ω while the flat conductors have an impedance determined as follows.

$$Z_0 = \frac{377}{\sqrt{\epsilon}} \frac{d}{h} \text{ for } \frac{d}{h} < 0.1$$

With a Mylar* or Teflon* dielectric ($\epsilon = 2.3$) two mils thick, impedance of the flat conductor pair is only 0.5 Ω. Power line impedance can also be reduced by periodically connecting RF type capacitors across the line; this effect is discussed in Chapter 4.

GROUND ON PC CARDS

It is essential to assign one layer of copper cladding almost exclusively to ground. This provides low impedance, non-interfering return paths for the current changes which travel along signal traces when the IC outputs change state. These currents flow from the V_{CC} leads of the IC packages, through the output transistors, then into the loads and the stray capacitances exist from an output to V_{EE}, to ground and to the terminations of other signal lines. Thus, displacement currents through stray capacitances flow in many paths, but must ultimately return through ground to the output transistor where they originated. To reduce the length and impedance of the return path, the ground metal should cover as large an area as possible and one decoupling capacitor should be provided for every four to six IC packages. These capacitors should be ceramic, mica or other RF types in the 0.01 to 0.1 μF range.

The load current returning to an IC package through ground metal is predictable, both in magnitude and in the return path. Since the magnetic and capacitive coupling between a signal trace and the underlying ground provides the transmission line characteristic, it follows that the load current flowing through the signal trace is accompanied by a ground return current equal in magnitude but opposite in direction. For example, a signal change into a 50 Ω line causes about 17 mA current change and, as this current change

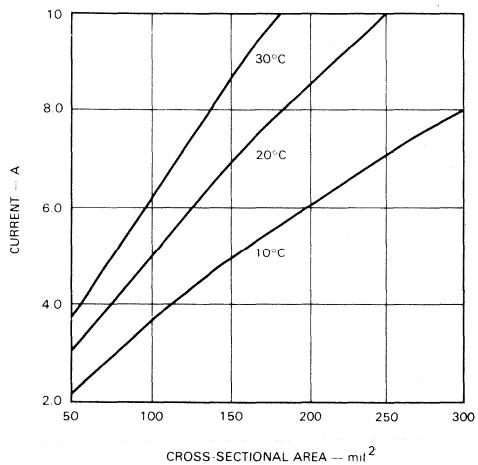


Fig. 6-8 Temperature Rise with Current Density in PC Board Traces

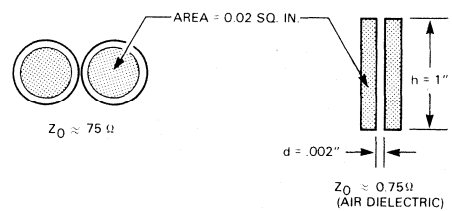


Fig. 6-9 Effect of Geometry on Power Bus Impedance

*Mylar and Teflon are registered trademarks of E.I. du Pont de Nemours Company.

propagates along the signal trace, a current of -17 mA is advancing along the ground directly underneath the signal trace. Therefore, if there is an interruption in the ground, the return current is forced to go around it. When it is necessary to interrupt the ground plane to provide crossover links between V_{EE} distribution lines or signal traces on the other side of the board, the interruptions should be kept as short as possible; every effort should be made to locate them away from overlying signal lines. When the ground plane is interrupted for short signal lines between packages, these lines should be at right angles to signal lines on the other side to minimize coupling. V_{EE} and V_{TT} distribution lines can also act as the return side of transmission lines, as long as decoupling capacitors to ground are placed in the immediate areas where the signal return current must continue through ground.

Several connections along the edge of a PC card should be assigned to ground to accomodate backplane signal ground. These should be spaced at one-half to one inch intervals to minimize the average path length for signal return currents and to simulate a distributed connection to the backplane signal ground.

BACKPLANE SIGNAL GROUND

A ground return path must be provided to control the impedance of single-ended point-to-point signal wiring between connectors in the backplane. If a motherboard is used as the backplane for a row of cards, one side of the motherboard can be a ground plane. Interconnect wires then exhibit an impedance which can be calculated from the wire-over ground formula.

$$Z_0 = \frac{138}{\sqrt{\epsilon}} \quad log \frac{4h}{d} \qquad (6\text{-}9)$$

where d is diameter, h is distance to ground, ϵ is dielectric constant.

For small insulated wire, the impedance ranges from about 75 Ω when lying flat against ground to about 150 Ω when spaced one diameter, including insulation, above ground. With one side of a motherboard committed to ground, the other side can be used to distribute timing signals and dc voltages.

When a motherboard is not practical, a ground screen can be used to establish the backplane signal wiring impedance. A screen is constructed by connecting the grounds of each card connector, as illustrated in *Figure 6-10*. Wires running over a ground screen exhibit an impedance in the range of 100 to 200 Ω, depending on distance from the screen, mesh size and the angular direction. The wires forming the screen provide a means for the signal return current to find a "piece-wise optimum" return path. Thus, the smaller the screen mesh, the more nearly it simulates a ground plane.

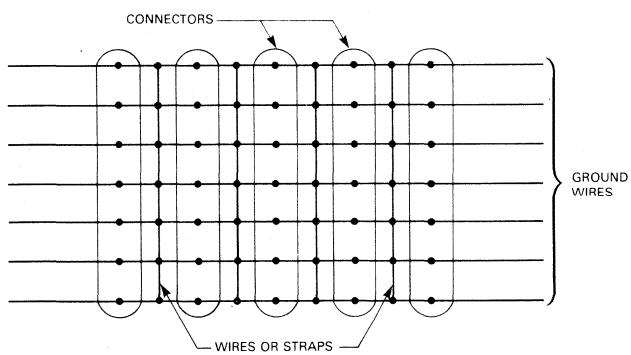


Fig. 6-10 Ground Screen

TERMINATION SUPPLY V_{TT}

A separate return voltage for the termination resistors offers a way to minimize power dissipation in systems extensively using parallel termination techniques. A -2 V V_{TT} value represents an optimum speed/power trade-off, allowing sufficient termination current to discharge load capacitances while minimizing the average power consumption. *Figure 6-11* shows the average values of current, IC power dissipation and resistor power dissipation for various values of the termination resistor R_T returned to -2 V. Average values are determined by calculating the output HIGH and output LOW values, then taking the average. These 50% duty cycle values are useful in determining the current drain on the -2 V supply and the contribution to dissipation on the logic boards. Peak values of termination current are approximately 60% greater than the average values listed.

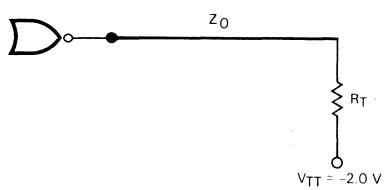
Regulation of the -2 V supply is not critical; a variation of ±5% causes a change in output levels of ±12 mV for 50 Ω terminations or ±7 mV for 100 Ω terminations. If V_{TT} is distributed on a logic board by using etched traces, as opposed to a solid voltage plane, decoupling capacitors to ground should be used to reduce the effective dynamic impedance of the traces. The capacitors should be distributed in about the same pattern as the termination resistors, with 0.01 μF for every four terminations. A 1 to 10 μF decoupling capacitor to ground should be placed on the card near the point where the V_{TT} supply enters from the backplane.

V_{EE} SUPPLY

The value of the V_{EE} voltage is not critical for F95K or F10K ECL, since they operate successfully over the range -4.7 to -6.2 V; simple OR/NOR gate elements operate from -3.7 to -6.2 V. The value of V_{EE} is similarly not critical for F100K since all circuits in the family operate over the range of -4.2 V to -5.7 V. Decoupling capacitors to ground should be used on each card, as previously discussed in connection with the ground on PC cards. In addition, each card should use a 1 to 10 μF decoupling capacitor near the point where V_{EE} enters the card.

The current drain for the V_{EE} supply for each circuit type can be determined from the data sheet specifications. For V_{EE} values other than -5.2 V, the current drain varies as shown in *Figures 6-12* and *6-13* for SSI and MSI elements respectively. The figures also show the variations exhibited by conventional uncompensated 10,000 ECL.

If conventional 10,000 series ECL elements are randomly mixed with F10K circuits in the same system, the more restrictive V_{EE} requirements of the conventional 10,000 series must be observed. It is common practice to limit V_{EE} regulation to the nominal -5.2 V ±2% because the ac and dc parameters exhibit a sensitivity to V_{EE}. Circuit manufacturers recommend that for single-ended signal transmission between two circuits, their respective V_{EE} values should not differ by more than 100 mV, to limit noise margin loss to 30 mV. This loss occurs in the LOW state when the driver circuit V_{EE} is -5.1 V and the receiving circuit V_{EE} is -5.2 V. In this situation, substituting an F10K circuit for the driver reduces the noise margin loss from 30 to 3 mV.



R_T Ω	P_D (avg) mW		I_{avg} mA
	Resistor	IC Output	
50	13	14	14
62	11	12	11
75	9.1	9.5	9.3
90	7.9	8.2	8.1
100	7.1	7.3	7.3
150	5.0	4.9	5.0

Fig. 6-11. Average Current and Power Dissipation for Parallel Termination to -2 V

Series dividers used to obtain Thevenin equivalent parallel terminations increase the current load on the V_{EE} supply, as do the pull down resistors to V_{EE} used with series termination. Average V_{EE} current and resistor dissipation for Thevenin equivalent terminations are listed in *Figure 6-14* for several representative values of equivalent resistance. The average values apply for 50% duty cycle; peak current values are approximately 11% greater. Dissipation in the IC output transistor is the same as in *Figure 6-11*. Average dissipation and I_{EE} current for several values of pull down resistance to V_{EE} are listed in *Figure 6-15*. The R_E values are appropriate for series termination of transmission lines with impedances listed in the Z_0 column, determined from *Equation 5-12*. Peak current values are approximately 12% greater than average values.

Figures 6-11, 14 and *15* show that the Thevenin equivalent parallel termination method leads to 10 times as much dissipation in the resistors as in the single resistor returned to -2 V. Similarly, the dissipation in R_E for series termination is three times the dissipation in the parallel termination resistor to -2 V.

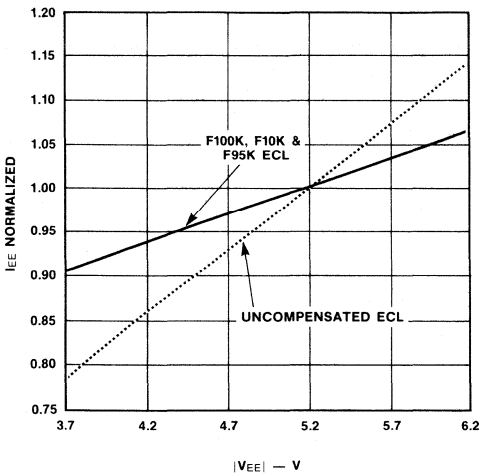


Fig. 6-12. Power Drain Current Versus Supply Voltage for ECL SSI

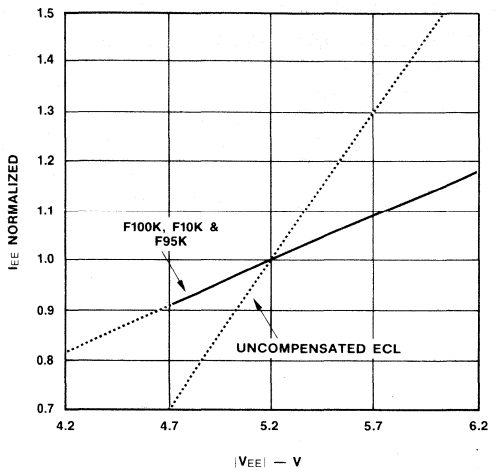
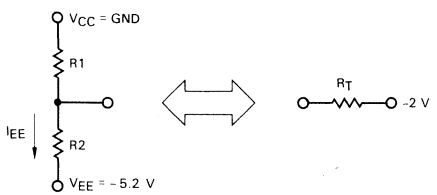
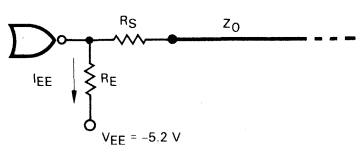


Fig. 6-13. Power Drain Current Versus Supply Voltage of ECL MSI



R_T Ω	R_1 Ω = 1.625 R_T	R_2 Ω = 2.6 R_T	P_D (avg) mW Resistors	I_{EE} (avg) mA
50	81	130	143	30
62	101	161	114	24
75	122	195	94	20
90	146	234	79	17
100	163	260	71	15
150	244	390	47	10

Fig. 6-14. Series Divider for Thevenin Equivalent Terminations



R_E Ω	Z_0 Ω	P_D (avg) mW R_E	P_D (avg) mW IC Output	I_{EE} (avg) mA
330	50	46	15	12
390	62	39	13	10
470	75	32	10	8.2
560	90	28	8.7	7.0
620	100	25	7.8	6.4
1K		16	4.8	4.0

Fig. 6-15. Average Power Dissipation and Current using Pull Down Resistor to V_{EE}

In some applications, it may be advantageous to distribute power in unregulated form and use local regulators on the logic boards. Fairchild 3-terminal regulators (μA78NO5, μA78NO2) are designed specifically for ECL. The μA78NO5 provides -5.2 V and the μA78NO2 provides -2 V; both can operate from the same input voltage.

THERMAL CONSIDERATIONS

F95K and F10K circuits are specified over the standard industrial temperature range, 0° C to +75° C. Operation over a -30° C to +85° C range results in slight degradation of worst case parameter limits. System cooling requirements are based on three considerations. One is the need to minimize temperature gradients between circuits communicating in the single-ended mode. Another concerns controlling the temperature environment of each circuit to assure that the parameters stay within guaranteed limits. The thermal conditions must also insure that the maximum rated junction temperature is not exceeded.

Temperature gradients are of no practical concern with F95K circuits since they are temperature compensated; their output voltage levels and input thresholds change very little with temperature, as discussed in Chapter 2. With F10K and conventional 10,000 circuits, output voltage levels and input thresholds vary with temperature. This causes a loss of noise margin when driver and receiving circuits are operating at different temperatures. Loss of HIGH-state noise margin occurs when the receiving circuit is at the higher temperature, amounting to approximately 1 mV/° C of temperature gradient. When the driver circuit is at the higher temperature, the LOW state margin decreases by approximately 0.5 mV/° C of gradient. The system designer should consider noise margin loss, as well as the effects of ground potential differences and V_{EE} gradients, when deciding whether to use single-ended wiring between two locations or to use differential wiring. Differential line receivers nullify the effects of temperature gradients, as well as V_{EE} gradients and ground voltage differences.

Each parameter limit on the F100K and F95K data sheets applies over the entire 0° C to 75° C temperature range, with either still or moving air. For F10K and conventional 10,000 series, parameter limits have different values for different ambient temperatures. Further, the specifications are based on a minimum air flow rate of 500 linear feet per minute. Thermal equilibrium must be established for incoming test results of F10K circuits to be valid. The time required to attain equilibrium can vary considerably, depending on the internal dissipation of the particular IC type and details of the thermal arrangement. Normally, an adequate waiting time is three to five minutes after power is applied. When an F10K circuit is operating with a cooling air temperature other than data sheet test temperatures, circuit parameter values can be estimated by interpolation. For example, if the cooling air temperature is +50° C, the circuit V_{OH} can be estimated by by averaging the V_{OH} values for +25° C and +75° C.

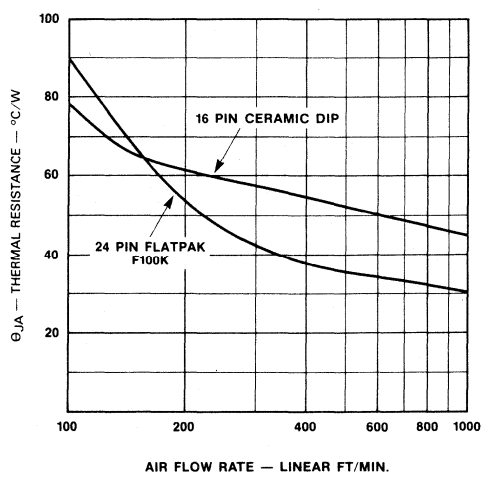


Fig. 6-16. Junction-to-Air Thermal Resistance Versus Air Flow Rate

The maximum rated junction temperature of F100K, F95K and F10K circuits is +150° C. An individual IC junction temperature can be determined by multiplying power dissipation by the junction-to-air thermal resistance θ_{JA} and adding the result to the ambient air temperature. The power dissipation is V_{EE} times I_{EE}, from the data sheet, plus the dissipation in the output transistors from *Figure 6-11* or *6-15*. The thermal resistance for the 16-lead ceramic DIP is shown in *Figure 6-16* as a function of cooling air flow rate. This figure applies when the IC is mounted on a board with the air flowing in a plane parallel to the board and perpendicular to the long axis of the IC package. When air temperature, flow rate and package power dissipation are known, junction temperature is determined as follows.

$$T_J = T_A + P_D\theta_{JA} \tag{6-10}$$

Conversely, when the maximum rated junction temperature (+150° C), the package power dissipation, and the air temperature are known, the minimum flow rate can be determined by first determining the maximum thermal resistance.

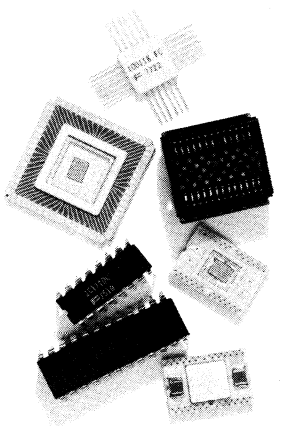
$$Maximum\ \theta_{JA} = \frac{(150^\circ - T_A)}{P_D} \tag{6-11}$$

For this value of θ_{JA} the minimum flow rate is determined from *Figure 6-16*.

When the system designer plans to depend on natural convection for cooling, it is recommended that thermal tests be conducted to determine actual conditions. The effectiveness of natural convection for cooling varies greatly. For instance, on a densely packed logic board in a horizonal attitude in still air, the effective ambient temperature for an IC varies with its position. An IC in the middle of the board is subjected to air that is partially heated by surrounding ICs. Additionally, the temperature of the board rises, due to heat flow through the component leads. These effects can cause a much higher junction temperature than might be expected.

REFERENCE

1. Harper, C.A., Editor, Handbook of Wiring, Cabling and Interconnecting for Electronics, McGraw-Hill, 1972.



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F10K VOLTAGE COMPENSATED ECL SERIES

GENERAL DESCRIPTION — Fairchild F10K Series Emitter Coupled Logic (ECL) circuits are high speed, low power logic elements intended for use in high speed systems such as central processors, memory controllers, peripheral equipment, instrumentation and digital communication systems.

F10,000 ECL is designed to be fully compatible with conventional 10,000 ECL and has the same part numbers, functions, pinouts, temperature behavior, test methods, propagation delay limits and signal voltages.

F10K circuits employ Emitter Coupled Logic to achieve typical power levels of 25 mW/gate. The nominal power supply is specified as V_{EE} equal to -5.2 V. All devices, however, may be operated over V_{EE} ranges of -4.7 to -6.2 V with negligible loss of noise immunity. Some SSI gates may be operated over a V_{EE} range of -3.5 to -6.2 V, again with a negligible loss of noise immunity, due to the built-in voltage regulator.

In accordance with standard IC practice, F10K devices are specified over 0° C to +75° C temperature range. However, limits ensure that the F10K series is fully compatible with other 10,000 devices specified over a -30° C to +85° C ambient temperature range.

High input impedance (typically 50 kΩ) and open outputs allow effective usage of series or parallel terminated line techniques and large numbers of OR-ties.

- **Very high speed . . . typically 2 ns per gate.**
- **Low power dissipation . . . typically 25 mW per gate.**
- **Voltage compensated . . . noise margin insensitive to power supply variations and transients, relaxed power supply requirements.**
- **Internal 50 kΩ (nominal) input pull down resistors . . . unused inputs may be left open.**
- **Open emitter-follower outputs drive terminated lines.**
- **Separate V_{CC} leads eliminate noise coupling.**
- **Single V_{EE} power supply . . . -4.7 to -6.2 V.**
- **Wired-OR capability.**
- **Complementary, simultaneous outputs.**
- **Fully compatible with other 10,000 series ECL.**

RECOMMENDED OPERATING AND TEST CONDITIONS — The Fairchild F10K series is designed to operate in a system whose ambient temperature is controlled by moving air or equivalent means. The ambient temperature may be any value between 0° C and +75° C, but the temperature gradient between the devices must be at a minimum to conserve noise immunity. The Fairchild F10K devices are designed to meet the specified dc characteristics when a thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

The Fairchild F10K series operates with a system power supply V_{EE} between -4.7 and -6.2 V. Detailed test specifications are for nominal V_{EE} = -5.2 V.

ABSOLUTE MAXIMUM RATINGS

(Non-operating, above which useful life may be impaired)

Storage Temperature	-65° C to +150° C
Junction Temperature	+150° C
Supply Voltage V_{EE} (Continuous)	-8 V
Input Voltage	Gnd to V_{EE}
Output Current	-50 mA

FUNCTIONAL DESCRIPTION

F10K offers many high speed system design advantages. High speed is achieved by using small, low capacitance device geometries and operating the transistors between the active and off modes, thereby avoiding saturation. The basic ECL gate is shown in *Figure 1*.

If the input voltages are more negative than V_{BB}, Q1 and Q2 are cut off and Q3 conducts, holding the collector of Q3 LOW. If either input is more positive than V_{BB}, Q1 or Q2 will conduct and Q3 will be cut off, raising its collector voltage. Since one or more transistors are always conducting, there is a constant current drain, independent of frequency which eliminates sharp switching transients and frequency dependent power dissipation effects. The outputs of the circuit are emitter-followers, Q4 and Q5. They provide low impedance drive to terminated lines and voltage shifting to levels compatible with the inputs. The basic gate simultaneously performs the positive logic OR and NOR functions, providing both true and complement outputs within a single gate delay period. The outputs of several gates may be tied to provide a wired-OR function. An external load resistor must be provided in all cases.

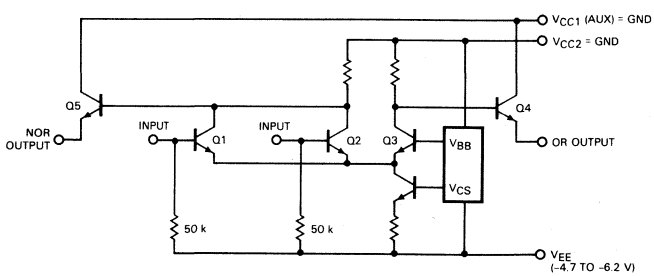
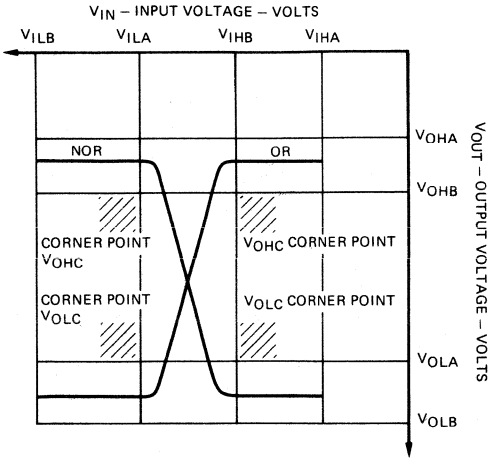


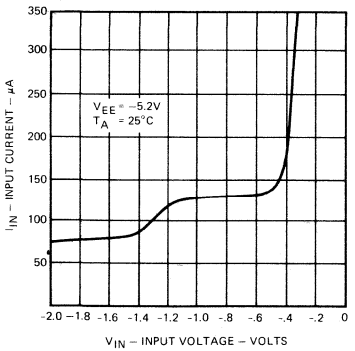
Figure 1

TYPICAL ECL TRANSFER CHARACTERISTICS WITH SPECIFICATION POINTS

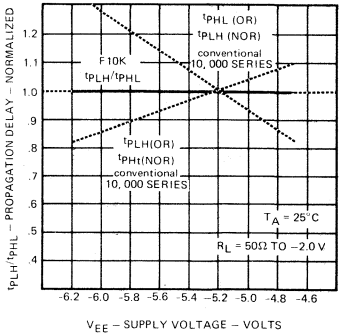


TYPICAL F10K SERIES CHARACTERISTICS

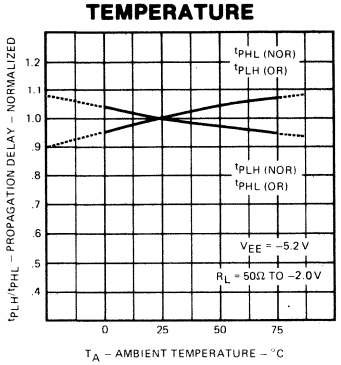
INPUT CHARACTERISTICS



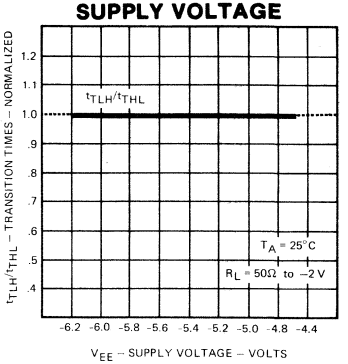
PROPAGATION DELAY VARIATION VERSUS SUPPLY VOLTAGE



TYPICAL PROPAGATION DELAY VERSUS TEMPERATURE



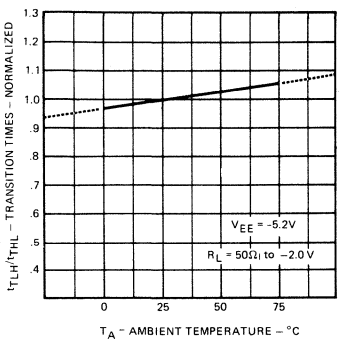
OUTPUT TRANSITION TIME VARIATION VERSUS SUPPLY VOLTAGE



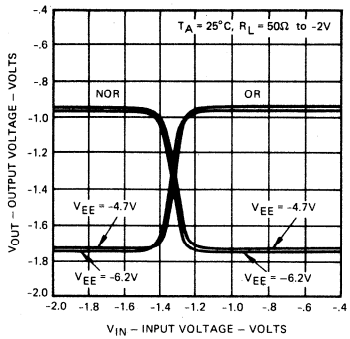
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TYPICAL F10K SERIES CHARACTERISTICS

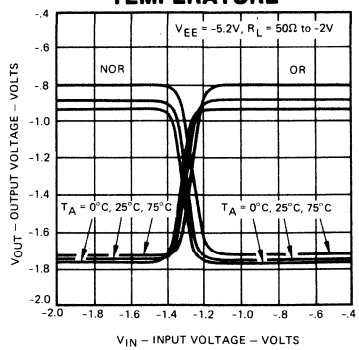
OUTPUT TRANSITION TIME VERSUS TEMPERATURE



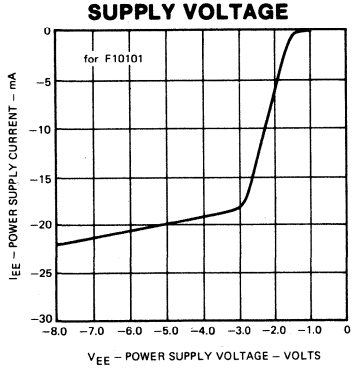
INPUT/OUTPUT TRANSFER CHARACTERISTICS VERSUS SUPPLY VOLTAGE



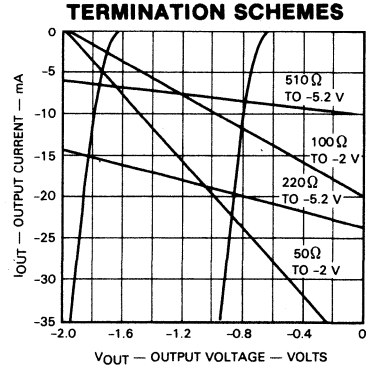
INPUT/OUTPUT TRANSFER CHARACTERISTICS VERSUS TEMPERATURE



CHANGE IN POWER SUPPLY CURRENT WITH RESPECT TO CHANGES IN POWER SUPPLY VOLTAGE



OUTPUT CHARACTERISTICS VERSUS TYPICAL OUTPUT TERMINATION SCHEMES



DC CHARACTERISTICS FOR THE F10K SERIES ECL FAMILY – Parametric Limits listed below are guaranteed for the entire Fairchild ECL Family unless otherwise specified on the individual data sheets.

COMMERCIAL GRADE (0 to 75°C)

DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	−1000 −960 −900		−840 −810 −720	mV	0°C 25°C 75°C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	−1020 −980 −920			mV	0°C 25°C 75°C	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			−1645 −1630 −1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	−1145 −1105 −1045		−840 −810 −720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IL}	Input Current LOW	0.5			μA	25°C	V_{IN} = V_{ILB}	

MILITARY GRADE (−55°C to +125°C)

DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	−1080 −930 −825		−880 −780 −630	mV	-55°C 25°C 125°C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 100 Ω to -2.0 V
V_{OL}	Output Voltage LOW	−1920 −1850 −1820		−1655 −1620 −1545	mV	-55°C 25°C 125°C		
V_{OHC}	Output Voltage HIGH	−1100 −950 −845			mV	-55°C 25°C 125°C	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			−1635 −1600 −1525	mV	-55°C 25°C 125°C		
V_{IH}	Input Voltage HIGH	−1255 −1105 −1000		−830 −720 −580	V	-55°C 25°C 125°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	−1920 −1850 −1820		−1510 −1475 −1400	mV	-55°C 25°C 125°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IL}	Input Current LOW	0.5			μA	25°C	V_{IN} = V_{ILB}	

F10000
4-BIT SHIFT REGISTER

GENERAL DESCRIPTION — The F10000 is a 4-Bit Parallel/Serial In, Parallel/Serial Out Shift Register. High Speed ECL technology permits storage, shifting, counting and serial code conversion at rates in excess of 200 MHz.

Features include assertion outputs for each stage, overriding asynchronous master reset, serial and parallel D type inputs and a gated clock. Availability of these features on one chip significantly improves the reliability, performance, and power consumption of high speed systems.

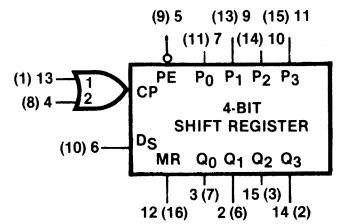
The F10000 incorporates a unique voltage compensation network which ensures that significant parameters such as logic levels, noise margins and speed remain constant over a wide range of power supply voltage.

- **HIGH SPEED . . . 200 MHz TYPICAL SHIFT FREQUENCY**
- **D TYPE INPUTS SERIAL AND PARALLEL**
- **GATED CLOCK INPUT**
- **ASYNCHRONOUS MASTER RESET**
- **TERMINATED LINE DRIVE CAPABILITY**
- **WIRED-OR CAPABILITY**
- **SEPARATE V_{CC} PINS ELIMINATE NOISE COUPLING**
- **50 kΩ INPUT PULL DOWNS . . . UNUSED INPUTS MAY BE LEFT OPEN**
- **SINGLE V_{EE} POWER SUPPLY . . . −4.7 V TO −6.2 V**
- **NOISE MARGINS INSENSITIVE TO POWER SUPPLY VARIATIONS AND GRADIENTS**

PIN NAMES

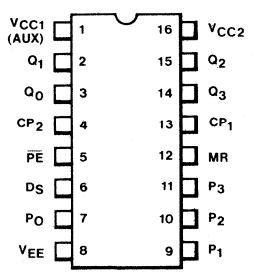
P_n	Parallel Data Inputs
PE	Parallel Enable (Active LOW)
CP_n	Clock In, Shifts on Positive Transition
MR	Asynchronous Master Reset—Active HIGH
D_S	Data Input, Serial
Q_n	Register Outputs

LOGIC SYMBOL

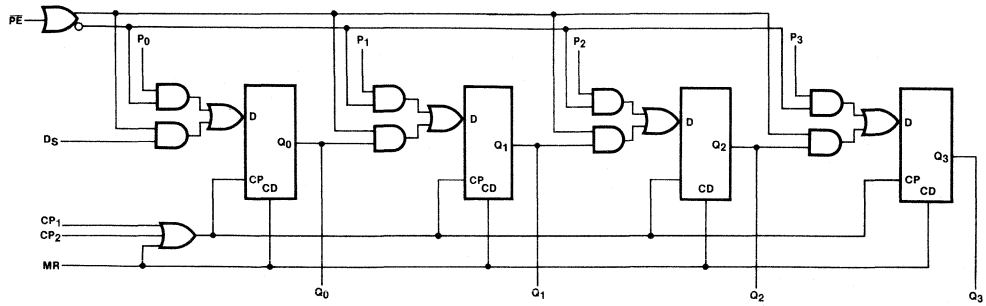


V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

FUNCTIONAL DESCRIPTION — The F10000 is a high-speed 4-Bit Shift Register. It consists of four master/slave flip-flops and four 2-input multiplexers interconnected so as to permit loading of the masters from either a preceding slave output (Q_{n-1}) or an external (P_n) input. The function desired is selected by the Parallel Enable (PE) input.

The masters are loaded during the LOW period of the clock (CP1, 2). As the clock changes from LOW to HIGH, the masters are inhibited from change followed by the enabling of the data path from master to slave. This data is then presented at the outputs (Q_n). While the clock is HIGH, the masters are inhibited from change and the master/slave data path remains open. During the HIGH to LOW transition of the clock, the master/slave data path is inhibited. This is followed by the enabling of the masters for the acceptance of data from the parallel or serial logic inputs.

As the two clock inputs are ORed together, both must be LOW for the masters to accept new data. If either is raised to a HIGH, the register is clocked.

A HIGH on one Clock input can prevent the register from shifting, providing a hold condition. To prevent false triggering, this input must change from LOW to HIGH while the clock is HIGH.

The Master Reset (MR) function is asynchronous. When held HIGH, it overrides all other commands and forces all outputs (Q_n) LOW.

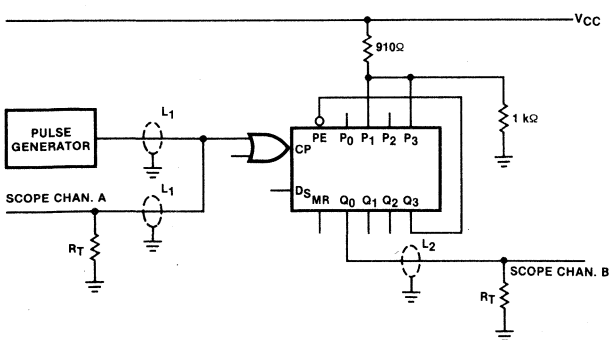
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

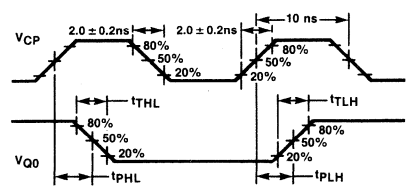
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH MR (Pin 12)			260 700	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−85	−66		mA	25°C	Outputs Open, Pin 4 or 13 Tied to V_{IH}

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
f_{count}	Shift Right Frequency	150	200		MHz	See Figure 3
t_{PLH}	Propagation Delay Clock to Output	2.0	3.2	5.0	ns	See Figure 1
t_{PHL}	Propagation Delay Clock to Output	2.0	3.2	5.0	ns	
t_{PHL}	Propagation Delay Master Reset to Output		2.5		ns	See Figure 2
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.3	2.0	3.5	ns	See Figure 1
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.3	2.0	3.5	ns	
t_w	Clock Pulse Width		2.5		ns	See Figure 3
t_w	MR Pulse Width		3.5		ns	
t_s	Set-Up Time Prior to Clock D_S to CP, P_n to CP	1.5	0.5		ns	
t_h	Hold Time After Clock D_S to CP, P_n to CP	1.0	−0.5		ns	
t_s	Set-Up Time Prior to Clock PE to CP	5.4	3.2		ns	
t_h	Hold Time After Clock PE to CP	0	−3.2		ns	

SWITCHING CIRCUITS AND WAVEFORMS

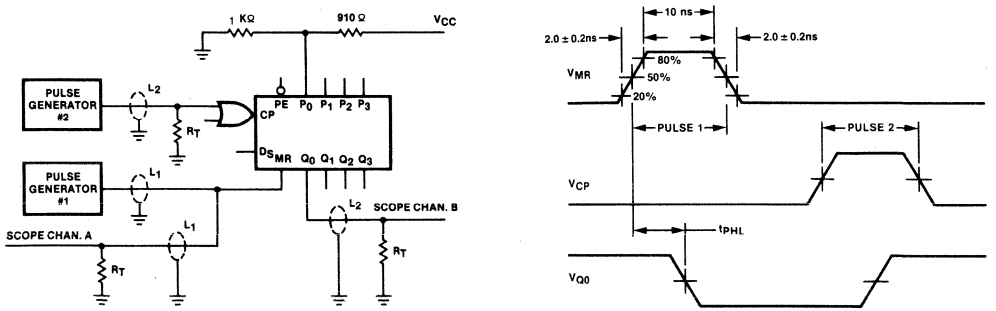




$L_1 = L_2 = 50\ \Omega$ impedence lines
$V_{CC} = +2.0$ V, Pin 1 and 16
$V_{EE} = -3.2$ V, Pin 8
$R_T = 50\ \Omega$ termination of scope
f = 10 MHz
Pulse Width = 10 ns

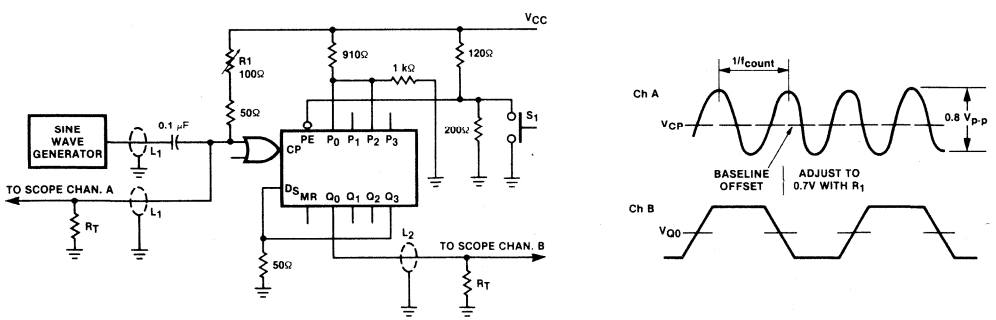
Fig. 1. Clock to Output, Output Transition Time

SWITCHING CIRCUIT AND WAVEFORMS (Cont'd)



$L_1 = L_2 = 50\ \Omega$ impedance lines.
$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\ \Omega$ Termination of Scope
f = 10 MHz
Pulse 2 ≃ Pulse 1

Fig. 2. Master Reset to Output



$L_1 = L_2 = 50\ \Omega$ impedance lines
$V_{CC1} = V_{CC2} = +2.0$ V
$R_T = 50\ \Omega$ termination of scope
$f = f_{MAX}$
Load the register by closing S_1

Fig. 3. Shift Frequency

F10010 • F10016
BCD DECADE COUNTER/4-BIT BINARY COUNTER

GENERAL DESCRIPTION — The F10010 is a high-speed synchronous, presettable, cascadable BCD Decade Counter and the F10016 is a high-speed synchronous, presettable, cascadable 4-Bit Binary Counter. They are multifunction MSI building blocks useful for a large number of counting, digital integration, and conversion applications. Up to nine devices can be cascaded with no speed degradation using standard 10K gates. A multidecade synchronous counter up to 150 MHz can be built. Typical count frequency is 200 MHz.

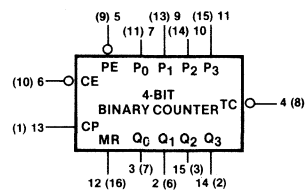
Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.

- **HIGH SPEED COUNT . . . 200 MHz TYPICAL COUNT FREQUENCY**
- **INTERNAL COUNT ENABLE—FOR HIGHEST SPEED EXPANSION**
- **ASYNCHRONOUS MASTER RESET**
- **50 Ω DRIVE CAPABILITY**
- **WIRED-OR CAPABILITY**
- **SEPARATE V_{CC} PINS—ELIMINATE NOISE COUPLING**
- **INTERNAL 50 kΩ INPUT PULL DOWNS**
- **SINGLE −5.2 V POWER SUPPLY**

PIN NAMES

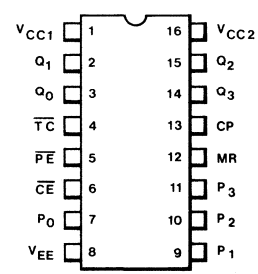
$\overline{PE}$	Parallel Load Enable (Active LOW)
P_n	Parallel Inputs
CP	Clock Input (Clocks on Positive Transition)
$\overline{CE}$	Count Enable (LOW to Count)
MR	Master Reset (HIGH Forces all Q Outputs LOW)
$\overline{TC}$	Terminal Count (10010, LOW at HLLH; 10016 LOW at HHHH)
Q_n	Counter Outputs

LOGIC SYMBOL

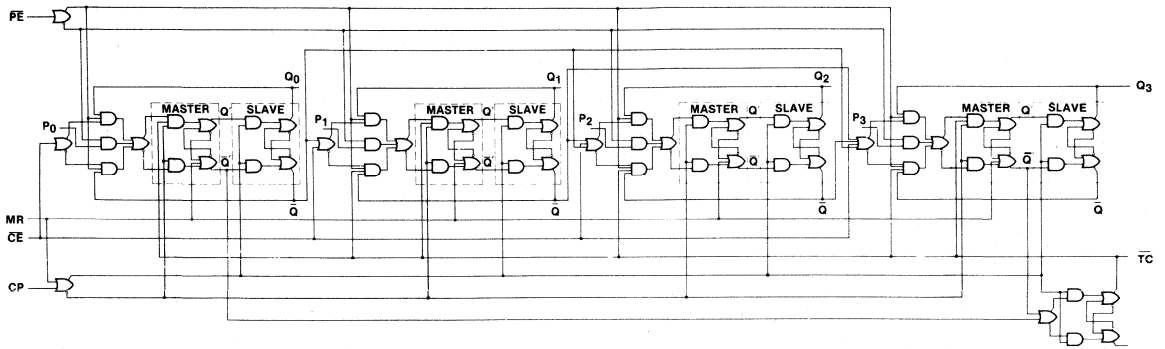


V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

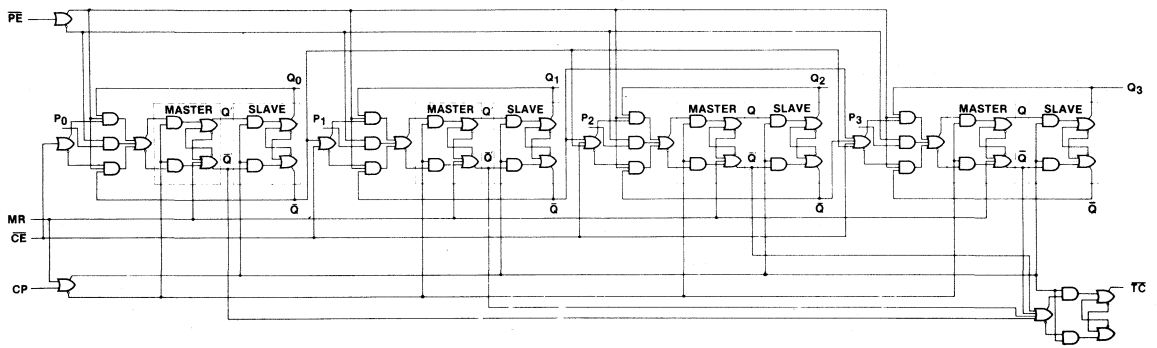
CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



LOGIC DIAGRAM F10010



LOGIC DIAGRAM F10016



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

FUNCTIONAL DESCRIPTION — The F10010 is a high-speed BCD Decade Counter and the F10016 is a high-speed Binary Counter. The four master/slave flip-flops are fully synchronous and are driven in parallel through a clock driver. The masters are loaded during the LOW period of the clock pulse. During the LOW to HIGH transition of the clock, the master is disabled from the input and data is transferred to the slaves and then to the outputs. When the clock is HIGH, the masters are inhibited from changing and the master/slave data path remains open. During the HIGH to LOW transition of the clock, the master/slave data path is inhibited, followed by the enabling of the masters for the acceptance of inputs from the counting logic, parallel entry, or count hold logic.

The Terminal Count ($\overline{TC}$) is generated at count 9 (HLLH) on the 10010 and at count 15 (HHHH) on the 10016.

The $\overline{TC}$ output is available simultaneously with the Q outputs through the use of unique lookahead logic and a fifth slave which is loaded during the LOW portion of the clock cycle. This feature, in conjunction with the triggered Count Enable ($\overline{CE}$) and the Parallel Enable ($\overline{PE}$) select the mode of operation as shown in the table next page. The status of these control lines is sampled only during the LOW to HIGH transition of the clock.

The Master Reset (MR) function is asynchronous. When HIGH, it overrides all other commands and forces all Q outputs LOW and the $\overline{TC}$ HIGH.

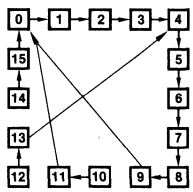
TRUTH TABLE

$\overline{CE}$	$\overline{PE}$	MR	CP	Function
L	L	L	Z	Load Parallel (P_n to Q_n)
H	L	L	Z	Load Parallel (P_n to Q_n)
L	H	L	Z	Count
H	H	L	Z	Hold
X	X	L	ZZ	Masters Respond; Slaves Hold
X	X	H	X	Reset (Q_n = LOW, $\overline{TC}$ = HIGH)

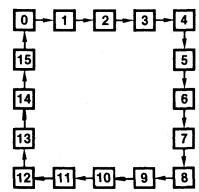
L = LOW
H = HIGH Voltage Level
X = Don't Care
Z = Clock Pulse (LOW to HIGH)
ZZ = Clock Pulse (HIGH to LOW)

STATE DIAGRAMS

F10010



F10016



NOTE: The 10010 can be preset to any state, but will not count beyond 9 (HLLH). If preset to state 10, 11, 12, 13, 14 or 15, it will return to its normal sequence within two clock pulses.

DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND

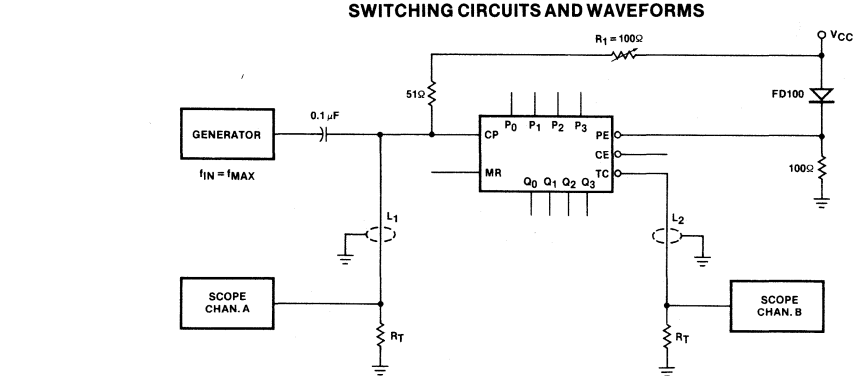
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH MR (Pin 12)			265 700	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−115	−80		mA	25°C	Outputs Open, Pin 12 Tied to V_{IH}

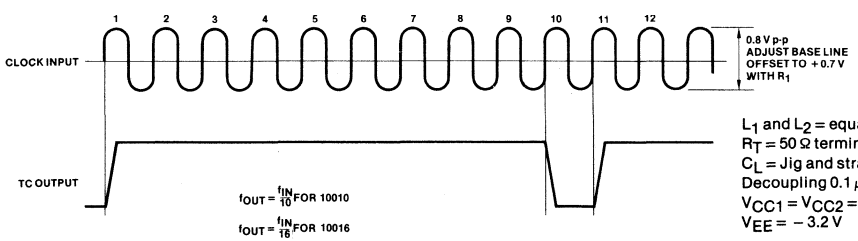
SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
f_{count}	Count Frequency	140	200		MHz	See Figure 1
t_{PLH}	Propagation Delay Clock to Output (Q_n or $\overline{TC}$)	2.0	3.6	5.0	ns	See Figure 2
t_{PHL}	Propagation Delay Clock to Output (Q_n or $\overline{TC}$)	2.0	3.6	5.0	ns	
t_{PHL}	Propagation Delay Master Reset to Output		4.0		ns	See Figure 3
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.3	2.5	3.3	ns	See Figure 2
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.3	2.5	3.3	ns	
t_w	Clock Pulse Width		2.3		ns	See Figure 2
t_w	MR Pulse Width		2.8		ns	See Figure 3
t_s	Set-Up Time Prior to Clock P_n to CP	2.0			ns	
t_h	Hold Time After Clock P_n to CP	1.0			ns	
t_s	Set-Up Time Prior to Clock PE or CE to CP	2.5			ns	
t_h	Hold Time After Clock PE or CE to CP	0.5			ns	

7

SWITCHING CIRCUITS AND WAVEFORMS

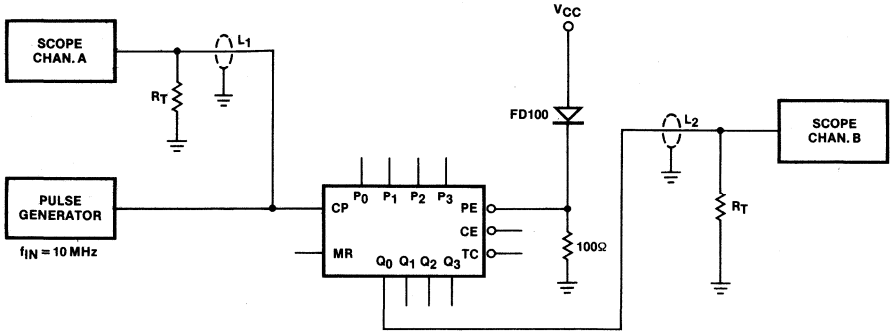


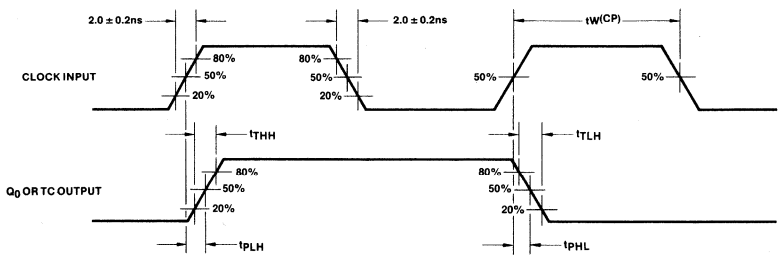


L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 1. Maximum Count Frequency

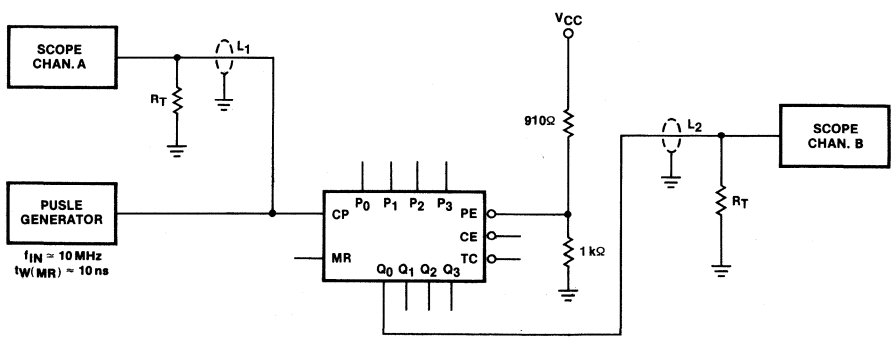
SWITCHING CIRCUITS AND WAVEFORMS (Cont'd)

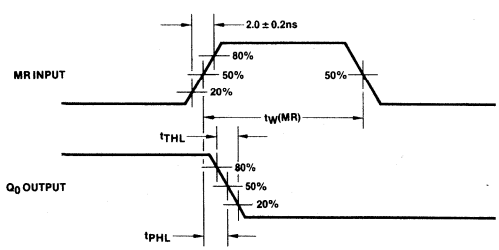




L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 2. Clock to Output

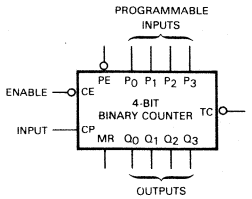




L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

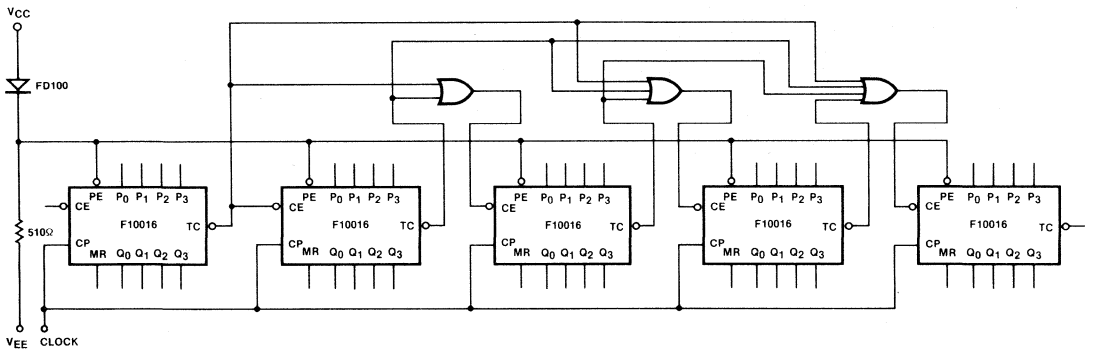
Fig. 3. Master Reset to Output

APPLICATION INFORMATION



DIVIDE RATIO	INPUT REQUIRED P_0	P_1	P_2	P_3
2	L	H	H	H
3	H	L	H	H
4	L	L	H	H
5	H	H	L	H
6	L	H	L	H
7	H	L	L	H
8	L	L	L	H
9	H	H	H	L
10	L	H	H	L
11	H	L	H	L
12	L	L	H	L
13	H	H	L	L
14	L	H	L	L
15	H	L	L	L
16	L	L	L	L

The F10016 may be connected to divide by any modulo from 2 to 16. The table illustrates the inputs required for each modulo. The terminal count output is utilized to load the parallel data, this in turn determines the number of clock pulses which will occur before $\overline{TC}$ goes LOW again.



CASCADE COUNTERS USING OR GATES FOR CARRY PROPAGATION

F10014

ACTIVE TERMINATOR

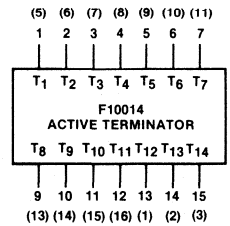
F10K VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION — The F10014 is a voltage compensated ECL circuit which replaces discrete diode clamping circuits at considerable reduction in cost, board space and power dissipation. It operates from the standard −5.2 V ECL power supply and has 14 termination pins. Each termination pin is a bilateral clamp, acting as a low impedance source, which sinks current at the V_{OH} level and sources current at the V_{OL} level. In the transition region between V_{OL} and V_{OH}, a termination pin has a high impedance and thus has minimal effect on signal rise times.

The clamping action limits overshoot and ringing in situations where wiring impedance is not controlled or where other types of termination are not practical. The clamp voltage levels are fully compatible with all ECL families. The very low power supply current and low drain on signal sources minimizes power dissipation.

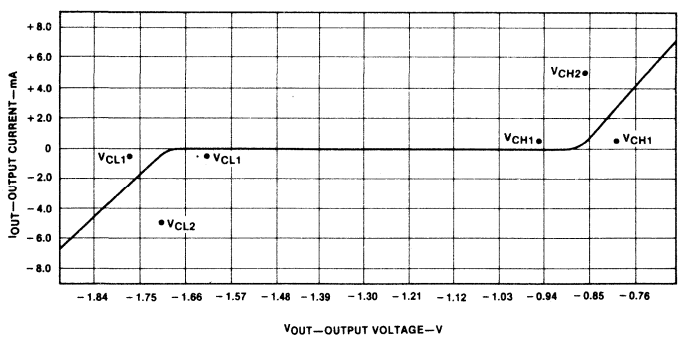
- **LOW STANDBY POWER −4.5 mW/TERMINAL**
- **COMPATIBLE WITH ALL ECL LOGIC FAMILIES**
- **ALLOWS SINGLE ENDED INTERFACE WITHOUT LOSS OF NOISE IMMUNITY**
- **MATCHED IMPEDANCE LINES OR TERMINATING RESISTORS ARE NOT REQUIRED**
- **ELIMINATES NEED FOR −2.0 V SUPPLY AT INTERFACE**

LOGIC SYMBOL

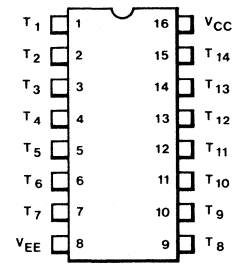


V_{EE} = 8 (12)
V_{CC} = 16 (4)
( ) = Flatpak

TYPICAL V_{OUT} VERSUS I_{OUT} CHARACTERISTIC



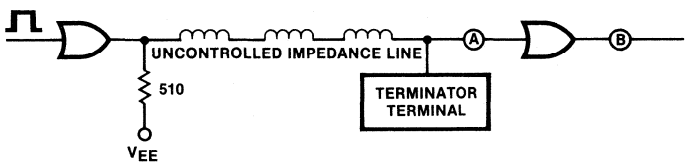
CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



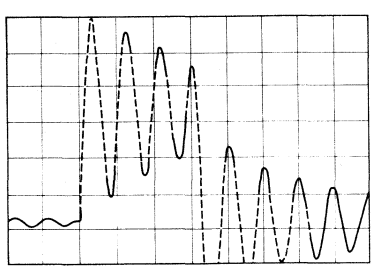
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
V_{CH1}	Clamp Voltage HIGH	−1000 −980 −1020		−810 −830 −790	mV	0°C 25°C 75°C	$V_{IN} = +0.5$ mA
V_{CL1}	Clamp Voltage LOW	−1870 −1800 −1800		−1650 −1650 −1550	mV	0°C 25°C 75°C	$I_{IN} = -0.5$ mA
V_{CH2}	Clamp Voltage HIGH	−890			mV	25°C	$I_{IN} = +5.0$ mA
V_{CL2}	Clamp Voltage LOW			−1740	mV	25°C	$I_{IN} = -5.0$ mA
I_{EE}	Power Supply Current	−16	−12		mA	25°C	Terminals Open

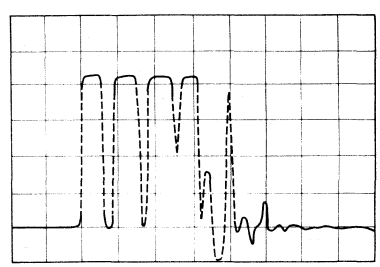
PERFORMANCE OF ACTIVE TERMINATOR



The terminator should be placed sufficiently close to the receiving circuit so the ringing caused by reflections will be limited to 35% overshoot of the signal. Under worst case conditions, with the device on a PC board and using microstrip connecting techniques, this distance should not exceed five inches.

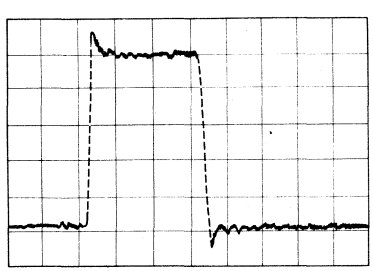


POINT A WITHOUT TERMINATOR

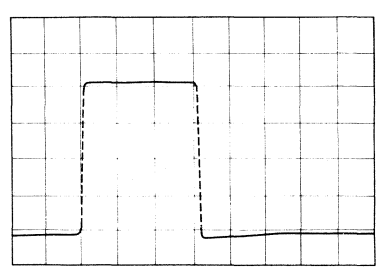


POINT B WITHOUT TERMINATOR

SCALE: VERTICAL = 200 mV/div HORIZONTAL = 50 ns/div



POINT A WITH TERMINATOR



POINT B WITH TERMINATOR

APPLICATIONS

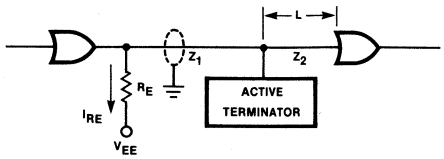


Fig. 1
ACTIVE TERMINATOR APPLICATION EXAMPLE

$$\Delta V = \Delta I \cdot Z_1 \geq 0.6\ V$$

$$\Delta I = I_{RE} = \frac{V_{OH} - V_{EE}}{R_E + Z_1}$$

$$R_E \leq 6.3\, Z_1$$

TABLE 1

R_E Ω	Z_1 Ω	P_D (avg) mW		I_{RE} (avg) mA
		R_E	IC Output	
330	50	46	15	12
390	62	39	13	10
470	75	32	10	8.2
560	90	28	8.7	7.0
620	100	25	7.8	6.4
1K		16	4.8	4.0

R_E Value Determination Method

Resistor R_E provides the pull down current necessary to generate the negative going signal swing when the driver output goes LOW. An initial step of 0.6 V is sufficient to ensure a clean negative edge in worst-case situations. Since the initial step voltage is the product of I_{RE} and the line impedance Z_1 (see Table 1), the minimum R_E value for a given Z_1 can be calculated. Use a quiescent V_{OH} value of −0.82 V, which is a typical value for the range of R_E values commonly used.

Prorated standby power = (16 mA) (5.2 V)14 terminators = 6.0 mW/terminator. Signal power dissipation = ½ mA ($V_{EE} - V_{OH}$)/2 ≅ 1.0 mW. In the V_{OL} state, the signal dissipation in the terminator matches the decrease in dissipation in the driving circuit output. Terminator dissipation is ≅ 7.0 mW/terminator.

Line Length (L) Determination Method

The interconnection from the terminator to the receiving circuit (L in Figure 1) constitutes an unterminated line and is therefore subject to reflections. Thus the length L must be limited to prevent excessive overshoot and ringing at the receiver input. When more than one receiving circuit is connected to the same line, the length must be proportionately shorter. Maximum recommended lengths for microstrip and stripline on G10 epoxy board are listed in Tables 2-5 for various A_2 values. Tables 2 and 3 apply when the receiving circuits are distributed along L, while Tables 4 and 5 apply when the receiving circuits are concentrated at the unterminated end of L. Methods for determining appropriate limits for other types of board material are given in the Users Guide section of the Fairchild ECL Handbook.

TABLE 2
MAXIMUM WORST-CASE LINE LENGTHS (L) FOR MICROSTRIP

Z_2	NUMBER OF FAN OUT LOADS				
	2	3	4	6	8
50	4.15	3.75	3.45	2.85	2.45
62	3.95	3.50	3.15	2.55	2.10
75	3.75	3.25	2.85	2.25	1.85
90	3.55	3.00	2.60	2.00	1.60
100	3.45	2.85	2.45	1.85	1.45

TABLE 3
MAXIMUM WORST-CASE LINE LENGTHS (L) FOR STRIPLINE

Z_2	NUMBER OF FAN OUT LOADS				
	2	3	4	6	8
50	3.30	3.00	2.70	2.55	1.90
62	3.15	2.80	2.50	2.00	1.65
75	3.00	2.60	2.25	1.80	1.45
90	2.80	2.40	2.05	1.55	1.25

Length in inches
Unit load = 3.0 pF; epoxy board distributed loading.

TABLE 4
MAXIMUM WORST-CASE LINE LENGTHS (L) FOR MICROSTRIP

Z_2	NUMBER OF FAN OUT LOADS				
	1	2	4	6	8
50	4.40	3.65	2.60	1.90	1.40
62	4.30	3.45	2.30	1.60	1.15
75	4.20	3.20	2.05	1.40	0.95
90	4.05	2.95	1.75	1.05	0.65
100	3.90	2.80	1.60	0.90	0.50

TABLE 5
MAXIMUM WORST-CASE LINE LENGTHS (L) FOR STRIPLINE

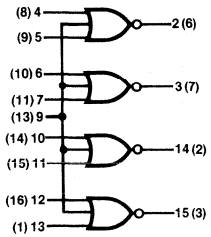
Z_2	NUMBER OF FAN OUT LOADS				
	1	2	4	6	8
50	3.45	2.85	2.00	1.50	1.10
62	3.40	2.70	1.80	1.30	0.90
75	3.30	2.55	1.60	1.10	0.75
90	3.15	2.35	1.40	0.85	0.50
100	3.10	2.20	1.25	0.70	0.40

Length in inches
Unit load = 3.0 pF; epoxy board concentrated loading.

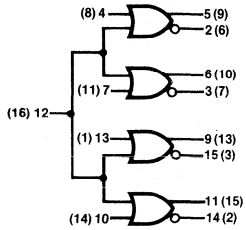
LOGIC DIAGRAMS

V_{CC1} = Pin 1(5), V_{CC2} = Pin 16(4), V_{EE} = Pin 8(12), ( ) = Flatpak

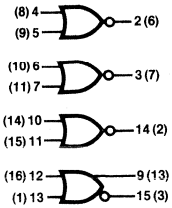
F10100/F10500



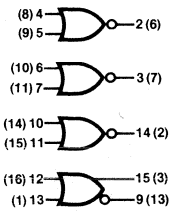
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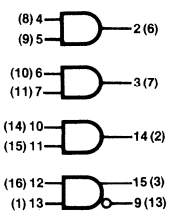
F10102/10502



F10103/10503

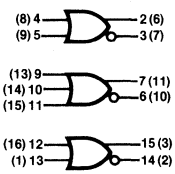


F10104/10504

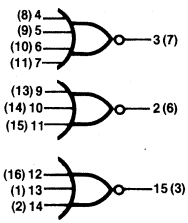


V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = 8 (12)

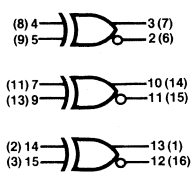
F10105/10505



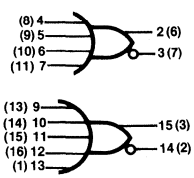
F10106/10506



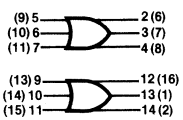
F10107/10507



F10109/10509

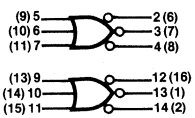


F10110/10510



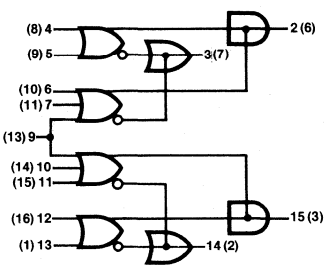
V_{CC1} = 1, 15 (5, 3)
V_{CC2} = 16 (4)

F10111/10511

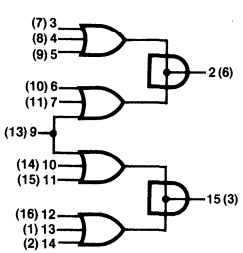


V_{CC1} = 1, 15 (5, 3)
V_{CC2} = 16 (4)

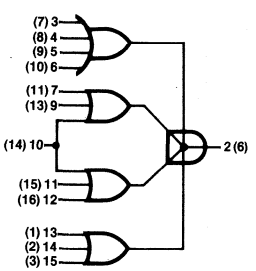
F10117/10517



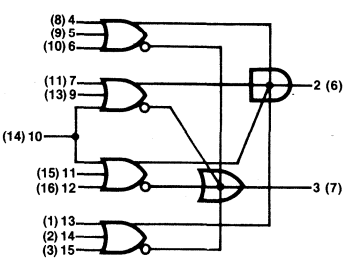
F10118/10518



F10119/10519



F10121/10521



7

F10K SERIES
GATE FAMILY SPECIFICATIONS

DC CHARACTERISTICS: $V_{EE} = -5.2\,V, V_{CC} = GND$

F10100 • F10500 • F10101 • F10501 • F10102 • F10502
F10103 • F10503 • F10104 • F10504 • F10105 • F10505
F10106 • F10506 • F10107 • F10507 • F10109 • F10509
F10110 • F10510 • F10111 • F10511 • F10118 • F10518
F10119 • F10519 • F10121 • F10521

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	All Input Current HIGH's are 265, unless otherwise noted				μA	25°C	$V_{IN} = V_{IHA}$
	F10100 Pin 9			550			
	F10101 Pin 12			550			
	F10103 All Inputs			245			
	F10104 Pins 4, 6, 10, 12			220			
	F10107 Pins 5, 7, 15			220			
	F10110 All Inputs			425			
	F10111 All Inputs			425			
	F10118 Pin 9			370			
	F10119 Pin 10			370			
	F10121 Pin 10			370			
I_{EE}	Power Supply Current				mA	25°C	Inputs and Outputs Open
	F10100	−26	−21				
	F10101	−26	−20				
	F10102	−26	−20				
	F10103	−26	−20				
	F10104	−35	−28				
	F10105	−21	−15				
	F10106	−21	−15				
	F10107	−28	−22				
	F10109	−14	−10				
	F10110	−38	−28				
	F10111	−38	−28				
	F10118	−26	−20				
	F10119	−26	−20				
	F10121	−26	−20				

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2\,V, T_A = 25°C$

F10100 • F10101 • F10102 • F10103 • F10105 • F10106 • F10109
F10500 • F10501 • F10502 • F10503 • F10505 • F10506 • F10509

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay	1.0	2.0	2.9	ns	See Figure 1
t_{TLH} t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.5	2.2	3.3	ns	

SWITCHING CHARACTERISTICS: V_{EE} = −5.2 V, T_A = 25°C **F10104 • F10504**

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay Inputs 5, 6, 11, 12	1.4	2.2	3.4	ns	See Figure 1
t_{PHL}, t_{PLH}	Propagation Delay, Inputs 4, 7, 10, 13	1.4	2.9	3.7	ns	
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.5	2.2	3.5	ns	

SWITCHING CHARACTERISTICS: V_{EE} = −5.2 V, T_A = 25°C **F10107 • F10507**

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay	1.1	2.4	3.7	ns	See Figure 1
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.5	2.5	3.5	ns	

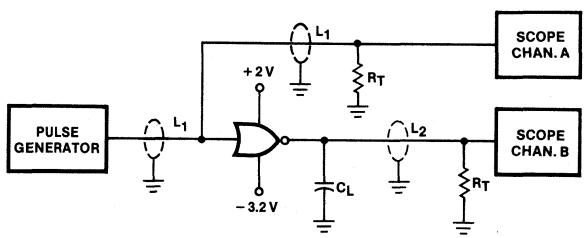
SWITCHING CHARACTERISTICS: V_{EE} = −5.2 V, T_A = 25°C **F10110 • F10510 • F10111 • F10511**

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay	1.4	2.4	3.5	ns	See Figure 1
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.5	2.2	3.5	ns	

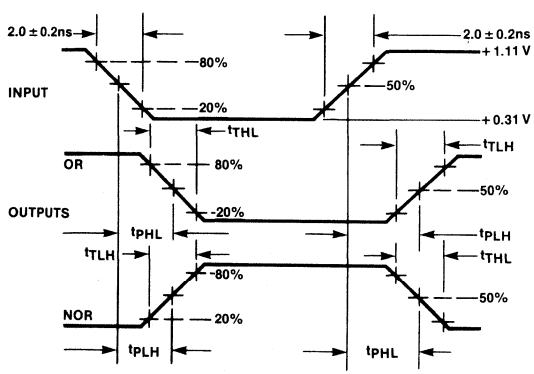
SWITCHING CHARACTERISTICS: V_{EE} = −5.2 V, T_A = 25°C **F10118 • F10518 • F10119 • F10519 • F10121 • F10521**

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay	1.4	2.3	3.4	ns	See Figure 1
t_{TLH} t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.5	2.2	4.0	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}



Jig set-up with no circuit under test
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 1

F10113 • F10513

QUAD EXCLUSIVE OR WITH ENABLE

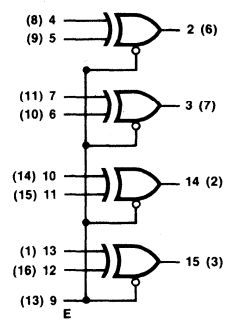
F10K VOLTAGE COMPENSATED ECL

DESCRIPTION — The F10113 and F10513 are Quad Exclusive OR Gates, with an Enable common to all four gates. When the Enable ($\overline{E}$) input is HIGH, all outputs are forced LOW.

A 4-bit active LOW comparator can be formed by tying the four outputs together. When each pair of inputs agrees, the output will go LOW. A disagreement in any pair will cause the output to go HIGH.

Input pull-down resistors included in the circuit make it unnecessary to tie down unused inputs. Open emitter outputs permit direct connection to busses.

LOGIC SYMBOL



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
( ) = Flatpak

- **VOLTAGE COMPENSATED . . . NOISE MARGIN INSENSITIVE TO POWER SUPPLY VARIATIONS AND GRADIENTS: RELAXED POWER SUPPLY REQUIREMENTS**
- **INTERNAL 50 k Ω (NOMINAL) PULL-DOWN RESISTORS . . . UNUSED INPUTS MAY BE LEFT OPEN**
- **OPEN EMITTER-FOLLOWER OUTPUTS DRIVE TERMINATED LINES**
- **SINGLE V_{EE} POWER SUPPLY . . . -4.7 V TO -6.2 V**
- **FULLY COMPATIBLE WITH OTHER 10K SERIES ECL**

7

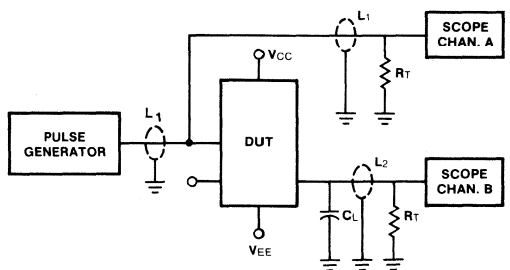
DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH				uA	25°C	V_{IN} = V_{IHA}
	Pin 9			545			
	Pins 5, 6, 11, 12			220			
	Pins 4, 7, 10, 13			265			
I_{EE}	Power Supply Current	−42	−33		mA	25°C	Inputs Open

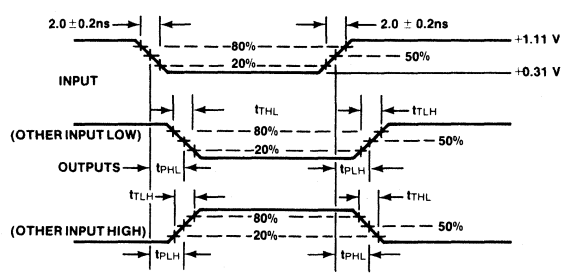
SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay, Inputs to Outputs	1.1	2.5	3.7	ns	See Figure 1
t_{PHL}, t_{PLH}	Propagation Delay, $\overline{E}$ to Outputs	1.1	3.0	4.0	ns	
t_{TLH}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.5	2.0	3.5	ns	

SWITCHING TEST CIRCUIT AND WAVEFORMS



Jig set-up with no circuit under test
$V_{CC1} = V_{CC2}$ = +2.0V
V_{EE} = -3.2 V



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}

Figure 1

F10114 • F10514

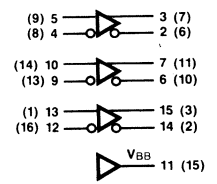
LINE RECEIVER

F10K VOLTAGE COMPENSATED ECL

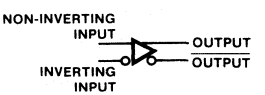
DESCRIPTION — The F10114 and F10514 are Triple Differential Amplifiers with low impedance emitter-follower outputs. An internal reference supply (V_{BB}) is available for added versatility. Active current sources provide an improved common mode rejection limit of 1 V in either the positive or the negative direction. The devices are used primarily to receive data from balanced twisted pair lines; however, with appropriate external circuitry, they may operate as Schmitt triggers, high speed comparators, oscillators, or broadband amplifiers. The F10114 is voltage compensated and fully compatible with other 10,000 series devices.

- **±1 V COMMON MODE REJECTION**
- **FULLY COMPATIBLE WITH 10K**
- **VOLTAGE COMPENSATED**
- **TRUE AND COMPLEMENTARY OUTPUTS**
- **V_{BB} REFERENCE VOLTAGE**
- **OPEN BASE INPUTS (NO 50 k INPUT PULLDOWNS)**

LOGIC DIAGRAM



FUNCTION



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
( ) = Flatpak

TRUTH TABLE

NON-INVERTING INPUT	INVERTING INPUT	TRUE OUTPUT	COMPLEMENT OUTPUT
L	H	L	H
H	L	H	L
L	V_{BB}	L	H
H	V_{BB}	H	L
V_{BB}	H	L	H
V_{BB}	L	H	L
H	H	UNDEFINED	
L	L	UNDEFINED	
OPEN	OPEN	L	H

NOTE: See Page 7-33 for addtional applications information.

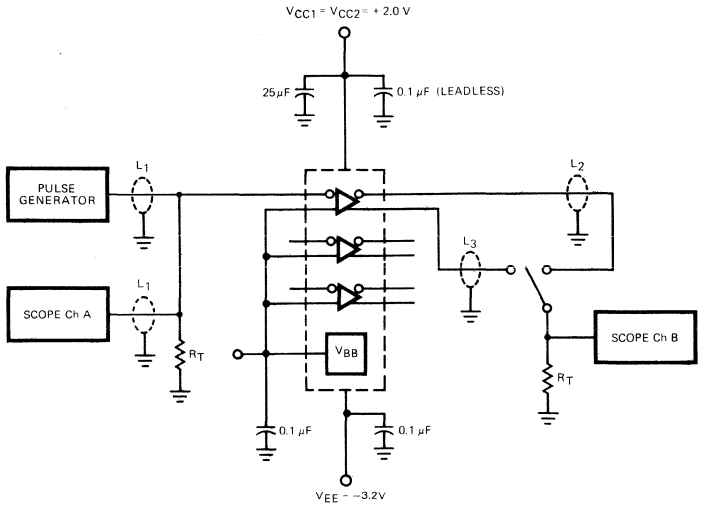
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

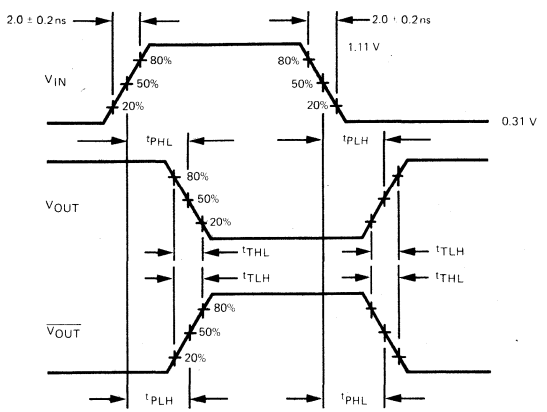
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
V_{IHH}	Common Mode Rejection Input Voltage HIGH +1.0 V			+0.170 +0.280 +0.420	V	-55°C 25°C 125°C	
V_{ILH}	Common Mode Rejection Input Voltage LOW +1.0 V	-0.920 -0.850 -0.820			V	-55°C 25°C 125°C	
V_{IHL}	Common Mode Rejection Input Voltage HIGH -1.0 V			-1.830 -1.720 -1.580	V	-55°C 25°C 125°C	
V_{ILL}	Common Mode Rejection Input Voltage LOW -1.0 V	-2.920 -2.850 -2.820			V	-55°C 25°C 125°C	
V_{BB}	Reference Voltage	-1440 -1350 -1240		-1320 -1230 -1120	mV	-55°C 25°C 125°C	Connect pins 8, 10, 13 to pin 11
I_{IH}	Input Current HIGH			45	μA	25°C	$V_{IN} = V_{IHA}$
I_{CBO}	Input Collector - Base Leakage Current	-1.0			μA	25°C	V_{IN} = -5.2 V
I_{EE}	Power Supply Current	-35	-28		mA	25°C	pins 4, 9, 12 = V_{ILB}, pins 5, 10, 13 = V_{BB}
V_{BB}	Reference Voltage	-1380 -1350 -1305		-1255 -1230 -1165	mV	0°C 25°C 75°C	Connect pins 5, 10, 13 to pin 11
V_{IHH}	Common Mode Rejection Input Voltage HIGH +1.0 V			+0.160 +0.190 +0.280	V	0°C 25°C 75°C	
V_{ILH}	Common Mode Rejection Input Voltage LOW +1.0 V	-0.870 -0.850 -0.830			V	0°C 25°C 75°C	
V_{IHL}	Common Mode Rejection Input Voltage HIGH -1.0 V			-1.840 -1.810 -1.720	V	0°C 25°C 75°C	
V_{ILL}	Common Mode Rejection Input Voltage LOW -1.0 V	-2.870 -2.850 -2.830			V	0°C 25°C 75°C	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay	1.0	2.1	4.0	ns	See Figure 1
t_{TLH}, t_{THL}	Output Transition Time 20% to 80%, 80% to 20%	1.5	2.1	3.5	ns	

SWITCHING TEST CIRCUIT AND WAVEFORMS





Unused outputs connect to a 50Ω resistor to ground.

One input from each gate must be tied to V_{BB} during testing.

L_1, L_2, and L_3 = equal length 50Ω impedance lines.

R_T = 50Ω termination of scope

Figure 1

F10115 • F10116 • F10515 • F10516
LINE RECEIVERS

DESCRIPTION — The F10115 and F10116 are differential amplifiers with low impedance emitter-follower outputs. An internal reference supply (V_{BB}) is available for added versatility. Active current sources provide improved common mode rejection. The F10115 is a quad line receiver with single ended outputs. The F10116 is a triple line receiver with complementary outputs. The devices are voltage compensated and are fully compatible with other 10,000 series devices. The line receivers are used primarily to receive data from balanced twisted pair lines, however, with appropriate connections and feedback, they may operate as Schmitt triggers, high-speed comparators, oscillators, or broadband amplifiers.

TRUTH TABLES

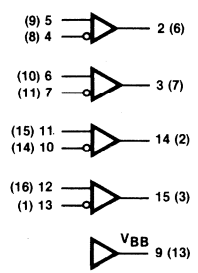
F10115 Quad Line Receiver

NON-INVERTING INPUT	INVERTING INPUT	OUTPUT
L	H	L
H	L	H
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	H	L
V_{BB}	L	H

F10116 Triple Differential Line Receiver

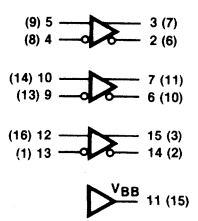
NON-INVERTING INPUT	INVERTING INPUT	OUTPUT	$\overline{\text{OUTPUT}}$
L	H	L	H
H	L	H	L
L	V_{BB}	L	H
H	V_{BB}	H	L
V_{BB}	H	L	H
V_{BB}	L	H	L

LOGIC DIAGRAM



( ) = Flatpak

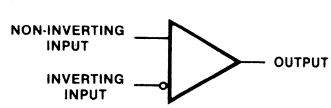
F10115 • F10515



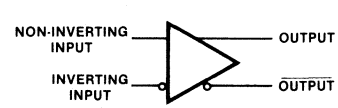
( ) = Flatpak

F10116 • F10516

FUNCTIONS



V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)



V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)

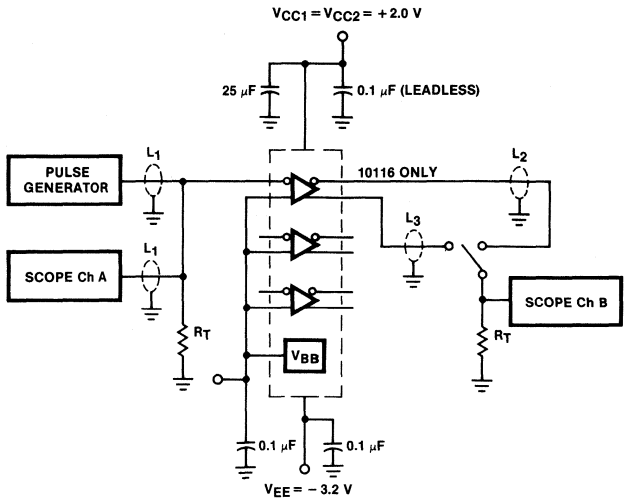
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC		LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH				95	μA	25°C	$V_{IN} = V_{IHA}$
I_{CBO}	Input Collector—Base Leakage Current		−1.0			μA	25°C	$V_{IN} = -5.2$ V
I_{EE}	Power Supply Current	F10115	−26	−18		mA	25°C	Pins 4, 7, 10, 13 = V_{ILB}' Pins 5, 6, 11, 12 = V_{BB}
		F10116	−21	−14		mA	25°C	Pins 4, 9, 12 = V_{ILB}' Pins 5, 10, 13 = V_{BB}
V_{BB}	Reference Voltage		−1380		−1255	mV	0°C	F10115, Connect pins i.e.; 5, 6, 11, 12 to pin 9
			−1350		−1230		25°C	
			−1305		−1165		75°C	F10116, Connect Pins i.e.; 5, 10, 13 to pin 11
V_{BB}	Reference Voltage		−1440		−1320		−55°C	F10115, Connect pins i.e.; 5, 6, 11, 12 to pin 9
			−1350		−1230		25°C	
			−1240		−1120		125°C	F10116, Connect Pins i.e.; 5, 10, 13 to pin 11

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay	1.0	2.0	2.9	ns	See Figure 1
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.5	2.2	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



One input from each gate must be tied to V_{BB} during testing.

L_1, L_2, and L_3 = equal length 50Ω impedance lines.

R_T = 50Ω termination of scope

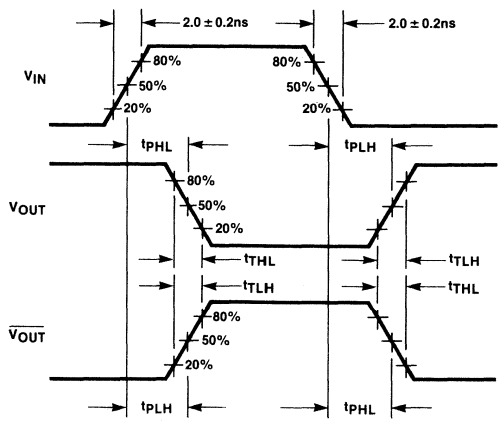


Fig.1

A line receiver is shown in *Figure 2*. The line is normally terminated in its characteristic impedance (typically 100 Ω) and output pull down resistors (typically 510 Ω) are used. The voltage across the terminating resistor V_T may be calculated as follows:

$$V_T = \frac{(V_{EE} - V_{OH})\, R_T}{R_E + R_T + R_{LINE}}$$

Where V_{OH} is the output voltage HIGH of the driving gate, R_{LINE} is the resistance and R_T is the terminating resistor. With typical values, V_T is 620 mV. The line receivers have a minimum differential input voltage gain of 7 V/V allowing very long twisted pairs to be driven. The line receivers employ active current sources which allow them to reject common mode inputs between -0.55 and -3 V.

Information transfer is often organized with a data bus approach, where many sources may input and receive data on a common bus as illustrated in *Figure 3*. This configuration is a special case of wired-OR and the line receiver inputs are essentially single ended which reduces worst case voltage gain to 3.5 V/V. In practice it is possible to transmit data at rates in excess of 100 MHz over bus lengths of 10 feet, having 10 or more receivers and transmitters on the line.

Twisted pair differential lines are recommended for clock distribution since clock skew may be balanced by adjusting line lengths. Propagation time is approximately 1 ns per eight inches of line.

TWISTED-PAIR CONNECTIONS

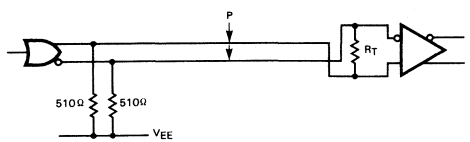


Fig. 2. Differential Transmission and Reception

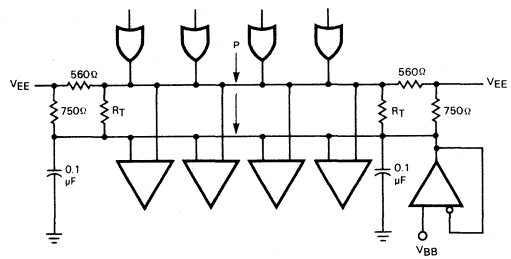


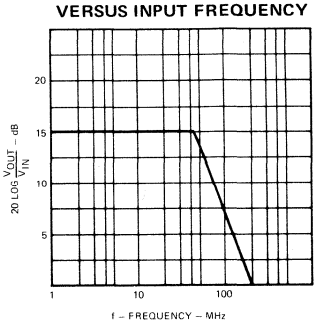
Fig. 3. Backplane Data Bus

PARAMETERS FOR LINEAR APPLICATIONS

V_{EE} = -5.2 V, V_{CC} = GND, T_A = 25°C

PARAMETER	LIMITS			UNITS
	B	TYP	A	
Voltage Gain	3.5	5.0	6.0	V/V
Bandwidth		60		MHz
Input Resistance	4	6		kΩ
Input Capacitance		3		pF
Input Offset Current		2		μA
Input Bias Current		17	30	μA
Common Mode Input Voltage Range	-3.0		-0.55	V
Common Mode Rejection Ratio	50			dB
Supply Voltage Rejection Ratio		35		dB
Output Voltage Swing		0.40		Vpp
Output Source Current			50	mA
Output Resistance		9		Ω

TYPICAL LINE RECEIVER DIFFERENTIAL GAIN VERSUS INPUT FREQUENCY



F10123 • F10523

TRIPLE BUS DRIVER

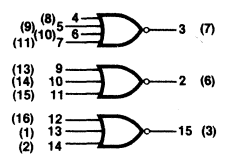
F10K VOLTAGE COMPENSATED ECL

DESCRIPTION — The F10123 and F10523 contain three NOR gates designed for bus driving applications. The outputs are designed and specified for driving 25 Ω loads to −2.1 V. This allows an output to drive a 50 Ω bus terminated at both ends. Higher impedance busses can also be driven.

The output LOW level is designed and specified to be less than −2.0 V. This means that a passive output tied to a bus is a high impedance and thus has little or no effect on the characteristic impedance of the bus. Reflections and resultant waveform distortion are thus reduced to a minimal level.

- **VOLTAGE COMPENSATED . . . NOISE MARGIN INSENSITIVE TO POWER SUPPLY VARIATIONS AND TRANSIENTS, RELAXED POWER SUPPLY REQUIREMENTS**
- **INTERNAL 50 kΩ (NOMINAL) INPUT PULL-DOWN RESISTORS . . . UNUSED INPUTS MAY BE LEFT OPEN**
- **OPEN EMITTER-FOLLOWER OUTPUTS DRIVE TERMINATED LINES**
- **SINGLE V_{EE} POWER SUPPLY . . . −4.7 TO −6.2 V**
- **FULLY COMPATIBLE WITH OTHER 10,000 SERIES ECL**

LOGIC DIAGRAM



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
( ) = Flatpak

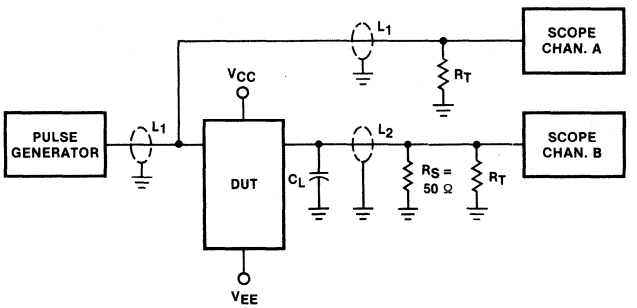
DC CHARACTERISTICS: V_{EE} = −5.2V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
V_{OL}	Output Voltage LOW	−2100		−2030	mV	0°C	Loading is 25 Ω to −2.1 V
		−2100		−2030		25°C	
		−2100		−2030		75°C	
V_{OLC}	Output Voltage LOW			−2010	mV	0°C	
				−2010		25°C	
				−2010		75°C	
I_{IH}	Input Current HIGH			220	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−75	−60		mA	25°C	Inputs Open
V_{OL}	Output Voltage LOW	−2100		−2030	mV	−55°C	Loading is 25 Ω to −2.1 V
		−2100		−2030		25°C	
		−2100		−2030		+125°C	
V_{OLC}	Output Voltage LOW			−2010	mV	−55°C	
				−2010		25°C	
				−2010		+125°C	

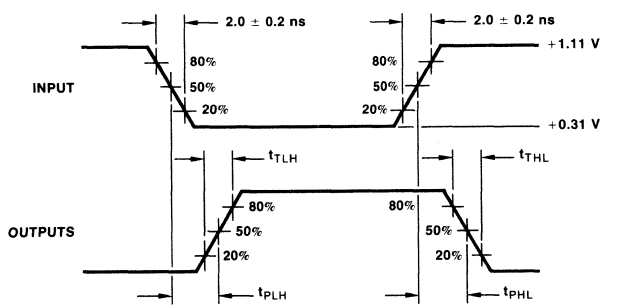
AC CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL}, t_{PLH}	Propagation Delay	1.2	3.0	4.4	ns	
t_{TLH}, t_{THL}	Output Transition Time (20% to 80%)(80% to 20%)	1.0	2.5	3.5	ns	See Figure 1

AC TEST CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}



Jig set-up with no circuit under test
$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V

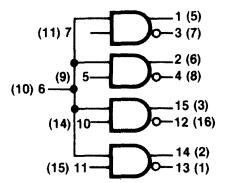
Figure 1

F10124 • F10524
QUAD TTL TO ECL TRANSLATOR

DESCRIPTION — The F10124 and F10524 are Quad Translators, designed to convert TTL logic levels to 10K ECL logic levels. The inputs are compatible with standard or with Schottky TTL. A Common Enable input (E_C), when LOW, holds all inverting outputs HIGH and holds all True outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator or as a differential line driver. The output levels are voltage compensated.

When the circuit is used in the differential mode, the F10124, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems.

LOGIC DIAGRAM



V_{CC} = 9 (13)
V_{EE} = 8 (12)
GND = 16 (4)

Logic Equations
2 = 5•6
4 = 5•6

DC CHARACTERISTICS: $V_{EE} = -5.2$ V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH	+1.9 +1.8 +1.8		5.0 5.0 5.0	V	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs
V_{IL}	Input Voltage LOW	0 0 0		+1.1 +1.1 +0.95	V	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs
V_{CD}	Clamp Input Voltage	−1.5			V	25°C	$I_{IN} = -10$ mA
V_{BD}	Input Breakdown Voltage	+5.5			V	25°C	$I_{IN} = +1.0$ mA, Other Inputs V_{IN} = GND
I_{IH}	Input Current HIGH			50	μA	25°C	$V_{IN} = +2.4$ V, E_C $V_{IN} = +0.4$ V
I_{IHX}	Input Current HIGH E_C			200	μA	25°C	E_C $V_{IN} = +2.4$ V All Other Inputs $V_{IN} = +0.4$ V
I_{ILX}	Input Current LOW E_C	−12.8		mA	25°C		E_C $V_{IN} = +0.4$ V, All Other Inputs $V_{IN} = +4.0$ V
I_{IL}	Input Current LOW	−3.2			mA	25°C	$V_{IN} = +0.4$ V, E_C $V_{IN} = +4.0$ V
I_{EE}	Power Supply Current	−34	−26		mA	25°C	Inputs and Outputs Open
I_{CCH}	Power Supply Current		+13	+16	mA	25°C	All Inputs $V_{IN} = +4.0$ V
I_{CCL}	Power Supply Current		+18	+25	mA	25°C	All Inputs V_{IN} = GND

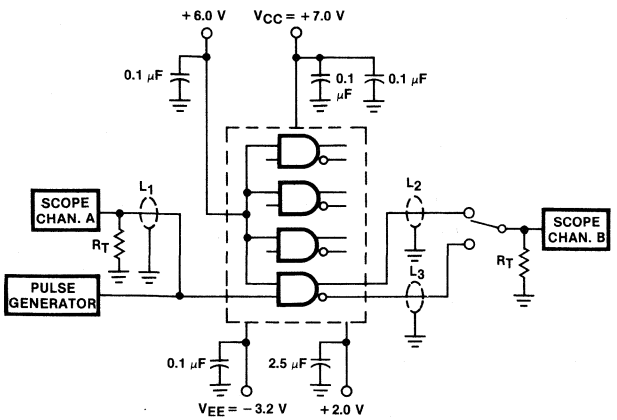
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

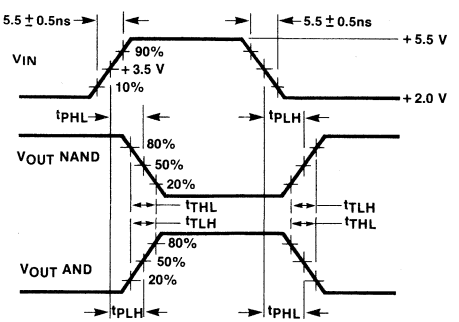
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IL}	Input Current LOW	−3.2			mA	25°C	$V_{IN} = +0.4$ V, E_C $V_{IN} = +4.0$ V
I_{EE}	Power Supply Current	−34	−26		mA	25°C	Inputs and Outputs Open
I_{CCH}	Power Supply Current		+13	+16	mA	25°C	All Inputs $V_{IN} = +4.0$ V
I_{CCL}	Power Supply Current		+18	+25	mA	25°C	All Inputs $V_{IN} = GND$

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay	1.5	3.0	6.0	ns	See Figure 1
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.1	2.5	3.9	ns	

SWITCHING TEST CIRCUIT AND WAVEFORMS





NOTES:

L_1, L_2 and L_3 are equal lengths of 50 Ω impedance lines.
R_T equals 50 Ω termination of scope

Fig. 1

F10125 • F10525

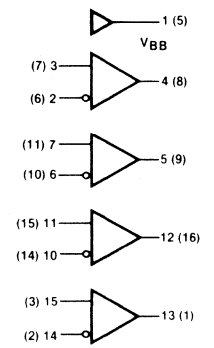
QUAD ECL TO TTL TRANSLATOR

F10K VOLTAGE COMPENSATED ECL

DESCRIPTION — The F10125 and F10525 are Quad Translators for converting F10K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or as a differential receiver. An Internal reference voltage generator provides V_{BB} on Pin 1 for single-ended operation or for use in Schmitt trigger applications. The outputs, which will go LOW when the inputs are left unconnected, have a fan-out of 10 Schottky TTL loads.

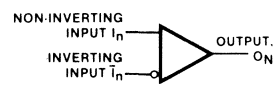
When used in the differential mode, the inputs have a common mode rejection of +1 V, making this device tolerant of ground offsets and transients between the signal source and the translator.

LOGIC DIAGRAM



V_{CC} = 9 (13) GND = 16 (4)
V_{EE} = 8 (12) ( ) = Flatpak

FUNCTION



TRUTH TABLE

INPUTS		OUTPUT
Non-Inverting I_n	Inverting $\overline{I}_n$	O_n
L	H	L
H	L	H
L	L	*
H	H	*
OPEN	OPEN	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

*Undetermined

DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	+2.5 +2.5 +2.5			V	−55/0 °C 25 °C 125/75 °C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is −2.0 mA V_{OH} +20mA V_{OL}
V_{OL}	Output Voltage LOW			+0.5 +0.5 +0.5	V	−55/0 °C 25 °C 125/75 °C		
V_{OHC}	Output Voltage HIGH	+2.5 +2.5 +2.5			V	−55/0 °C 25 °C 125/75 °C	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			+0.5 +0.5 +0.5	V	−55/0 °C 25 °C 125/75 °C		

DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$ (Cont'd)

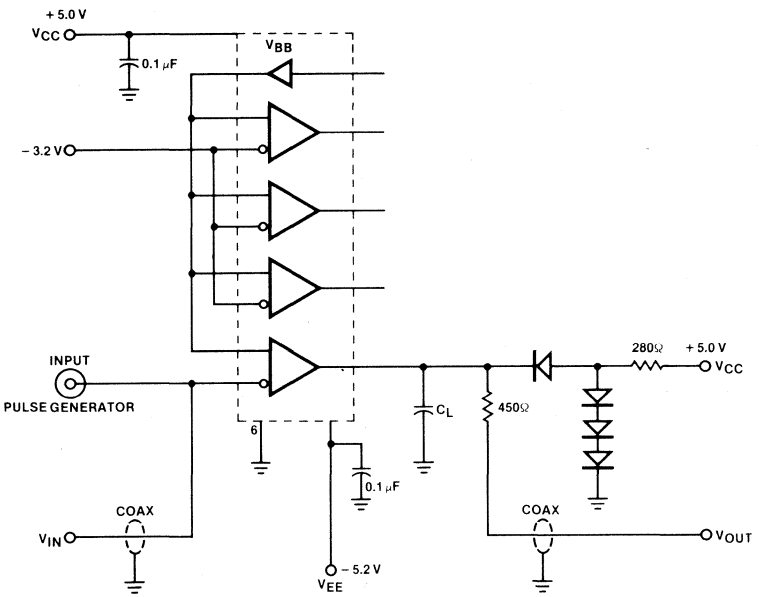
V_{IHH}	Common Mode Rejection Input Voltage HIGH +1.0 V			+0.160 +0.190 +0.280	V	0°C 25°C 75°C	
V_{ILH}	Common Mode Rejection Input Voltage LOW +1.0 V	−0.870 −0.850 −0.830			V	0°C 25°C 75°C	
V_{IHL}	Common Mode Rejection Input Voltage HIGH −1.0 V			−1.840 −1.810 −1.720	V	0°C 25°C 75°C	
V_{ILL}	Common Mode Rejection Input Voltage LOW −1.0 V	−2.870 −2.850 −2.830			V	0°C 25°C 75°C	
V_{BB}	Reference Voltage	−1380 −1350 −1305		−1250 −1230 −1165	mV	0°C 25°C 75°C	$V_{IN} = V_{ILB}$
I_{CBO}	Input Leakage Current	−1.0			μA	25°C	$V_{IN} = V_{EE}$ Note 1
I_{IH}	Input Current HIGH			115	μA	25°C	$V_{IN} = V_{IHA}$ Note 1
I_{OS}	Short Circuit Current	−100		−40	mA	25°C	$V_{IN} = GND$ Note 2
I_{EE}	Negative Power Supply	−40			mA	25°C	Inputs and Outputs Open
I_{CCH}	Positive Power Supply			52	mA	25°C	$V_{IN} = V_{IHA}$ Note 3
I_{CCL}	Positive Power Supply			39	mA	25°C	$V_{IN} = V_{ILB}$ Note 3
V_{IHH}	Common Mode Rejection Input Voltage HIGH +1.0 V			+0.170 +o.280 +0.420	V	−55°C 25°C 125°C	
V_{ILH}	Common Mode Rejection Input Voltage LOW +1.0 V	−0.920 −0.850 −0.820			V	−55°C 25°C 125°C	
V_{IHL}	Common Mode Rejection Input Voltage HIGH −1.0 V			−1.830 −1.720 −1.580	V	−55°C 25°C 125°C	
V_{ILL}	Common Mode Rejection Input Voltage −1.0 V	−2.920 −2.850 −2.820			V	−55°C 25°C 125°C	
V_{BB}	Reference Voltage	−1.440 −1350 −1240		−1320 −1230 −1120	mV	−55°C 25°C 125°C	$V_{IN} = V_{ILB}$

NOTES:
1. Complementary Input = V_{BB}
2. One Output at a Time
3. Pin 2, 6, 10, 14 = V_{IN};
   Pin 3, 7, 11, 15 = Pin 1 (V_{BB})

SWITCHING CHARACTERISTICS: V_{EE} = −5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay, LOW to HIGH, HIGH to LOW	1.0		6.0	ns	See Figure 1
t_{TLH}, t_{THL}	Output Transition Time 1.0 V to 2.0 V, 2.0 V to 1.0 V			3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



50Ω termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin.

C_L = 25 pF, including fixture

One input from each gate must be tied to V_{BB} during testing.

PROPAGATION DELAY

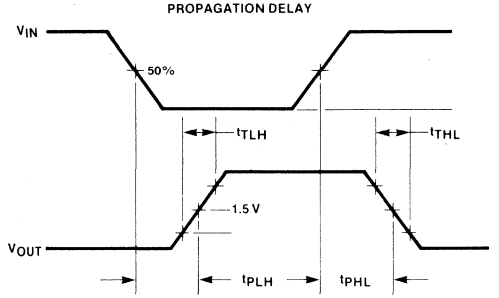


Fig. 1

F10130 • F10530
DUAL D LATCH

DESCRIPTION – The F10130/F10530 contains a pair of D type latches with a Common Enable ($\overline{E}_C$) input. Each latch has its own Enable ($\overline{E}_n$), Set (S) and Reset (R) inputs. For each latch, the data present on the D input appears on the Q output when both $\overline{E}_n$ and $\overline{E}_C$ are LOW, as indicated in the truth table. As long as $\overline{E}_n$ and $\overline{E}_C$ remain LOW, the Q output follows the D input signal each time it changes. When either $\overline{E}_n$ or $\overline{E}_C$ (or both) go HIGH, the latch no longer responds to changes on the D input, but retains the last valid data present at D before $\overline{E}_n$ or $\overline{E}_C$ go HIGH. The two latches can be strobed individually by using the $\overline{E}_n$ inputs, or simultaneously by using the $\overline{E}_C$ input.

The Set and Reset inputs are effective only if $\overline{E}_n$ or $\overline{E}_C$ (or both) are HIGH. Note that in this mode of operation the output voltage levels of a latch are unpredictable if both the S and R signals are HIGH.

PIN NAMES

$\overline{E}_n$	Enable Inputs (Active LOW)
$\overline{E}_C$	Common Enable (Active LOW)
S_n	Set
R_n	Reset
D_n	Data Inputs
Q_n	Output
$\overline{Q}_n$	Output (Active LOW)

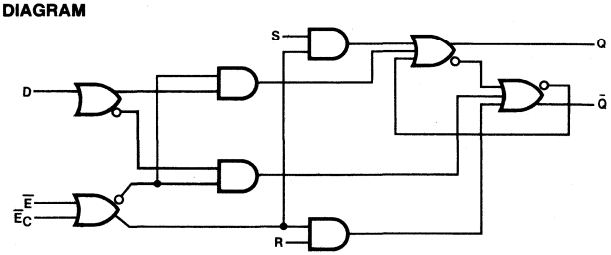
TRUTH TABLE

D	$\overline{E}_n$	$\overline{E}_C$	S	R	Q_{n+1}	OPERATION
L	L	L	X	X	L	D Function
H	L	L	X	X	H	D Function
X	H	X	L	L	Q_n	Memory
X	X	H	L	L	Q_n	Memory
X	H	X	H	L	H	Set
X	X	H	H	L	H	Set
X	H	X	L	H	L	Reset
X	X	H	L	H	L	Reset
X	H	X	H	H	-	Electrically Indeterminate
X	X	H	H	H	-	Electrically Indeterminate

L = LOW Voltage Level X = Don't Care

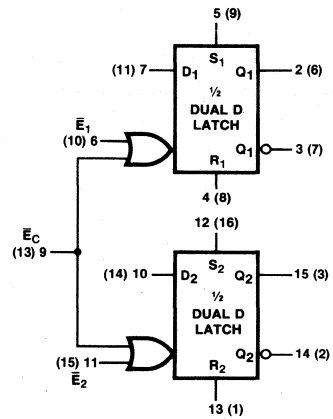
H = HIGH Voltage Level Q_n = Output

LOGIC DIAGRAM



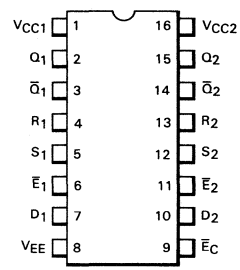
(1/2 OF CIRCUIT SHOWN)

LOGIC SYMBOL



V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)



7

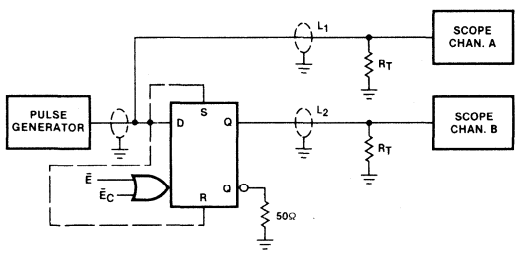
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH				μA	25°C	$V_{IN} = V_{IHA}$
	$\overline{E}_n$			220			
	$\overline{E}_C$			265			
	D_n			285			
	S_n and R_n			285			
I_{EE}	Power Supply Current	−35	−25		mA	25°C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	1.0	2.5	3.5	ns	See Figures 1, 2
t_{PLH}	Propagation Delay Set to Output	1.0	2.7	3.5	ns	See Figures 1, 3
t_{PHL}	Propagation Delay Clear to Output	1.0	2.7	3.5	ns	See Figures 1, 4
t_{TLH} t_{THL}	Output Transition Time 20% to 80%, 80% to 20%	1.5	2.5	3.5	ns	See Figures 1, 2, 3, 4
t_s	Set-up Time Data to Enable	2.5			ns	
t_h	Hold Time Data to Enable	1.5			ns	

SWITCHING CIRCUITS AND WAVEFORMS



$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V

$R_T = 50\ \Omega$ termination of scope
$L_1 = L_2$ equal 50 Ω impedance lines

Fig. 1

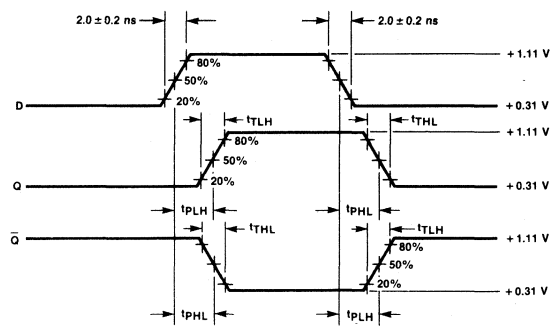


Fig. 2

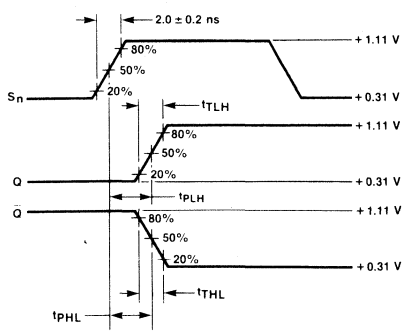


Fig. 3

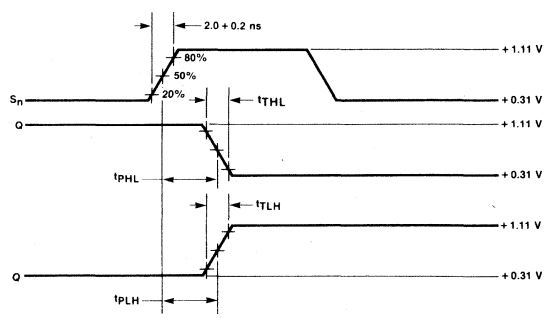


Fig. 4

F10131 • F10531
HIGH SPEED DUAL D FLIP-FLOP

DESCRIPTION – The F10131/F10531 contains two master/slave D-type flip-flops. The internal clock is the OR of two clock inputs, one common to both flip-flops. The OR clock permits the use of one input as a clock pulse and the other as an active LOW enable. While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times.

Each flip-flop has separate set and clear inputs which asynchronously determine the state of the output independent of the clock levels. Note that the output voltage levels of a flip-flop are unpredictable if both set and clear signals are HIGH.

PIN NAMES

D_n	Data Input to Master
CP_n	Clock Input
CP_C	Common Clock Input
Q_n	Output
$\overline{Q}_n$	Complement Output
S_D	Set Direct Input
C_D	Clear Direct Input

TRUTH TABLES

SYNCHRONOUS OPERATION
D TABLE

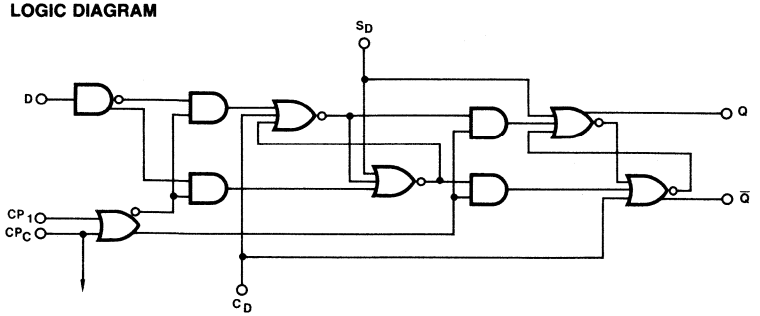
D	$Q_{(t+1)}$
L	L
H	H
$S_D = C_D$ = LOW	

$(t+1)$ = Time after positive going clock transition

ASYNCHRONOUS OPERATION
S_D C_D TABLE

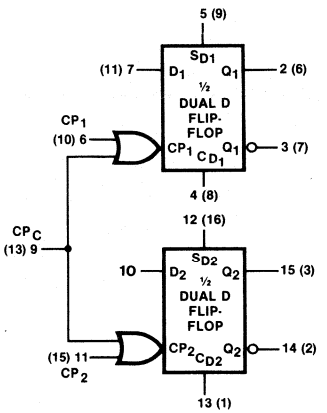
C_D	S_D	Q	$\overline{Q}$
L	L	See D Table	See D Table
L	H	H	L
H	L	L	H
H	H	undetermined	

LOGIC DIAGRAM



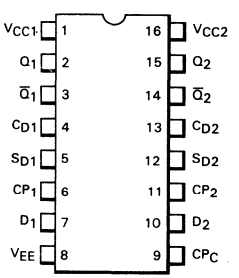
Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays, as many gate functions are achieved internally without incurring a full gate delay.

LOGIC SYMBOL



V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)



7

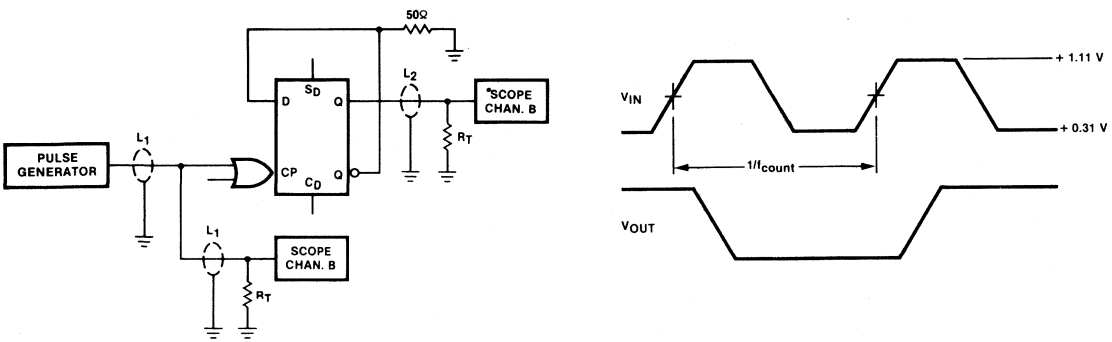
DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH				μA	25°C	$V_{IN} = V_{IHA}$
	CP			220			
	C_{CP}			265			
	D			245			
	S_D & C_D			330			
I_{EE}	Supply Current	−56	−45		mA	25°C	Inputs Open

SWITCHING CHARACTERISTICS: T_A = 25°C, V_{EE} = −5.2V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
f_{count}	Toggle Frequency	125	160		MHz	See Figure 1
t_{PHL}, t_{PLH}	Propagation Delay, Clock to Output	1.5	3.0	4.5	ns	See Figure 2
t_{PLH} t_{PHL}	Propagation Delay, SET, CLEAR to $\overline{Q}$, Q	1.2	2.2	4.3	ns	
t_{TLH}, t_{THL}	Transition Time 20% to 80%, 80% to 20%	1.5	2.2	4.5	ns	
t_s	Set-up Time Data to Clock	2.5	0.5		ns	
t_h	Hold Time Data to Clock	1.5	−0.5		ns	

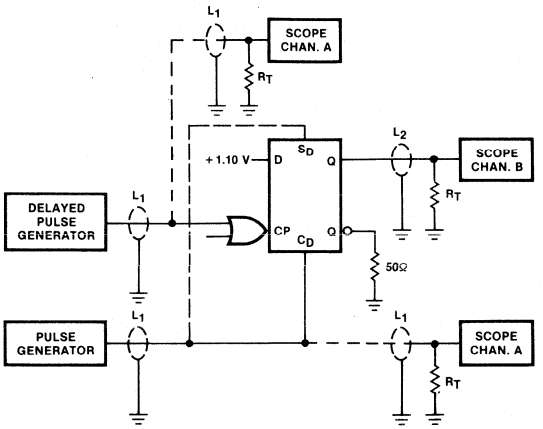
SWITCHING CIRCUITS AND WAVEFORMS



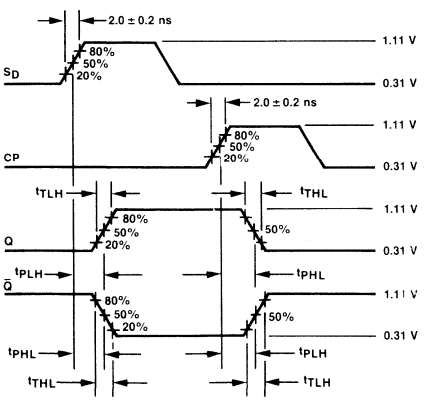
$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\ \Omega$ termination of scope
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}

Fig. 1. Toggle Rate Test Circuit

SWITCHING CIRCUITS AND WAVEFORMS (Cont'd)



$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\ \Omega$ termination of scope
$L_1 = L_2$ equal 50 Ω impedance lines
All input transition times are 2 ±0.2 ns



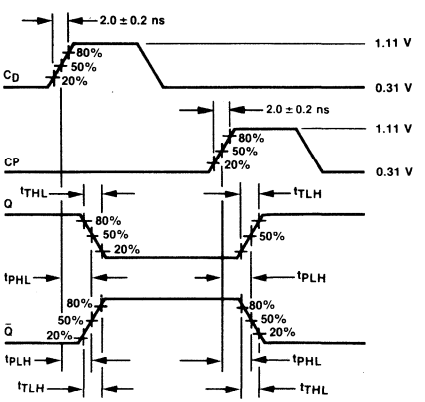


Fig. 2. Propagation Delay and C_D and S_D Test Circuit.

F10132 • F10532
DUAL MULTIPLEXER/LATCH

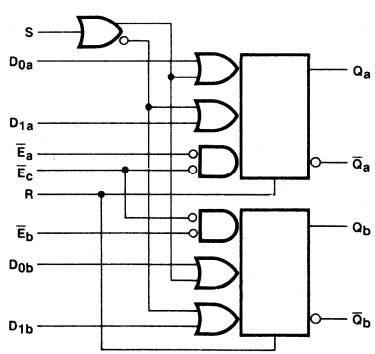
DESCRIPTION — The F10132 and F10532 are dual multiplexers with D type latches and have common Data Select and Reset inputs. Each latch may be enabled separately by holding the Common Enable ($\overline{E}_C$) in the LOW state or by using the Enable ($\overline{E}_n$) inputs. If the Common Enable is used to enable the latch, the $\overline{E}_n$ inputs must be in the LOW state. In this mode, the $\overline{E}_n$ inputs perform the function of controlling $\overline{E}_C$.

The Data Select (S) input determines which Data input is enabled. A HIGH input enables Data inputs D_{1a} and D_{1b} and a LOW input enables Data inputs D_{0a} and D_{0b}. Any change on the Data input appears at the outputs while the Enable is LOW. The outputs are latched on the positive transition of the enable. While the Enable is in the HIGH state, a change in the information present at the Data inputs does not affect the output information. Reset input is enabled when $\overline{E}_C$ or both $\overline{E}_a$ and $\overline{E}_b$ are in the HIGH state.

PIN NAMES

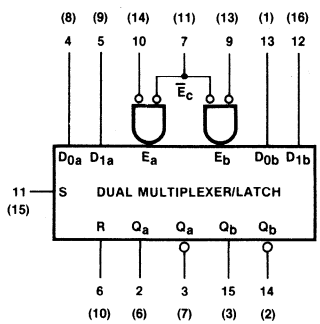
S	Data Select
D_n	Data Input
$\overline{E}_n$	Enable Inputs (Active LOW)
$\overline{E}_C$	Common Enable (Active LOW)
R	Reset
Q_n	Output
$\overline{Q}_n$	Output (Active LOW)

LOGIC DIAGRAM



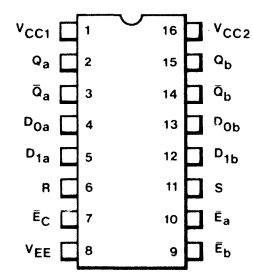
Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

LOGIC SYMBOL



V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



TRUTH TABLE

R	D	$\overline{E}_C$	$\overline{E}_n$	Q_{n+1}
L	L	L	L	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	H	Q_n
L	H	L	L	H
L	H	L	H	Q_n
L	H	L	H	Q_n
L	H	H	H	Q_n
H	X	X	H	L

L = LOW Logic Level
H = HIGH Logic Level
X = Don't Care

$D = (\overline{S} \bullet D_{0a}) + (S \bullet D_{1a})$

DC CHARACTERISTICS: $V_{EE} = -5.2$ V, V_{CC} = GND

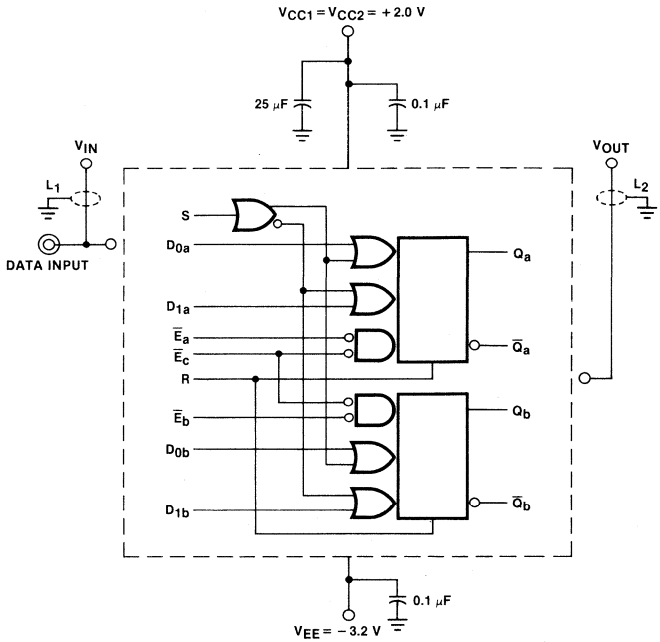
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH				μA	25°C	$V_{IN} = V_{IHA}$
	Select and Enable			265			
	Data and Common Enable			290			
	Reset			390			
I_{EE}	Power Supply Current	−55			mA	25°C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

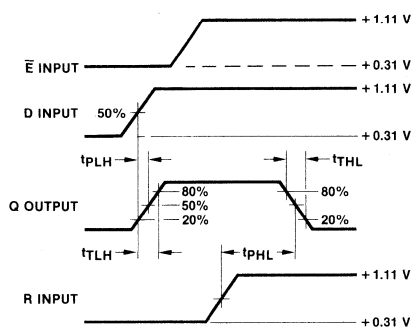
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay Enable to Output	1.0	4.5	5.7	ns	
t_{PHL}, t_{PLH}	Propagation Delay Select to Output	1.0	3.7	4.6	ns	
t_{PLH}, t_{PHL}	Propagation Delay Data to Output	1.0	3.5	3.3	ns	
t_{PHL}, t_{PLH}	Propagation Delay Reset to Output	1.0	2.5	3.8	ns	
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.5	2.0	3.5	ns	See Figure 1
t_s	Set-Up Time					
	Data	2.5	1.5		ns	
	Select	3.5	2.5			
t_h	Hold Time					
	Data	1.5	0.0		ns	
	Select	0.0	−0.5			

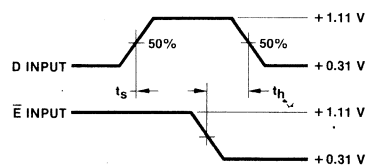
7

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω Impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V





NOTE:

t_s is the minimum time before the transition of the enable that information must be present at the data input (D).

t_h is the minimum time after the transition of the enable pulse that information must remain unchanged at the data input (D).

Fig. 1

F10133 • F10533
QUAD LATCH

DESCRIPTION — The F10133 and F10533 are high-speed low power Quad Latches consisting of four bistable latch circuits with D type inputs and gated outputs.

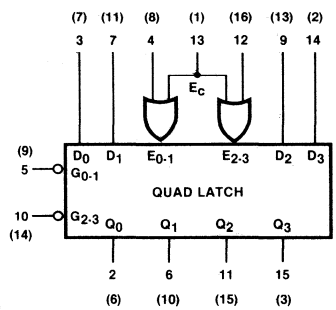
Open emitters allow a large number of outputs to be wired-OR together and latch outputs are gated, allowing direct wiring to a bus.

When either Enable is HIGH, outputs will folllow the Data inputs. Information is latched on the negative going transition of the enable.

PIN NAMES

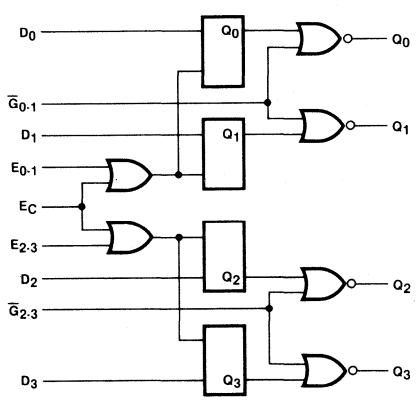
D_n	Data Input
$\overline{G}_n$	Gate Input (Active LOW)
E_n	Enable (Active HIGH)
E_C	Common Enable (Active HIGH)
Q_n	Output

LOGIC SYMBOL



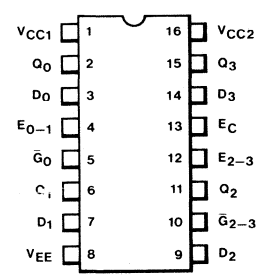
V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



TRUTH TABLE

$\overline{G}$	E	D	Q_{n+1}
H	X	X	L
L	L	X	Q_n
L	H	L	L
L	H	H	H

L = LOW Logic Level
H = HIGH Logic Level
X = Don't Care

$E = E_C + E_n$

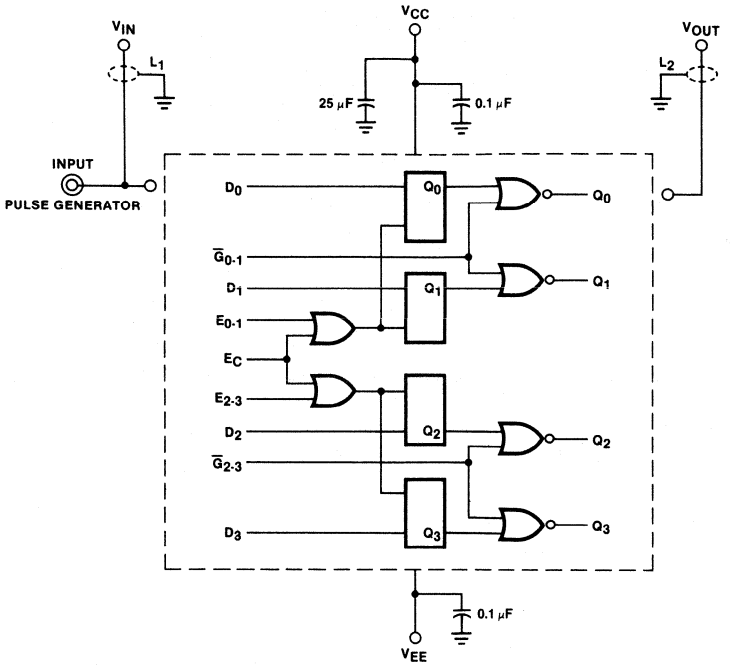
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH				μA	25°C	$V_{IN} = V_{IHA}$
	Data			245			
	Common Enable			265			
	Gate and Enable			350			
I_{EE}	Power Supply Current	−75			mA	25°C	Inputs and Outputs Open

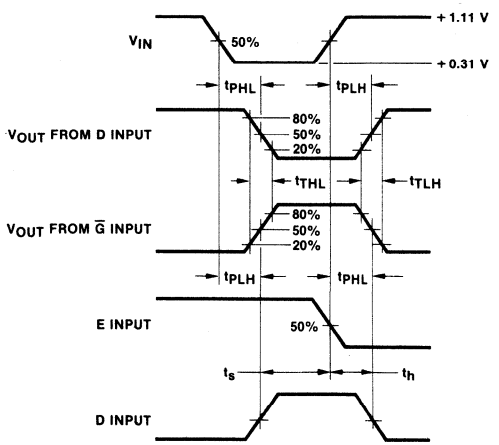
SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay Enable to Output	1.0	4.0	5.4	ns	See Figure 1
t_{PLH}, t_{PHL}	Propagation Delay Data to Output	1.0	4.0	5.4	ns	
t_{PHL}, t_{PLH}	Propagation Delay Gate to Output	1.0	2.0	3.1	ns	
t_{THL} t_{TLH},	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.5	2.0	3.5	ns	
t_s	Set-Up Time Data	2.5	0.7		ns	
t_h	Hold Time Data	1.5	0.7		ns	

SWITCHING TEST CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω Termination of scope C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V



t_s is the minimum time before the negative transition of the enable pulse (E) that information must be present at the data input (D).

t_h is the minimum time after the negative transition of the enable pulse (E) that information must remain unchanged at the data input (D).

Fig. 1

F10134 • F10534
DUAL MULTIPLEXER/LATCH

DESCRIPTION — The F10134 and F10534 are Dual Multiplexers with D type latches. Each latch may be enabled separately by holding the Common Enable in the LOW state and using the Enable ($\overline{E}_n$) inputs. If the Common Enable ($\overline{E}_C$) is used to enable the latch, the $\overline{E}_n$ inputs must be in the LOW state. In this mode, the Enable inputs perform the function of controlling the Common Enable.

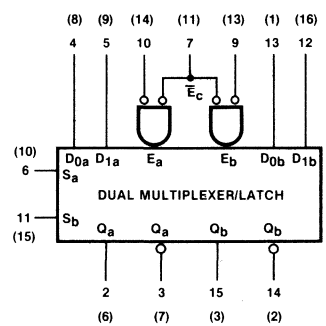
The Data Select inputs determine which Data input is enabled, as indicated in the Truth Table and Logic Diagram.

Any change on the Data input is reflected at the outputs while the Enable is LOW. The outputs are latched on the positive transition of the Enable. While the Enable is in the HIGH state, a change in the information present at the Data inputs does not affect the output information.

PIN NAMES

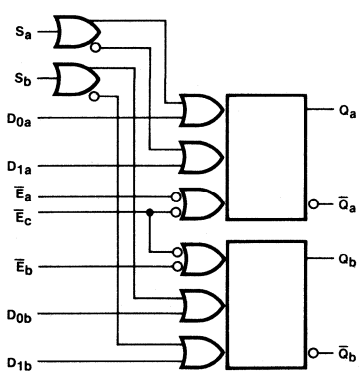
S_n	Data Select
D_n	Data Inputs
$\overline{E}_n$	Enable (Active LOW)
$\overline{E}_C$	Common Enable (Active LOW)
Q_n	Outputs
$\overline{Q}_n$	Outputs (Active LOW)

LOGIC SYMBOL



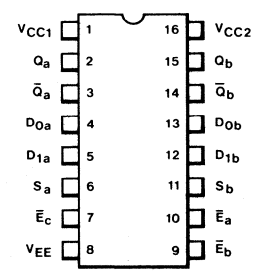
V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



TRUTH TABLE

$\overline{E}$	S_a	D_{0a}	Q_{n+1}	
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Q_n

$\overline{E} = \overline{E}_n + \overline{E}_c$
L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

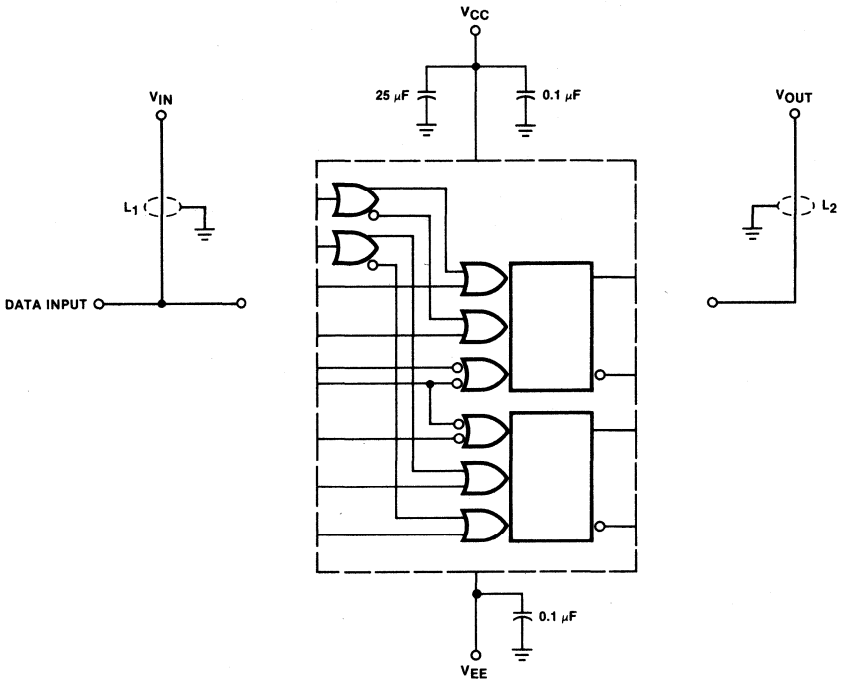
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH				μA	25°C	$V_{IN} = V_{IHA}$
	Enable			265			
	Select			265			
	Data and Common Enable			290			
I_{EE}	Power Supply Current	−55			mA	25°C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

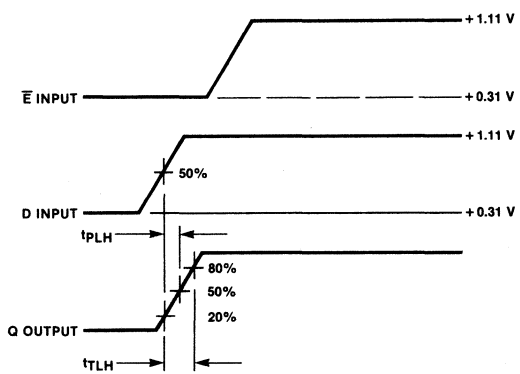
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay Enable to Output	1.0	4.5	5.7	ns	See Figure 1
t_{PLH}, t_{PHL}	Propagation Delay Data to Output	1.0	3.0	3.3	ns	
t_{PHL}, t_{PLH}	Propagation Delay Select to Output	1.0	3.7	4.6	ns	
t_{THL}, t_{TLH}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.5	2.0	3.5	ns	
t_s	Set-Up Time					
	Data	2.5	1.5		ns	
	Select	3.5	2.5			
t_h	Hold Time					
	Data	1.5	0.0		ns	
	Select	1.0	−0.5			

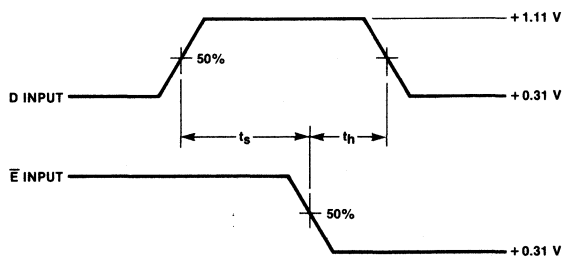
7

SWITCHING TEST CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V





NOTE:

t_s is the minimum time before the positive transition of the enable that information must be present at the data input (D).

t_h is the minimum time after the positive transition of the enable pulse that information must remain unchanged at the data input (D).

Fig. 1

F10135 • F10535

F10K VOLTAGE COMPENSATED ECL

DUAL $\overline{JK}$ FLIP-FLOP

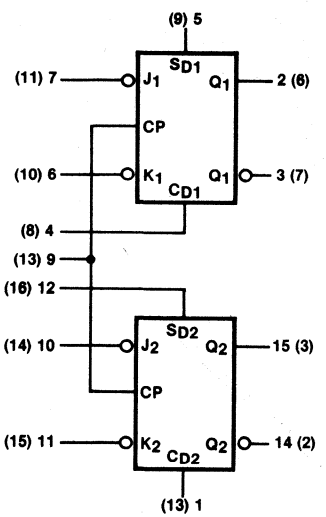
DESCRIPTION – The F10135 and F10535 are Dual Master/Slave DC Coupled Flip-Flop. Asynchronous Clear Direct (C_D) and Set Direct (S_D) are provided and override the clock. The output states of each flip-flop change on the LOW to HIGH transition of the common clock. When the clock is in a steady state (HIGH or LOW), it does not affect the output state.

- **VOLTAGE COMPENSATED . . . NOISE MARGIN INSENSITIVE TO POWER SUPPLY VARIATIONS AND TRANSIENTS, RELAXED POWER SUPPLY REQUIREMENTS**
- **INTERNAL 50 kΩ (NOMINAL) INPUT PULL DOWN RESISTORS . . . UNUSED INPUTS MAY BE LEFT OPEN**
- **OPEN EMITTER-FOLLOWER OUTPUTS DRIVE TERMINATED LINES**
- **SEPARATE V_{CC} PINS ELIMINATE NOISE COUPLING**
- **SINGLE V_{EE} POWER SUPPLY . . . −4.7 TO −6.2 V**
- **COMPLEMENTARY, SIMULTANEOUS OUTPUTS**
- **FULLY COMPATIBLE WITH OTHER 10,000 SERIES ECL**

PIN NAMES

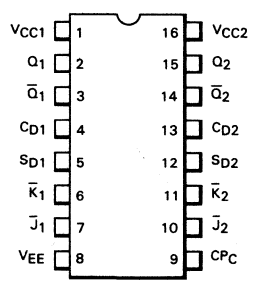
CP_C	Common Clock Input
$\overline{J}_n$	J Input
$\overline{K}_n$	K Input
S_{Dn}	Set Direct Input
C_{Dn}	Clear Direct Input
Q_n	Output
$\overline{Q}_n$	Complement Output

LOGIC SYMBOL



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)



$C_D - S_D$ TRUTH TABLE

C_D	S_D	Q_{t+}
L	L	Q_t
L	H	H
H	L	L
H	H	ND

ND = Not Defined

CLOCKED $\overline{JK}$ TRUTH TABLE

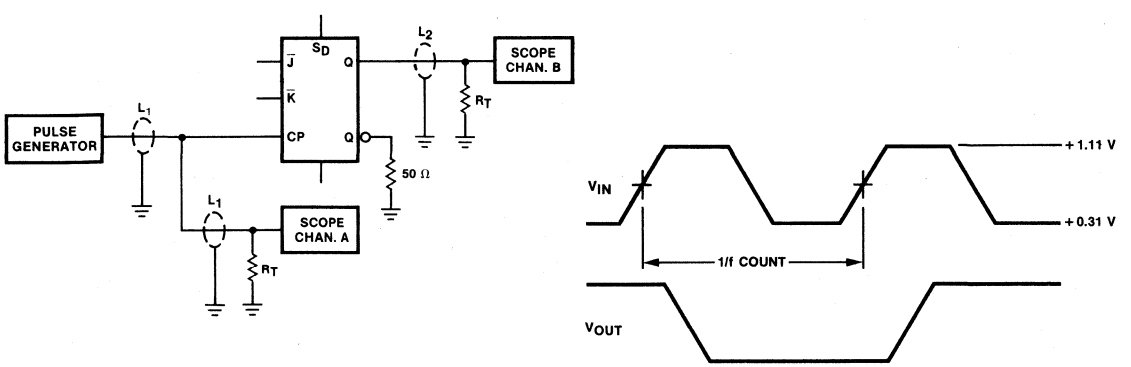
$\overline{J}$	$\overline{K}$	Q_{t+1}
L	L	Q_t
H	L	L
L	H	H
H	H	Q_t

DC CHARACTERISTICS: $V_{EE} = -5.2$ V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH CP_C, $\overline{J}$, $\overline{K}$ S_D & C_D			265 390	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−68	−45		mA	25°C	Inputs and Outputs Open

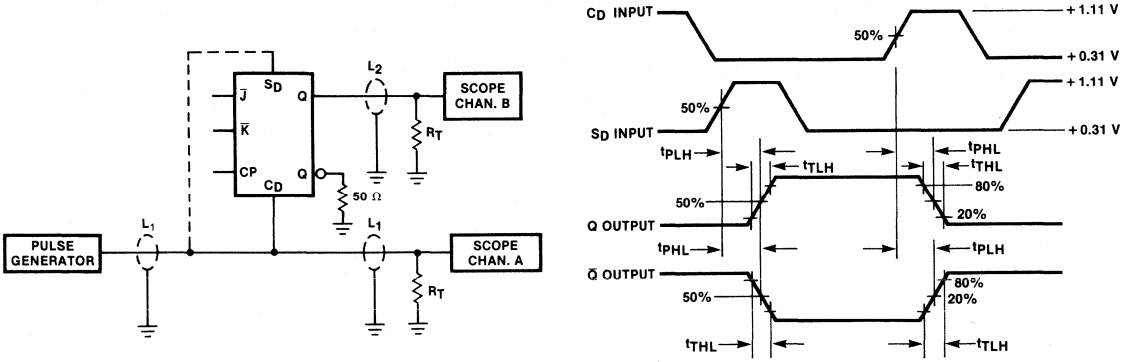
SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
f_{COUNT}	Toggle Frequency	125	200		MHz	See Figure 1
t_{PLH}, t_{PHL}	Propagation Delay Clock to Output	1.5	3.0	4.5	ns	See Figure 2
t_{PLH}, t_{PHL}	Propagation Delay S_D, C_D to $\overline{Q}$, S_D, C_D to Q	1.2	3.0	5.0	ns	
t_{TLH}, t_{THL}	Output Transition Time (20% to 80%) (80% to 20%)	1.5	2.2	3.3	ns	
t_s	Set-up Time	2.5			ns	See Figure 3
t_h	Hold Time	1.5			ns	



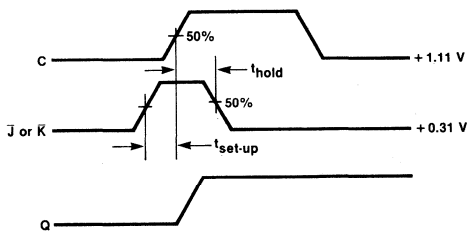
$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\ \Omega$ termination of scope
Decoupling 0.1 μF (leadless) from GND to V_{EE} and V_{CC}

Fig. 1 Toggle Rate Test Circuit



$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\ \Omega$ termination of scope
$L_1 = L_2$ equal 50 Ω impedance lines
All input transition times are 2 ± 0.2 ns
Decoupling 0.1 μF (leadless) from GND to V_{EE} and V_{CC}

Fig. 2 Propagation Delay, C_D and S_D Test Circuit



NOTE:

$t_{set\text{-}up}$ is the minimum time before the positive transition of the clock pulse (C) that information must be present at the inputs $\overline{J}$ or $\overline{K}$.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the inputs $\overline{J}$ or $\overline{K}$.

Fig. 3 Set-up and Hold Time Test Waveform

F10136 • F10536 • F10137 • F10537

4-STAGE UP/DOWN COUNTERS

F10K VOLTAGE COMPENSATED ECL

DESCRIPTION – The F10136/F10536 and F10137/F10537 are 4-stage synchronous counters capable of operating at typical count rates of 250 MHz. The circuits are designed to operate in count up, count down, hold, and preset modes, as determined by signals applied to select inputs S_1 and S_2. The F10136 is a modulo-16 binary counter and the F10137 is a BCD (8421) decade counter.

All operations are synchronous and state changes are initiated by the rising edge of the clock. Each circuit has an active LOW Count Enable ($\overline{CE}$) input and an active LOW Terminal Count ($\overline{TC}$) output which allow two or more counters to be cascaded without extra logic. The preset feature makes it possible to use the F10136 and F10137 as programmable counters in a broad variety of applications.

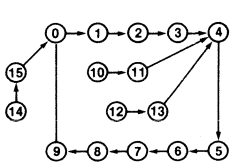
- **HIGH SPEED . . . 250 MHz TYPICAL COUNT RATE**
- **FULLY SYNCHRONOUS**
- **RIPPLE CARRY SIMPLIFIES CASCADING**
- **PRESETTABLE, FOR VARIABLE MODULUS APPLICATIONS**
- **SELECT INPUTS CAN BE WIRED TO V_{CC}**
- **50 Ω LINE DRIVING CAPABILITY**
- **SEPARATE V_{CC} PINS ELIMINATE NOISE COUPLING**
- **INTERNAL 50 kΩ INPUT PULL-DOWN RESISTORS . . . UNUSED INPUTS CAN BE LEFT OPEN**

PIN NAMES

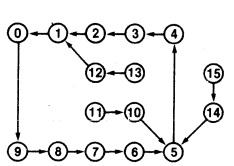
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Positive-Going Active Edge)
P_n	Preset Data Inputs
Q_n	Flip-flop Outputs
S_n	Operating Mode Select Inputs
$\overline{TC}$	Terminal Count Output (Active LOW)

STATE DIAGRAMS

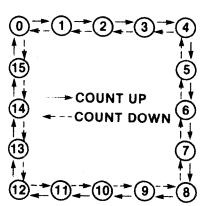
10537/10137 COUNT UP



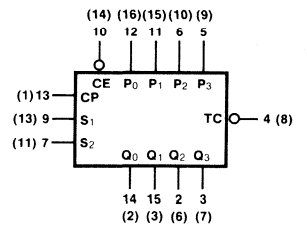
10537/10137 COUNT DOWN



10536/10136



LOGIC SYMBOL



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)

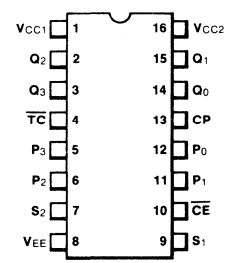
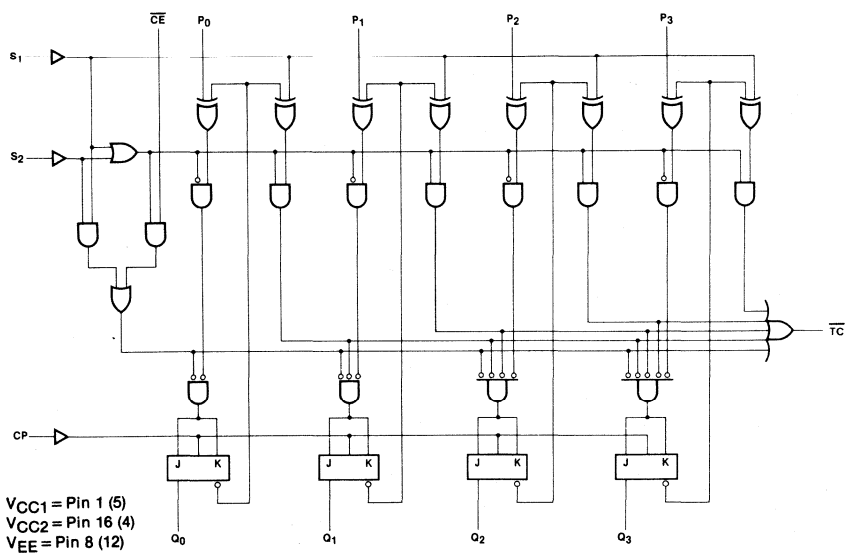


Fig. 1. Sample Operating Sequences, F10136 • F10536 Binary

INPUTS								OUTPUTS					SELECT
S_1	S_2	$\overline{CE}$	CP	P_3	P_2	P_1	P_0	Q_3	Q_2	Q_1	Q_0	$\overline{TC}$	MODE
L	L	X	⎍	H	L	H	H	H	L	H	H	L	PRESET*
L	H	L	⎍	X	X	X	X	H	H	L	L	H	COUNT
L	H	L	⎍	X	X	X	X	H	H	L	H	H	UP
L	H	L	⎍	X	X	X	X	H	H	H	L	H	
L	H	L	⎍	X	X	X	X	H	H	H	H	L	(Max)
L	H	H	X	X	X	X	X	H	H	H	H	H	($\overline{CE}$ Inhibit)
L	H	L	⎍	X	X	X	X	L	L	L	L	H	
L	H	L	⎍	X	X	X	X	L	L	L	H	H	
H	H	X	X	X	X	X	X	L	L	L	H	H	HOLD
L	L	X	⎍	L	H	L	L	L	H	L	L	L	PRESET*
H	L	L	⎍	X	X	X	X	L	L	H	H	H	COUNT
H	L	L	⎍	X	X	X	X	L	L	H	L	H	DOWN
H	L	L	⎍	X	X	X	X	L	L	L	H	H	
H	L	L	⎍	X	X	X	X	L	L	L	L	L	(Min)
H	L	L	⎍	X	X	X	X	H	H	H	H	H	
H	L	L	⎍	X	X	X	X	H	H	H	L	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
* = Starting point, arbitrary preset data

F10136/F10536 LOGIC DIAGRAM



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

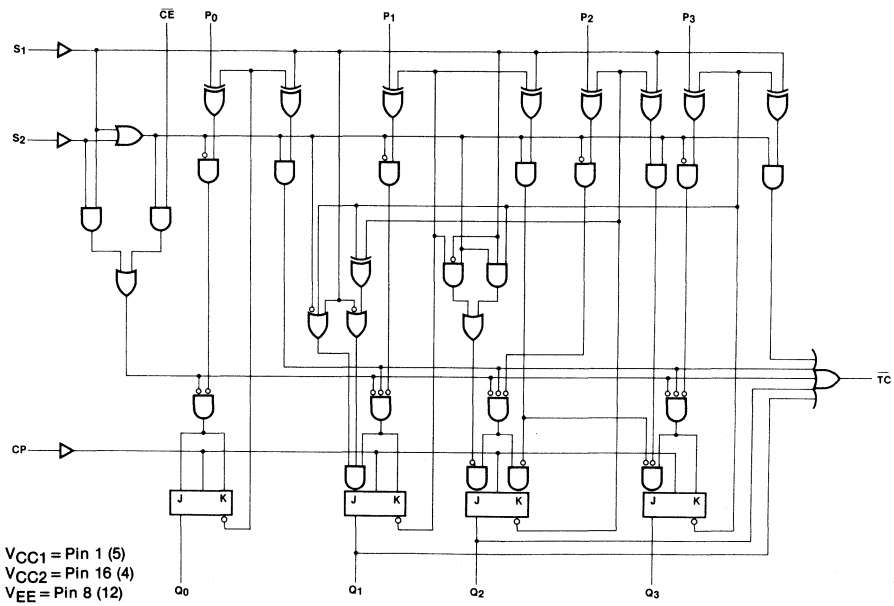
Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than indicated.

Fig. 2. Sample Operating Sequences, F10137 • F10537 Binary

INPUTS								OUTPUTS					SELECT
S_1	S_2	$\overline{CE}$	CP	P_3	P_2	P_1	P_0	Q_3	Q_2	Q_1	Q_0	$\overline{TC}$	MODE
L	L	X	⎍	L	H	L	H	L	H	L	H	H	PRESET*
L	H	L	⎍	X	X	X	X	L	H	H	L	H	COUNT
L	H	L	⎍	X	X	X	X	L	H	H	H	H	UP
L	H	L	⎍	X	X	X	X	H	L	L	L	H	
L	H	L	⎍	X	X	X	X	H	L	L	H	L	(Max)
L	H	H	X	X	X	X	X	H	L	L	H	H	($\overline{CE}$ Inhibit)
L	H	L	⎍	X	X	X	X	L	L	L	L	H	
L	H	L	⎍	X	X	X	X	L	L	H	L	H	
H	H	X	X	X	X	X	X	L	L	H	L	H	HOLD
L	L	X	⎍	L	H	L	L	L	H	L	L	H	PRESET*
H	L	L	⎍	X	X	X	X	L	L	H	H	H	COUNT
H	L	L	⎍	X	X	X	X	L	L	H	L	H	DOWN
H	L	L	⎍	X	X	X	X	L	L	L	H	H	
H	L	L	⎍	X	X	X	X	L	L	L	L	L	(Min)
H	L	L	⎍	X	X	X	X	H	L	L	H	H	
H	L	L	⎍	X	X	X	X	H	L	L	L	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
* = Starting point, arbitrary data

F10137/F10537 LOGIC DIAGRAM



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than indicated.

FUNCTIONAL DESCRIPTION—In the counting modes, the F10136 follows a straightforward binary sequence. The F10137 follows the 8421 BCD sequence, as indicated in the state diagrams on page 1. For either circuit type, the $\overline{CE}$ input must be LOW for counting to occur, as indicated in the sample sequences of *Figures 1* and *2*.

The Select inputs determine the operating mode of a circuit, as shown in the table of *Figure 3*. All operations are synchronous and state changes are initiated by the rising edge of the clock. The $\overline{CE}$ input has no effect on the preset and hold operations. Either of the Select inputs can be wired to V_{CC}; this simplifies designs in which S_1 or S_2 is required to always be HIGH.

In the counting modes the $\overline{TC}$ output is controlled by the $\overline{CE}$ input and by the state of the flip-flops, as indicated in *Figure 3*. $\overline{TC}$ is normally HIGH and goes LOW (assuming $\overline{CE}$ is LOW) when the counter reaches zero in the count down mode or when it reaches maximum (15 for the 10136, 9 for the 10137) in the count up mode. The control that the $\overline{CE}$ inputs has on the $\overline{TC}$ output makes it possible to form multi-stage counters without external logic, as shown in *Figure 4*. In order for a given stage to count, the $\overline{TC}$ outputs (and thus the $\overline{CE}$ inputs) of all the preceding stages must be LOW. The frequency capability of this arrangement is limited by the time required for a negative-going $\overline{TC}$ signal from the first stage to ripple through to the $\overline{CE}$ input of the last stage. The time between successive positive-going clock edges must not be less than the sum of the CP to $\overline{TC}$ delay of the first stage, the $\overline{CE}$ to $\overline{TC}$ delays of the intermediate stages, and the $\overline{CE}$ to CP set-up time of the last stage. The counter can be enabled/disabled at the $\overline{CE}$ input of the first stage (*Figure 4*), or by using the Select inputs.

In the preset mode, the $\overline{TC}$ output of the F10136 is forced LOW, while that of the F10137 depends on the state of Q_1 and Q_2, as indicated in *Figure 3*. For either circuit type, the $\overline{TC}$ output is forced HIGH in the hold mode. This feature can be used to simplify designs for certain types of applications. In the simple counter of *Figure 4*, for example, the second and subsequent stages can be prevented from counting by putting the first stage into the hold mode, causing a HIGH signal to ripple through to all $\overline{TC}$ outputs. Wiring simplification is possible if the counter is to operate in only one of the counting modes, plus preset and hold. For example, if the S_1 inputs of the second and subsequent stages are left open (LOW) and their S_2 inputs wired in parallel with S_2 of the first stage, then the S_2 signal selects either the count up or preset mode for these latter stages. Putting the first stage into the hold mode effectively achieves a hold for the entire counter in the manner previously described. Designers should bear in mind that a $\overline{TC}$ output is subject to decoding spikes and therefore should not be used as a clock.

The flip-flops are master/slave type with internal JK feedback. Information enters the master when the clock is LOW and transfers to the slave when the clock goes HIGH. Signals on the Preset, Select, and $\overline{CE}$ inputs must be in the intended state at least a set-up time before the clock rising edge. Hold times for these inputs are negative, however, which offers simplifications in some applications. *Figure 5* illustrates an arrangement for a programmable down counter using F10136 circuits. When the counter reaches the all-zeros state and the clock goes LOW, the $\overline{TC}$ outputs will go LOW, starting at the first stage and rippling through to make the S_1 inputs LOW. Thus with S_1 and S_2 LOW the circuits are in the preset mode and the preset data will be entered on the next rising clock edge. S_2 also goes HIGH (with the clock) but this does not interfere with presetting because of the negative hold time characteristic. The $\overline{CE}$ input of the first stage also goes HIGH with the presetting clock, causing the $\overline{TC}$ output to go HIGH and ripple through the second and third stages to make the S inputs HIGH. After this is accomplished the circuits are in the hold mode when the clock is HIGH and in the count down mode when the clock is LOW.

The outputs of these circuits have no internal pull-down resistors and the 50 kΩ input pull-down resistors of F10K elements do not provide sufficient current to perform the pull-down function at electronic speeds. External pull-down current is an integral function of the termination scheme selected by the system designer, as discussed in Chapter 5 of the Fairchild ECL Handbook.

Fig. 3. Mode Select and Terminal Count Equation Table

Select		Operating	Terminal Count Output Equation	
S_1	S_2	Mode	F10136 Binary	F10137 BCD
L	L	Preset	$\overline{TC} = LOW$	$\overline{TC} = Q_1 + Q_2$
L	H	Count Up	$\overline{TC} = \overline{CE} + \overline{Q_0} + \overline{Q_1} + \overline{Q_2} + \overline{Q_3}$	$\overline{TC} = \overline{CE} + \overline{Q_0} + Q_1 + Q_2 + \overline{Q_3}$
H	L	Count Down	$\overline{TC} = \overline{CE} + Q_0 + Q_1 + Q_2 + Q_3$	$\overline{TC} = \overline{CE} + Q_0 + Q_1 + Q_2 + Q_3$
H	H	Hold	$\overline{TC} = HIGH$	$\overline{TC} = HIGH$

DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH				μA	25°C	$V_{IN} = V_{IHA}$
	P_n			220			
	S_2			265			
	CP			290			
	S_1, $\overline{CE}$			245			
I_{EE}	Power Supply Current	−135	−105		mA	25°C	Outputs Open, Pin 12 tied to V_{IH}

AC CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	TEST CONDITIONS
f_{count}	Count Frequency	125	250		MHz	See Figure 6
t_{PLH} t_{PHL}	Propagation Delay, Clock to Q_n	1.0	2.2	4.5	ns	
t_{PHL} t_{PLH}	Propagation Delay, Clock to $\overline{TC}$		4.5		ns	
t_{PHL} t_{PLH}	Propagation Delay, $\overline{CE}$ to $\overline{TC}$	1.6	3.5	6.9	ns	
t_{TLH} t_{THL}	Output Transition Time LOW-to-HIGH, HIGH-to-LOW (20% to 80%), (80% to 20%)	1.1	2.0	3.3	ns	
t_s	Set-Up Time Prior to Clock				ns	
	Data		2.0			
	Select		4.0			
	$\overline{CE}$ (to Enable Count)		2.7			
	$\overline{CE}$ (to Inhibit Count)		1.2			
t_h	Hold Time After Clock				ns	
	Data		−2.0			
	Select		−4.0			
	$\overline{CE}$ (to Enable Count)		−1.0			
	$\overline{CE}$ (to Inhibit Count)		−2.5			

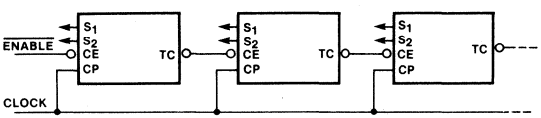


Fig. 4 Multi-Stage Counter Using Ripple Carry

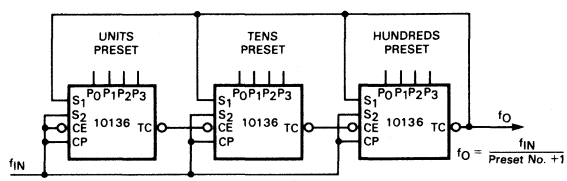
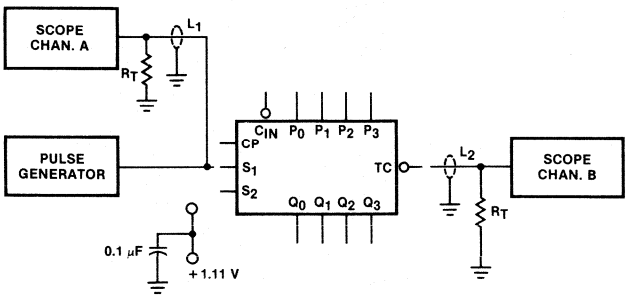
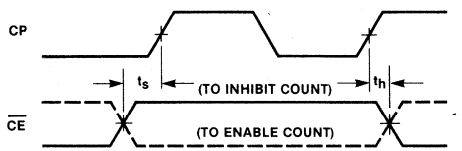
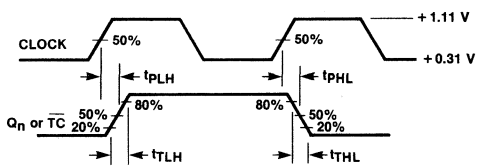


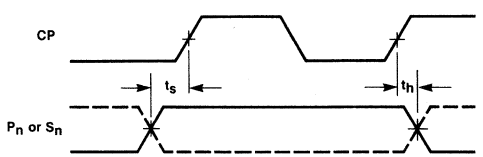
Fig. 5 Programmable Down Counter

SWITCHING CIRCUIT AND WAVEFORMS









L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 6

F10141 • F10541

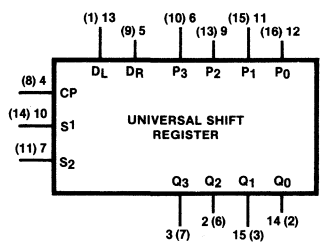
UNIVERSAL SHIFT REGISTER

F10K VOLTAGE COMPENSATED ECL

DESCRIPTION – The F10141/F10541 contains four clocked D type flip-flops with individual inputs and outputs for parallel operations, and with serial inputs and steering logic for bidirectional shifting. The flip-flops accept input data a set-up time before the positive-going transition of the clock and their outputs start to change (if required) after this rising clock edge.

The circuit operating mode is determined by Select inputs S_1 and S_2, which are internally decoded to select either Parallel Entry, Hold, Shift Left, or Shift Right operation. The circuit can thus perform parallel in/out, serial in/out, serial-to-parallel, and parallel-to-serial operations.

LOGIC SYMBOL

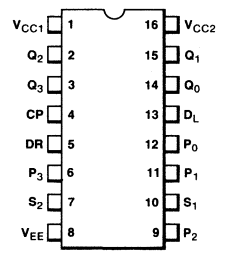


V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
() = Flatpak

PIN NAMES

D_L	Left Serial Data Input
D_R	Right Serial Data Input
P_n	Parallel Data Inputs
CP	Clock Pulse Input
S_n	Select Inputs for Operating Mode
Q_n	Outputs

CONNECTION DIAGRAM
DIP (TOP VIEW)

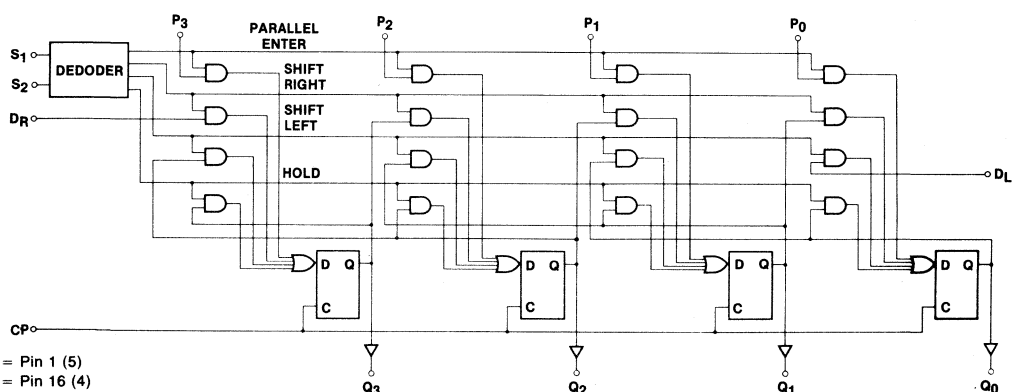


TRUTH TABLE

SELECT S_1	SELECT S_2	OPERATING MODE	OUTPUTS $Q_{0(t+1)}$	$Q_{1(t+1)}$	$Q_{2(t+1)}$	$Q_{3(t+1)}$
L	L	Parallel Entry	P_0	P_1	P_2	P_3
L	H	Shift Right	$Q_{1\,t}$	$Q_{2\,t}$	$Q_{3\,t}$	D_R
H	L	Shift Left	D_L	$Q_{0\,t}$	$Q_{1\,t}$	$Q_{2\,t}$
H	H	Hold	$Q_{0\,t}$	$Q_{1\,t}$	$Q_{2\,t}$	$Q_{3\,t}$

t and t +1 refers to the time before and after the positive-going clock edge.

LOGIC DIAGRAM



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

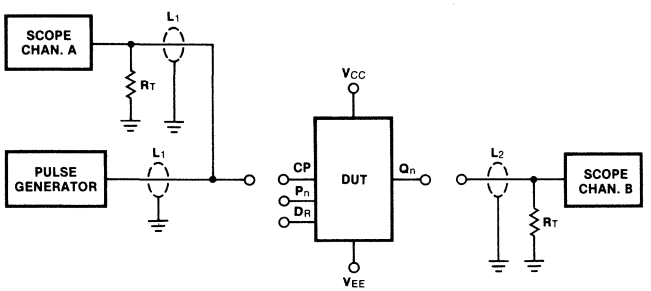
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH			220	μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	−102	−45		mA	Inputs and Outputs Open

AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -5.2 V

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL}, t_{PLH}	Propagation Delay	1.0	1.8	3.8	ns	See Figure 1
f_{SHIFT}	Max Shift Frequency	150	250		MHz	
t_{TLH}, t_{THL}	Transition Time 20% to 80%, 80% to 20%	1.5	2.0	3.3	ns	
t_s	Set-Up Time	2.5			ns	
t_h	Hold Time	1.5			ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2}$ = 2.0 V
V_{EE} = -3.2 V

SHIFT FREQUENCY TEST

1. Set D_1, D_2, D_3 = +0.31 V
   D_0 = +1.11 V
2. Apply Clock pulse V_{IH} / V_{IL} to set Q_0 HIGH
3. Maintain Clock LOW
   Set S_1 = +0.31 V
   Set S_2 = +1.11 V

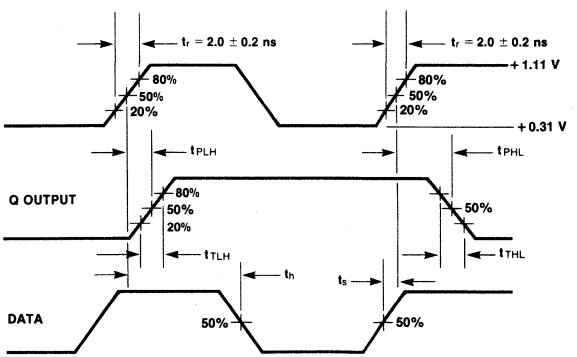


Figure 1

F10153 • F10553

F10K VOLTAGE COMPENSATED ECL

QUAD D LATCH

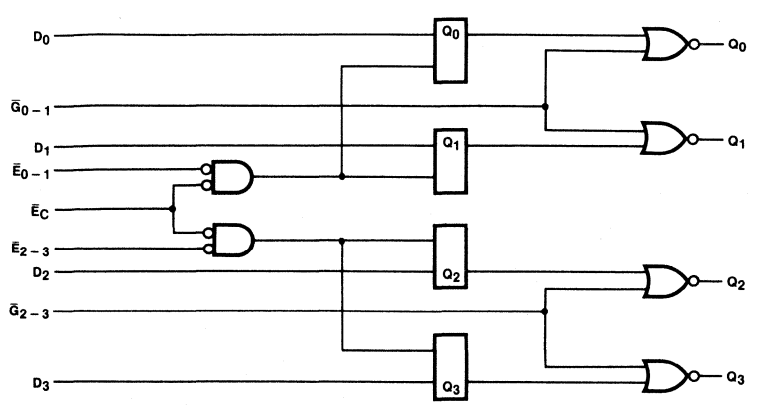
DESCRIPTION – The F10153/F10553 are high-speed Quad D Latches consisting of four bistable latch circuits with D type inputs and gated Q outputs. The gated outputs allow direct wiring to a bus. When the enable is LOW, outputs will follow the D inputs. Information is latched on the positive-going transition of the enable.

- **HIGH-SPEED . . . 4 ns TYP**
- **GATED OUTPUTS**
- **VOLTAGE COMPENSATED**
- **ENABLE IN PAIRS OR COMMON**
- **HIGH Z INPUTS**

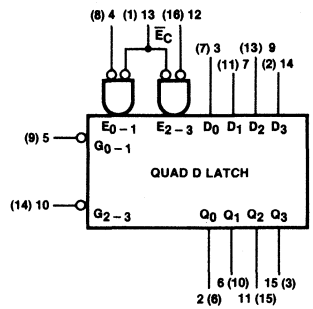
PIN NAMES

D_n	Data Inputs
$\overline{G}_n$	Gated Inputs (Active LOW)
$\overline{E}_C$	Common Enable (Active LOW)
$\overline{E}_n$	Enables (Active LOW)
Q_n	Outputs

LOGIC DIAGRAM

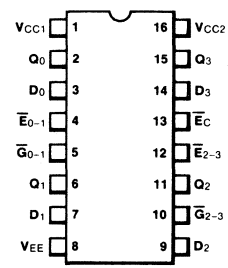


LOGIC SYMBOL



V_{CC} = Pins 1, 16 (5, 4)
V_{EE} = Pins 8 (12)
( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

$\overline{G}$	$\overline{E}$	D	Q_{t+1}
H	X	X	L
L	H	X	Q_t
L	L	L	L
L	L	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
E = E_C + E_n

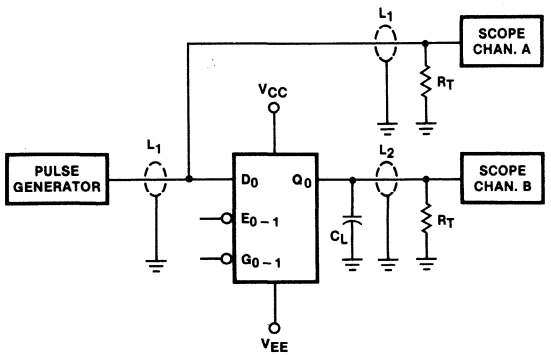
DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH D_n E_{0-1}, E_{2-3} E_C, G_n			245 265 350	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−75	−60		mA	25°C	Inputs Open

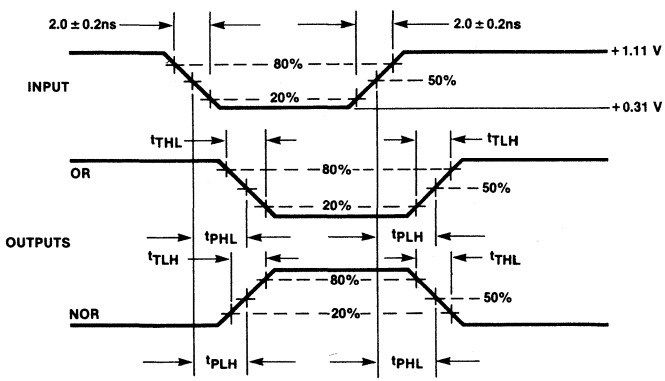
SWITCHING CHARACTERISTICS: V_{EE} = −5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay	1.0	4.0	5.4	ns	See Figure 1
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.5	2.0	3.5	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}



Jig set-up with no circuit under test
$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V

Fig.1

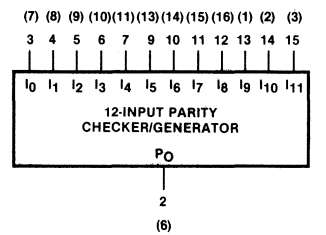
F10160 • F10560
12-BIT PARITY CHECKER/GENERATOR

DESCRIPTION — The F10160 and F10560 are 12-Input Parity Generators. The output will be HIGH when an odd number of inputs are HIGH; typical delay is 4 ns. For applications requiring fewer than 12 inputs, unused inputs may be left open, since internal input resistors hold unconnected inputs LOW.

PIN NAMES

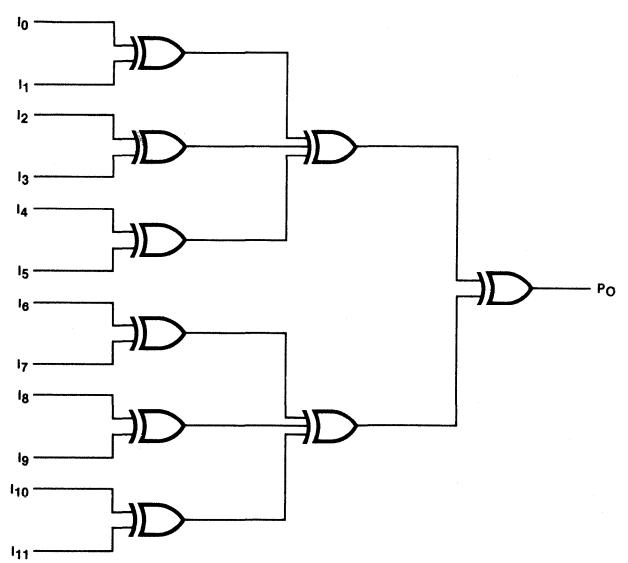
I_n	Inputs
P_O	Parity Odd

LOGIC SYMBOL

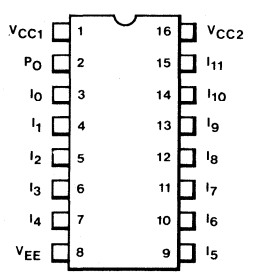


V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



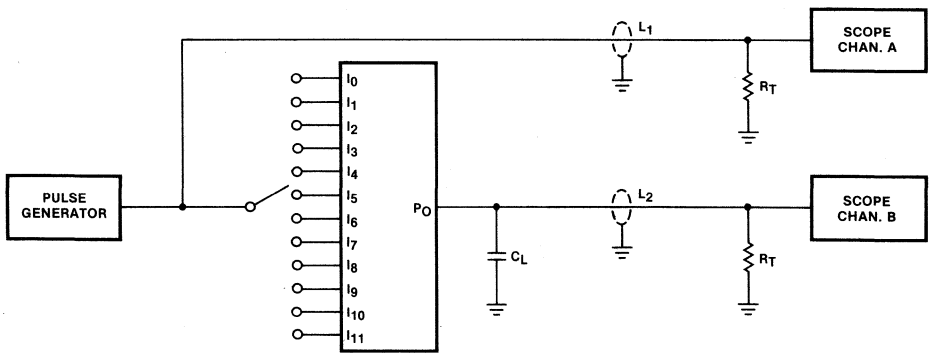
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH (All Inputs)			220	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−59	−46		mA	25°C	Inputs and Outputs Open

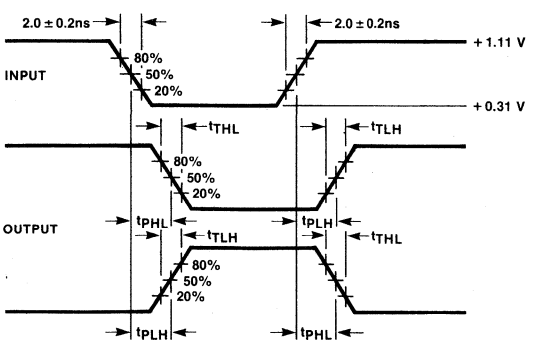
SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay, LOW to HIGH, HIGH to LOW	2.0	4.0	7.5	ns	See Figure 1
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.5	2.0	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORM



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF



Jig set-up with no circuit under test
$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V

Fig. 1.

F10161 • F10561

1-OF-8 DECODER

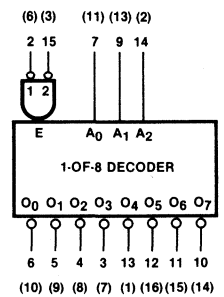
ACTIVE LOW OUTPUTS

DESCRIPTION — The F10161 and F10561 accept a 3-bit binary input and provides eight mutually exclusive outputs. The selected output will be LOW while all other outputs are HIGH. Two enable inputs force all outputs HIGH when either or both are HIGH. Typical delay is 4 ns from any address or enable to any output.

PIN NAMES

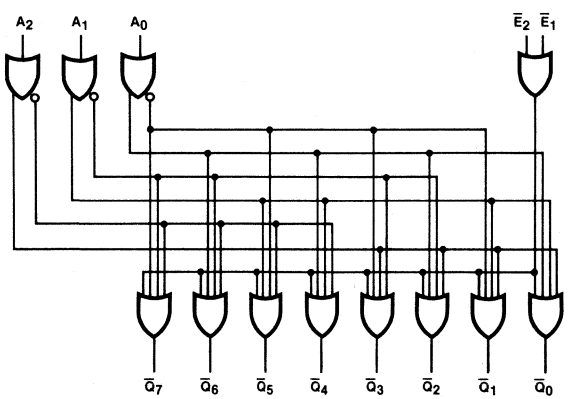
$\overline{E}_N$	Enable (Active LOW)
A_n	Address Inputs
$\overline{O}_n$	Output (Active LOW)

LOGIC SYMBOL

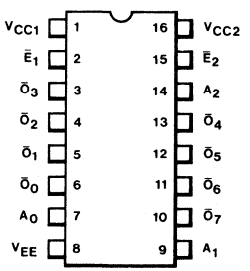


$V_{CC1} = 1$ (5)
$V_{CC2} = 16$ (4)
$V_{EE} = 8$ (12)
( ) = Flatpak

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E}_2$	$\overline{E}_1$	A_2	A_1	A_0	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	H	H	H	H	H	H	H	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

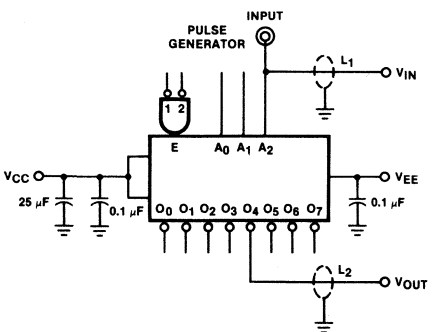
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

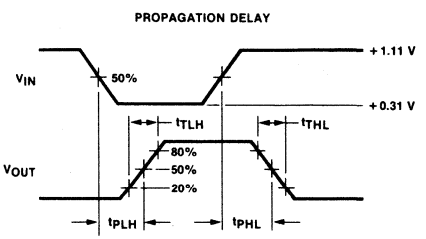
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH			220	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−76	−55		mA	25°C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay, LOW to HIGH, HIGH to LOW	1.5	4.5	6.0	ns	See Figure 1
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.5	2.0	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS





L_1 and L_2 = equal length 50 Ω impedance lines
$R_T = 50$ Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 1

F10162 • F10562

1-OF-8 DECODER

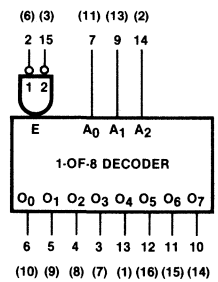
ACTIVE HIGH OUTPUTS

DESCRIPTION — The F10162 and F10562 accept a 3-bit binary input and provides eight mutually exclusive outputs. The selected output will be HIGH while all other outputs are LOW. Two enable inputs force all outputs LOW when either or both are HIGH. Typical delay is 4 ns from any address or enable to any output.

PIN NAMES

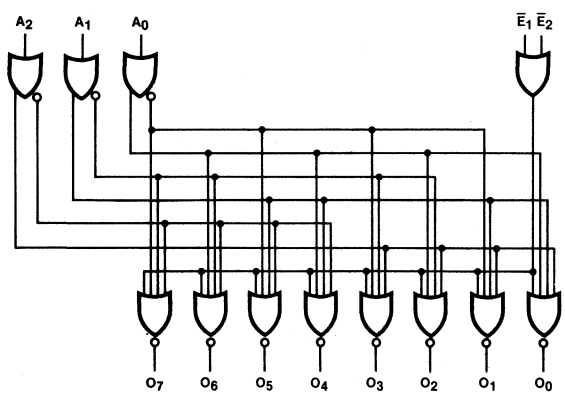
$\overline{E}_n$	Enable (Active LOW)
A_n	Address Inputs
O_n	Output (Active HIGH)

LOGIC SYMBOL

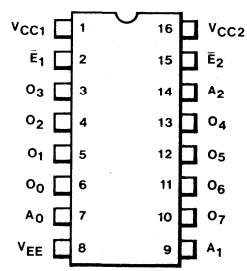


V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

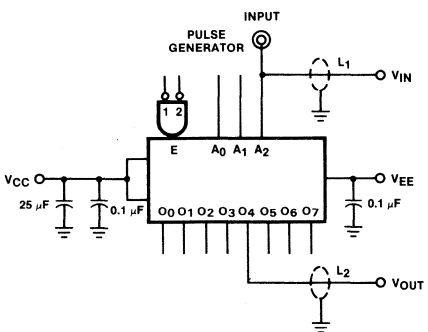
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} =$ GND

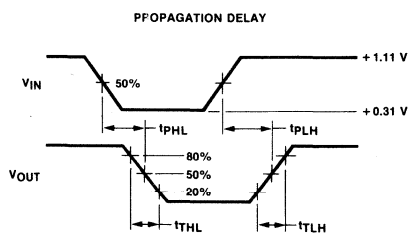
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH			220	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−76	−55		mA	25°C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay, LOW to HIGH, HIGH to LOW	1.5	4.0	6.0	ns	See Figure 1
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.5	2.0	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS





L_1 and L_2 = equal length 50 Ω impedance lines
$R_T = 50$ Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 1.

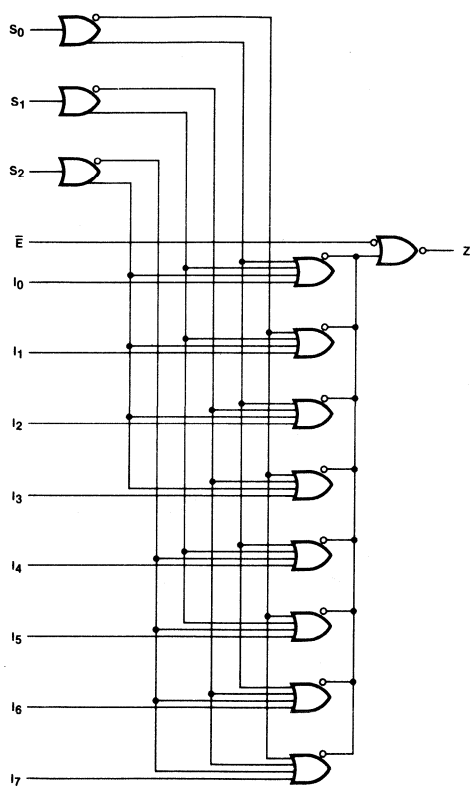
F10164 • F10564
8-INPUT MULTIPLEXER

DESCRIPTION — The F10164 and F10564 accept a 3-bit address and selects 1-of-8 inputs. The enable line, when HIGH, forces the output LOW. Typical address to output delays are 4 ns.

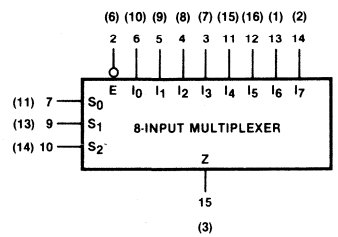
PIN NAMES

$\overline{E}$	Enable (Active LOW)
I_n	Inputs
S_n	Select Inputs
Z	Output

LOGIC DIAGRAM

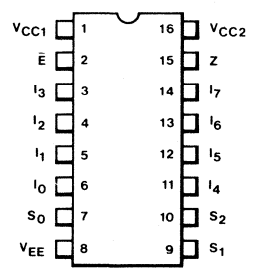


LOGIC SYMBOL



V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



TRUTH TABLE

$\overline{\text{ENABLE}}$	ADDRESS INPUTS S_2	S_1	S_0	Z
L	L	L	L	I_0
L	L	L	H	I_1
L	L	H	L	I_2
L	L	H	H	I_3
L	H	L	L	I_4
L	H	L	H	I_5
L	H	H	L	I_6
L	H	H	H	I_7
H	X	X	X	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

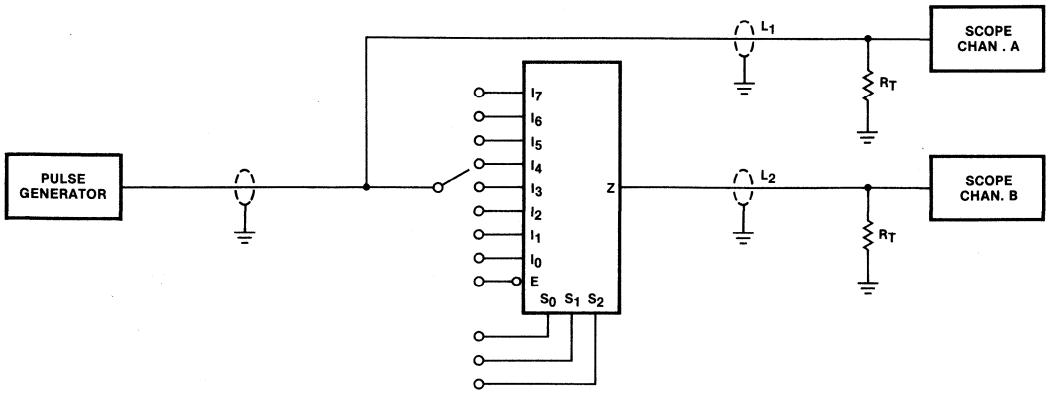
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS B	TYP	A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH (All Inputs)			265	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−75	−55		mA	25°C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	TYP	A	UNITS	CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	1.5	3.0	4.5	ns	Figure 1
t_{PLH}, t_{PHL}	Propagation Delay Address to Output	2.0	4.0	6.0	ns	
t_{PHL}	Propagation Delay Enable to Output	1.0	2.0	2.9	ns	
t_{THL}, t_{TLH}	Output Transition Time HIGH to LOW, LOW to HIGH	1.5	2.0	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORM



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

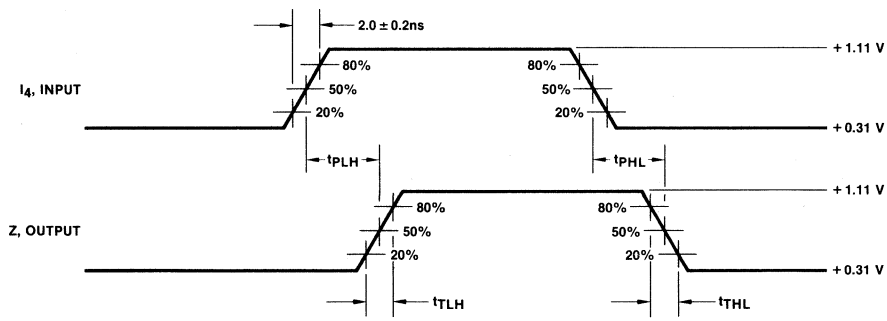


Fig. 1

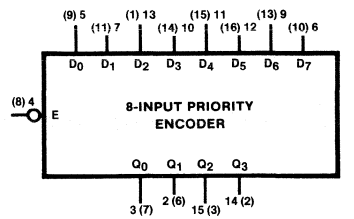
F10565• F10165

8-INPUT PRIORITY ENCODER
F10K VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION – The F10165/F10565 are 8-Input Priority Encoders with output latches. The inputs are preassigned an order of priority, with D_0 having the highest priority and D_7 the lowest. Outputs Q_2, Q_1, Q_0 constitute a binary code identifying the highest order input on which a HIGH signal is present. Output Q_3 is HIGH when any D_n input is HIGH, and thus constitutes a group signal useful for expansion with other encoders when more than eight inputs are involved.

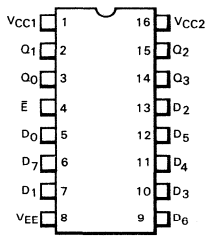
When the Common Enable ($\overline{E}$) input is LOW, the outputs will change in response to input changes. The outputs latch on the positive transition of $\overline{E}$ and are not affected by subsequent data changes. The F10165 is useful in a variety of applications involving groups of terminals, peripherals, sensors, status signals, or control functions requiring a system response according to an established precedence.

LOGIC SYMBOL



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)

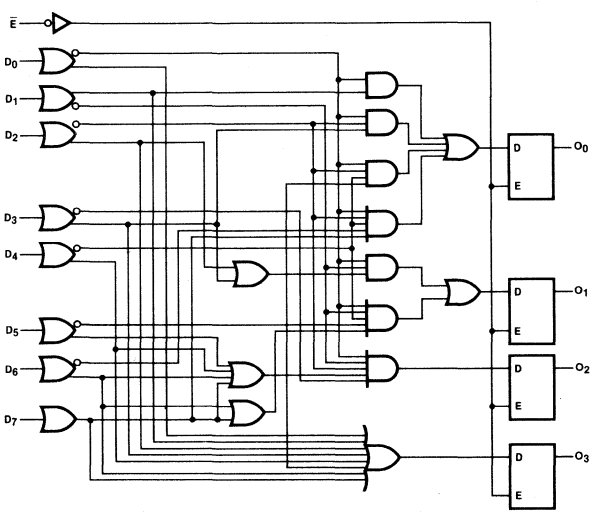


- **FULLY COMPATIBLE WITH OTHER 10,000 SERIES ECL**
- **VOLTAGE COMPENSATED—INSENSITIVE TO POWER SUPPLY VARIATIONS AND TRANSIENTS**
- **OPEN EMITTER-FOLLOWER OUTPUTS**
- **SEPARATE V_{CC} LEADS TO ELIMINATE NOISE COUPLING**
- **INTERNAL 50 kΩ (NOMINAL) INPUT PULL-DOWN RESISTORS—UNUSED INPUTS MAY BE LEFT OPEN**

PIN NAMES

D_n	Data Inputs
Q_n	Outputs
$\overline{E}$	Common Enable

LOGIC DIAGRAM



TRUTH TABLE

INPUTS								OUTPUTS			
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q_3	Q_2	Q_1	Q_0
H	X	X	X	X	X	X	X	H	L	L	L
L	H	X	X	X	X	X	X	H	L	L	H
L	L	H	X	X	X	X	X	H	L	H	L
L	L	L	H	X	X	X	X	H	L	H	H
L	L	L	L	H	X	X	X	H	H	L	L
L	L	L	L	L	H	X	X	H	H	L	H
L	L	L	L	L	L	H	X	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

7

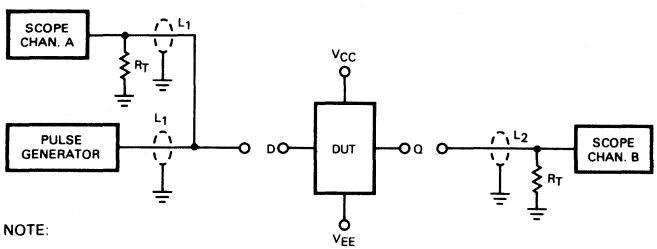
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
I_{IH}	Input Current HIGH Data Inputs Enable Inputs			 220 245	μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	−131	−100		mA	Inputs and Outputs Open

AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -5.2 V

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay, Enable Input	2.0	3.5	4.7	ns	See Figure 1
t_{PLH}, t_{PHL}	Propagation Delay, Data Inputs	3.0	6.0	9.0	ns	
t_{TLH} t_{THL}	Output Transition Time 20% to 80%, 80% to 20%	1.5	2.2	3.6	ns	
$t_s(H)$ $t_s(L)$	Set-Up Time Data Going HIGH Data Going LOW	 4.5 4.5	 2.9 3.2		ns	
$t_h(H)$ $t_h(L)$	Hold Time Data Going LOW Data Going HIGH	 −0.5 −0.5	 −2.5 −2.8		ns	

SWITCHING CIRCUIT AND WAVEFORMS



NOTE:

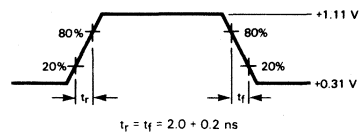
t_s is the minimum time before the positive transition of the enable pulse that information must be present at the data input (D).

t_h is the minimum time after the positive transition of the enable pulse that information must remain unchanged at the data input (D).

$L_1 = L_2$ equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF

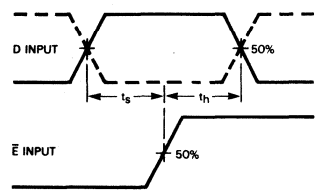
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2}$ = 2.0 V
V_{EE} = -3.2 V

INPUT PULSE

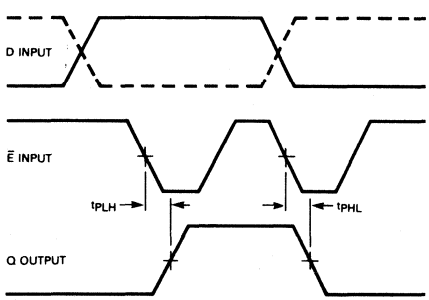


$t_r = t_f$ = 2.0 + 0.2 ns

SET-UP AND HOLD TIMES



ENABLE TO OUTPUT



DATA TO OUTPUT (ENABLE LOW)

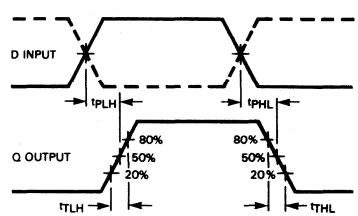


Fig. 1

F10166 • F10566

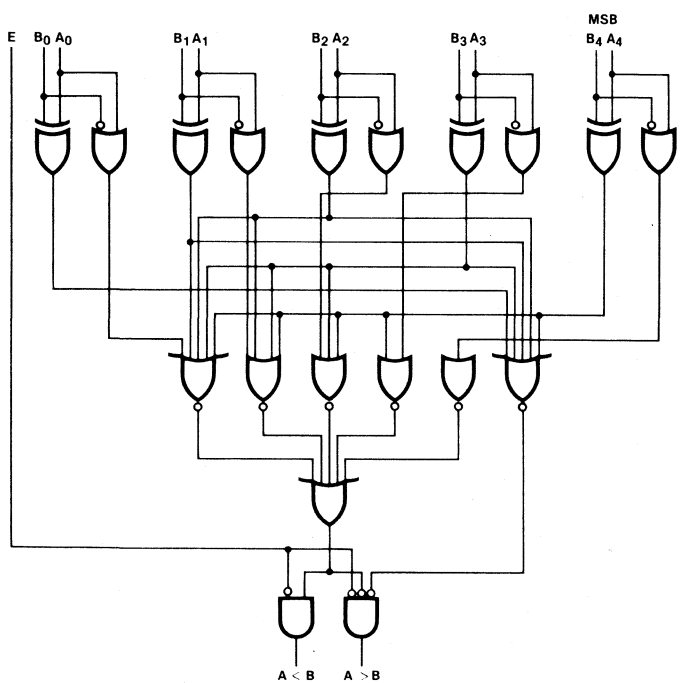
5-BIT COMPARATOR

F10K VOLTAGE COMPENSATED ECL

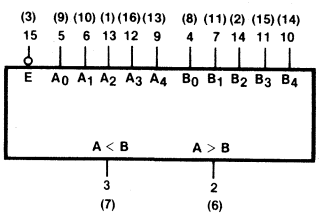
DESCRIPTION – The F10166/F10566 are high-speed expandable 5-Bit Comparators for comparing the magnitude of two binary words. Two outputs are provided: A>B and A<B. A = B can be obtained by NORing the two outputs with an additional gate. A HIGH level on the enable function forces both outputs with an additional gate. A HIGH level on the enable function forces both outputs LOW. Multiple F10166s may be used for larger word comparisons. Inputs A_4 and B_4 are the most significant bits.

- **VOLTAGE COMPENSATED . . . NOISE MARGIN INSENSITIVE TO POWER SUPPLY VARIATIONS AND TRANSIENTS, RELAXED POWER SUPPLY REQUIREMENTS**
- **INTERNAL 50 kΩ (NOMINAL) INPUT PULL-DOWN RESISTORS . . . UNUSED INPUTS MAY BE LEFT OPEN**
- **OPEN EMITTER-FOLLOWER OUTPUTS DRIVE TERMINATED LINES**
- **SINGLE V_{EE} POWER SUPPLY . . . −4.7 TO −6.2 V**
- **FULLY COMPATIBLE WITH OTHER 10,000 SERIES ECL**

LOGIC DIAGRAM

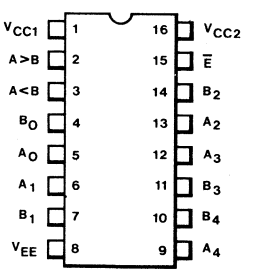


LOGIC SYMBOL



V_{CC1} = Pin 1 (5) V_{EE} = Pin 8 (12)
V_{CC2} = Pin 16 (4) ( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



TRUTH TABLE

INPUTS			OUTPUTS	
E	A_n	B_n	A < B	A > B
H	X	X	L	L
L	Word A = Word B		L	L
L	Word A > Word B		L	H
L	Word A < Word B		H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

7

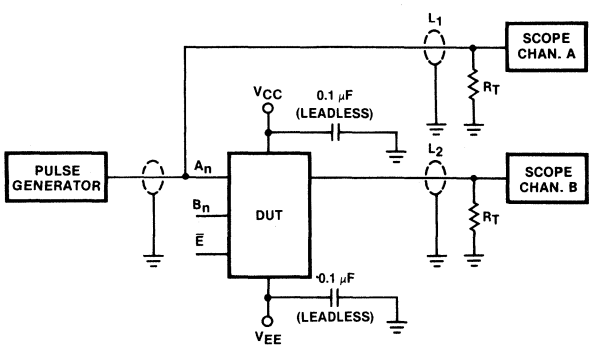
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

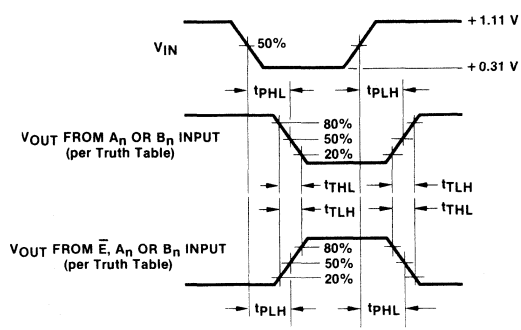
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH			220	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−75	−59		mA	25°C	Inputs and Outputs Open

AC CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, Enable to Output	1.0	2.5	3.4	ns	See Figure 1
t_{PHL}	Propagation Delay, Data to Output	1.7	4.5	6.5	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.0	3.5	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%	1.5	2.0	3.5	ns	

SWITCHING CIRCUIT AND WAVEFORMS





L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = jig and stray capacitance <5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig.1

F10168 • F10568

F10K VOLTAGE COMPENSATED ECL

QUAD LATCH/GATED OUTPUTS

DESCRIPTION – The F10168 and F10568 contains four D type latches with a Common Enable (E_C). When E_C is HIGH, outputs will follow the D inputs. Information is latched on the negative-going edge of E_C. Each latch output is combined with a separate gate control (G_n), allowing the final output (Q_n) to be forced LOW for wired-OR data bus applications.

PIN NAMES

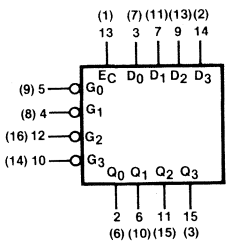
C_n	Data Inputs
$\overline{G}_n$	Output Gate Controls (Active LOW)
E_C	Common Enable (Active HIGH)
Q_n	Outputs

TRUTH TABLE

$\overline{G}$	E_C	D	Q_{t+1}
H	X	X	L
L	L	X	Q_t
L	H	L	L
L	H	H	H

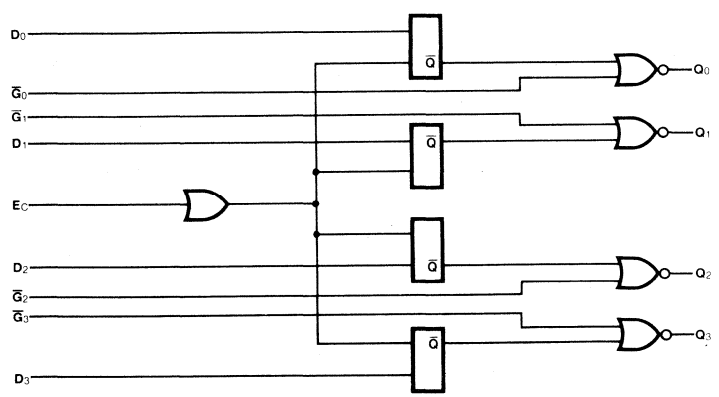
t, t + 1 = time before and after E_C negative transition.

LOGIC SYMBOL

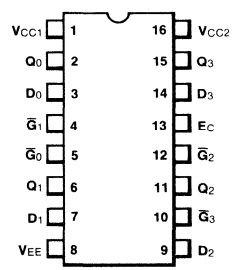


V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
( ) = Flatpak

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



7

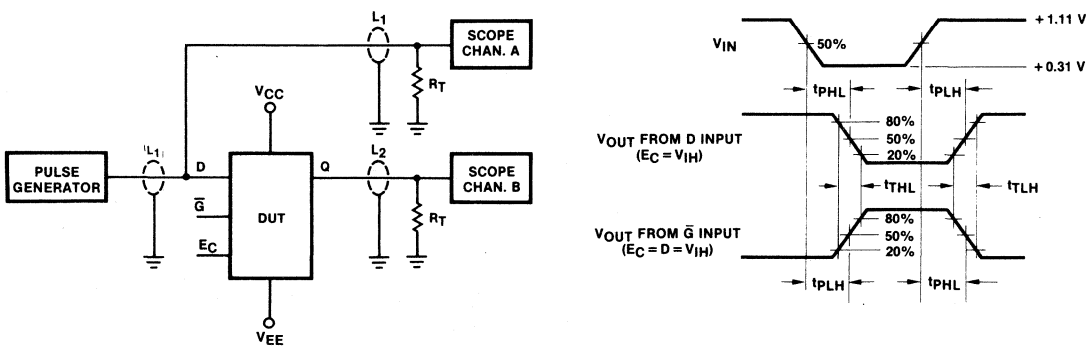
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH				μA	25°C	$V_{IN} = V_{IHA}$
	Data			245			
	Enable			290			
	Gate			265			
I_{EE}	Supply Current	−75	−60		mA	25°C	Inputs and Outputs Open

AC CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay,				ns	
	Enable and Data	1.0	4.0	5.4		
	Gate	1.0	2.0	3.5	ns	
t_{TLH}, t_{THL}	Transition Time, (20% to 80%) (80% to 20%)	1.5	2.0	3.5	ns	See Figure 1
t_s	Set-Up Time	2.5	−0.1		ns	
t_h	Hold Time	1.5	+0.1		ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_1 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 uF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Figure 1

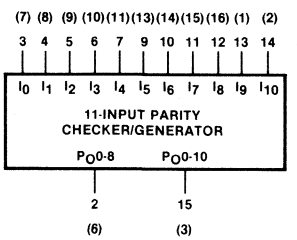
F10170 • F10570
11-INPUT PARITY CHECKER/GENERATOR

)ESCRIPTION — The F10170 and F10570 are very high-speed 11-Input Parity Check-
:r/Generators. It is useful for data processing, memory and data transmission applica-
ions. Two outputs are provided; P_O0-8 is HIGH when there is an odd number of HIGH
nputs on I_0, I_1 to I_8. The output P_O0-10 will be HIGH if there is an odd number of HIGH
nputs on I_0, I_1, to I_{10}. Unused inputs are held LOW by internal load resistors. Note from
he logic diagram that there is only a single gate delay from inputs I_9 and I_{10} to the
utput P_O0-10 making them ideal for expansion when more than 11 inputs are required.
ypical propagation delays are 4 ns from inputs I_0-I_8 to output P_O0-8, and 6 ns to output
$_O$0-10. Typical delay from I_9 and I_{10} to P_O0-10 is 2 ns.

IN NAMES

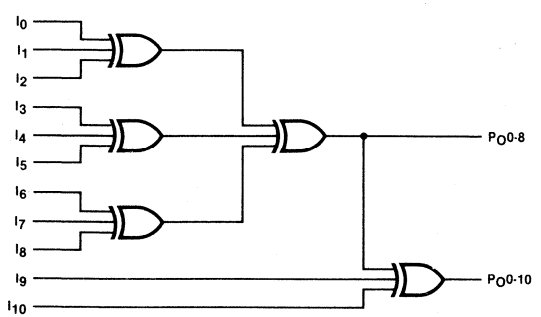
I_n	Inputs
P_O	Parity Odd

LOGIC SYMBOL

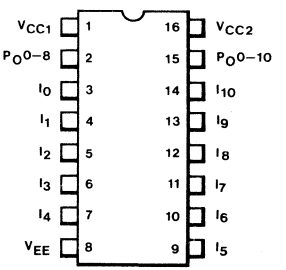


V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



7

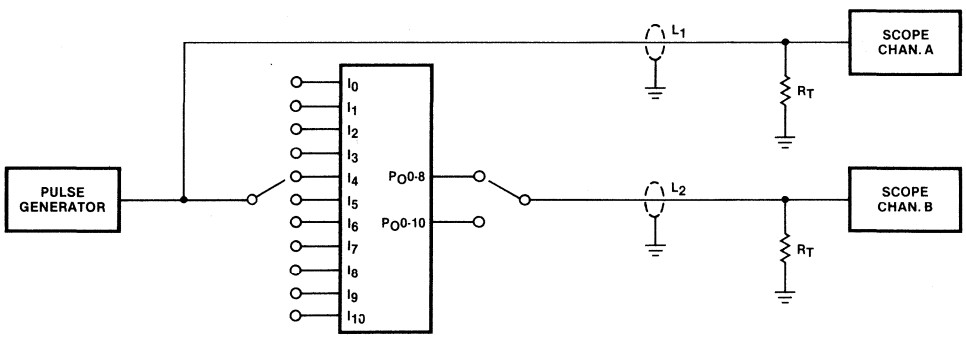
DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH (All Inputs)			220	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−68	−53		mA	25°C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS: V_{EE} = −5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay, HIGH to LOW LOW to HIGH Z (I, to P_O0-8)	2.0	4.0	7.5	ns	See Figure 1
t_{THL}, t_{TLH}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.5	2.0	3.3	ns	
t_{PLH}, t_{PHL}	Propagation Delay, HIGH to LOW LOW to HIGH (I_{10} to P_O0-10)	3.0		11.0	ns	

SWITCHING CIRCUIT AND WAVEFORM



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

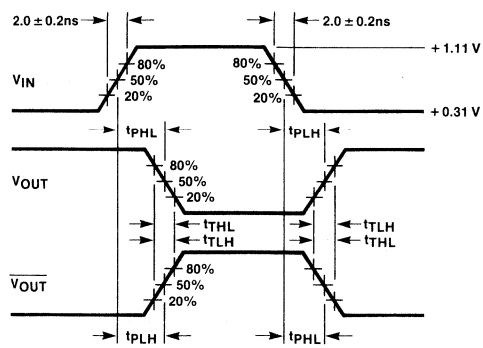


Fig. 1.

F10171 • F10571

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

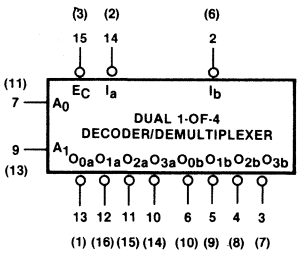
SELECTED OUTPUTS LOW

DESCRIPTION — The F10171 and F10571 contain a pair of 1-of-4 Decoder/Multiplexers with Common Enable ($\overline{E}_C$) and Address (A_0 and A_1) inputs. In each decoder the unselected (or disabled) outputs are HIGH and the selected (or enabled) output repeats the information present on its data input ($\overline{I}_a$ or $\overline{I}_b$). If the $\overline{E}_C$ input is HIGH all outputs of both decoders are HIGH, as indicated in the truth table. The F10171 can be used as a 1-of-8 decoder/demultiplexer by connecting the True and Complement of the third address bit to $\overline{I}_a$ and $\overline{I}_b$, respectively, and using $\overline{E}_C$ as either a data input or as an enable.

PIN NAMES

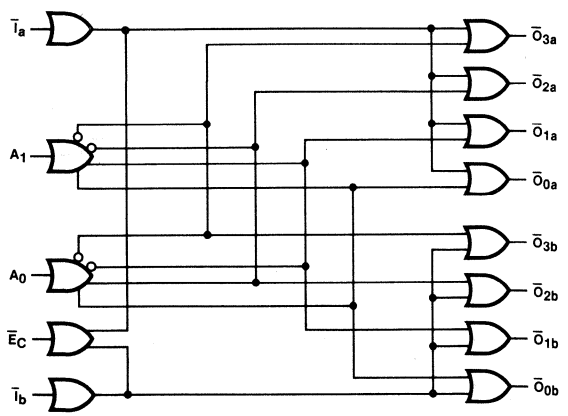
$\overline{E}_C$	Common Enable (Active LOW)
A_n	Address Inputs
$\overline{I}_n$	Data Inputs
$\overline{O}_n$	Outputs

LOGIC SYMBOL

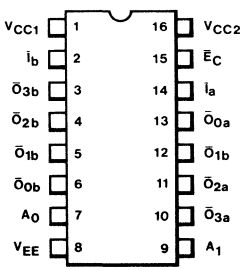


V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



7

TRUTH TABLE

$\overline{E}_C$	$\overline{I}_a$ / $\overline{I}_b$	A_1	A_0	$\overline{O}_{0a}$ / $\overline{O}_{0b}$	$\overline{O}_{1a}$ / $\overline{O}_{1b}$	$\overline{O}_{2a}$ / $\overline{O}_{2b}$	$\overline{O}_{3a}$ / $\overline{O}_{3b}$
L	L	L	L	L	H	H	H
L	H	L	L	H	H	H	H
L	L	L	H	H	L	H	H
L	H	L	H	H	H	H	H
L	L	H	L	H	H	L	H
L	H	H	L	H	H	H	H
L	L	H	H	H	H	H	L
L	H	H	H	H	H	H	H
H	X	X	X	H	H	H	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

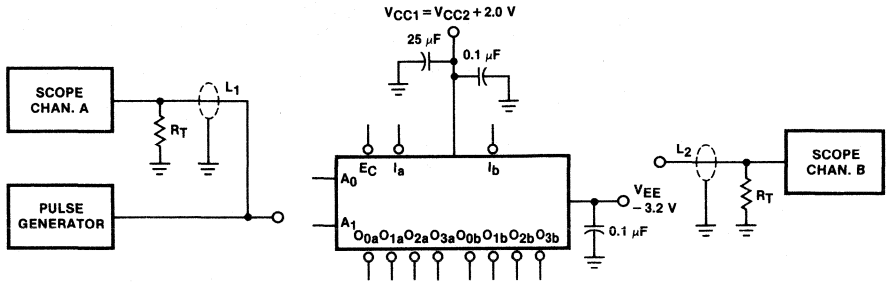
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH			220	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−77	−62		mA	25°C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay, LOW to HIGH, HIGH to LOW	1.5	4.0	6.0	ns	See Figure 1
t_{TLH} t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.1	2.0	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

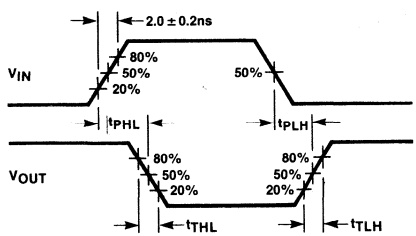


Fig. 1

F10172 • F10572

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

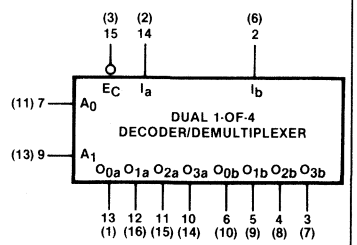
SELECTED OUTPUTS HIGH

DESCRIPTION — The F10172 and F10572 contain a pair of 1-of-4 Decoder/Multiplexers with Common Enable ($\overline{E}_C$) and Address (A_0 and A_1) inputs. In each decoder the unselected (or disabled) outputs are LOW and the selected (or enabled) output repeats the information present on its data input (I_a or I_b). If the $\overline{E}_C$ input is HIGH all outputs of both decoders are LOW, as indicated in the truth table. The F10172 can be used as a 1-of-8 decoder/demultiplexer by connecting the True and Complement of the third address bit to I_a and I_b, respectively, and using $\overline{E}_C$ as either a data input or as an enable.

PIN NAMES

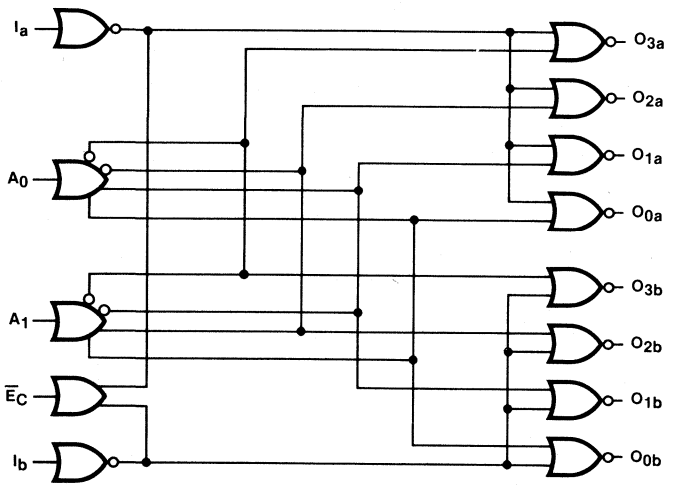
$\overline{E}_C$	Common Enable (Active LOW)
A_n	Address Inputs
I_n	Data Inputs
O_n	Outputs

LOGIC SYMBOL

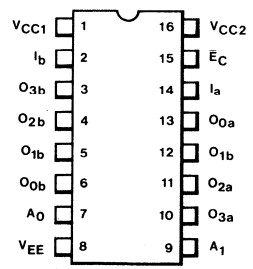


$V_{CC}1 = 1\ (5)$
$V_{CC}2 = 16\ (4)$
$V_{EE} = 8\ (12)$
( ) = Flatpak

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



TRUTH TABLE

E_C	I_a / I_b	A_1	A_0	O_{0a} / O_{0b}	O_{1a} / O_{1b}	O_{2a} / O_{2b}	O_{3a} / O_{3b}
L	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L
L	L	L	H	L	L	L	L
L	H	L	H	L	H	L	L
L	L	H	L	L	L	L	L
L	H	H	L	L	L	H	L
L	L	H	H	L	L	L	L
L	H	H	H	L	L	L	H
H	X	X	X	L	L	L	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

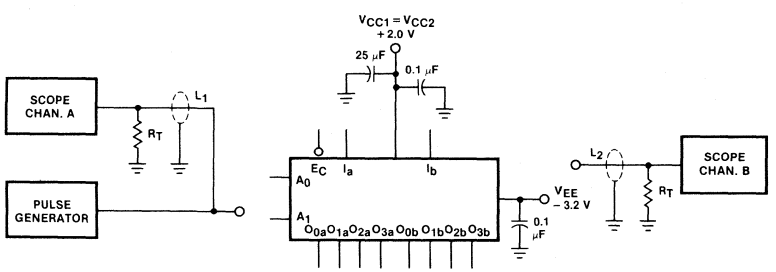
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH			220	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−77	−62		mA	25°C	Inputs and Outputs Open

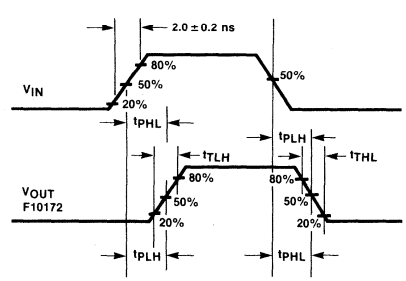
SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, LOW to HIGH, HIGH to LOW	1.5	4.0	6.0	ns	See Figure 1
t_{TLH} t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.1	2.0	3.3	ns	

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SWITCHING CIRCUIT AND WAVEFORMS





L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 1

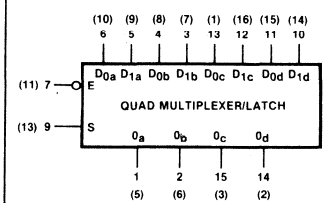
F10173 • F10573
QUAD MULTIPLEXER/LATCH

DESCRIPTION — The F10173 and F10573 are Quad 2-Channel Multiplexers with latches. They incorporate a common Enable and a common Data Select Input. The Select input determines which Data input is enabled. A HIGH input enables Data inputs D_{0a}, D_{0b}, D_{0c}, and D_{0d}, and a LOW enables Data inputs D_{1a}, D_{1b}, D_{1c}, D_{1d}. Any change on the Data input appears at the outputs while the Enable is LOW. The outputs are latched on the positive transition of the enable. While the Enable input is in the HIGH state, a change in the information present at the Data inputs does not affect the output information.

PIN NAMES

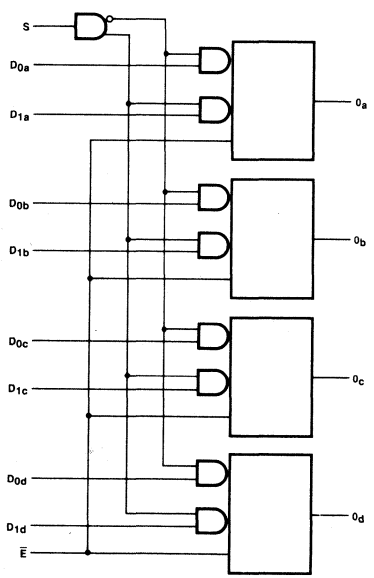
S	Data Select
D_n	Data Inputs
$\overline{E}$	Enable (Active LOW)
Q_n	Outputs

LOGIC SYMBOL



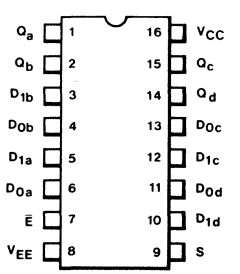
V_{CC} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



TRUTH TABLE

S	E	Q_{n+1}
H	L	D_{0a}
L	L	D_{1a}
X	H	Q_n

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

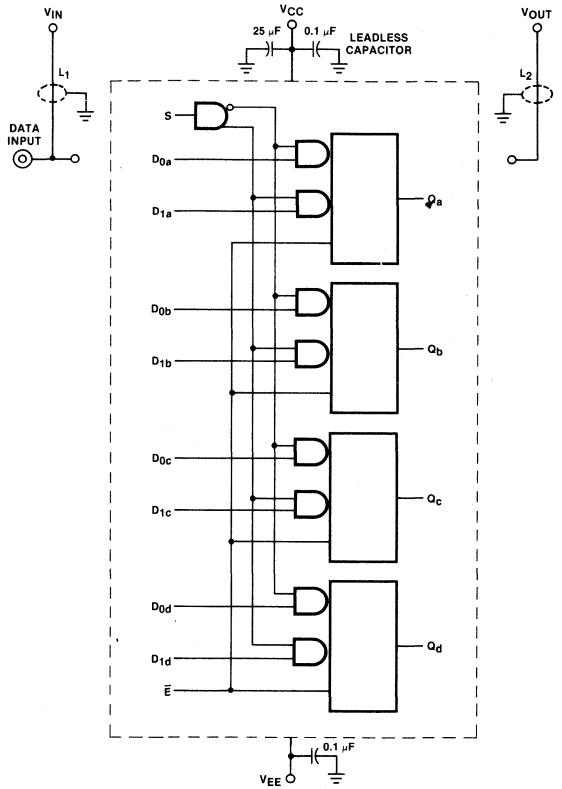
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH Enable and Select Data			 245 290	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−66			mA	25°C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

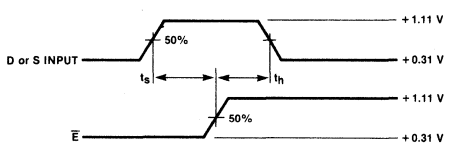
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay Enable to Output	1.0	4.5	5.2	ns	See Figure 1
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	1.0	2.5	3.8	ns	
t_{PLH}, t_{PHL}	Propagation Delay Select to Output	1.0	3.5	5.2	ns	
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.5	2.0	3.3	ns	
t_s	Set-Up Time Data Select		 1.5 2.5		ns	
t_h	Hold Time Data Select		 0.0 −0.5		ns	

7

SWITCHING TEST CIRCUIT AND WAVEFORMS



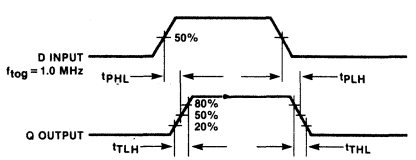
L_1 and L_2 = equal length 50 Ω impedance line
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
V_{CC} = 2.0 V
V_{EE} = −3.2 V



NOTE:

t_s is the minimum time before the positive transition of the enable pulse (E) that information must be present at the input (D) or (S).

t_h is the minimum time after the positive transition of the enable pulse (E) that information must remain unchanged at the data input (D) or (S).



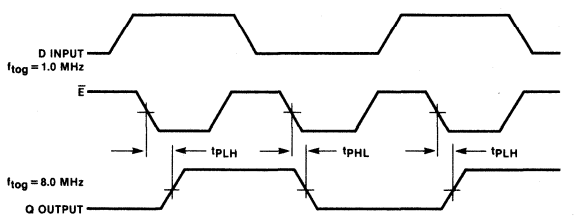


Fig.1

F10174 • F10574

DUAL MULTIPLEXER

F10K-VOLTAGE COMPENSATED ECL

DESCRIPTION — The F10174 and F10574 are high-speed Dual Channel Multiplexers with output enable capability. The Select inputs determine one of four active Data inputs for each multiplexer. When the Enable input is HIGH, both outputs are forced LOW. The Enable is also useful when OR-wiring several multiplexers to achieve additional channel capability.

PIN NAMES

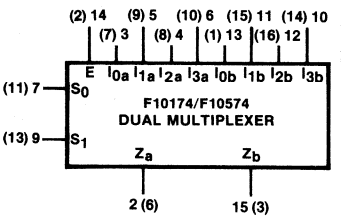
I_n	Address Inputs
$\overline{E}$	Enable (Active LOW)
Z_a	Outputs
S_n	Select Inputs

TRUTH TABLE

$\overline{E}$	S_1	S_0	Z_a	Z_b
H	X	X	L	L
L	L	L	I_{0a}	I_{0b}
L	L	H	I_{1a}	I_{1b}
L	H	L	I_{2a}	I_{2b}
L	H	H	I_{3a}	I_{3b}

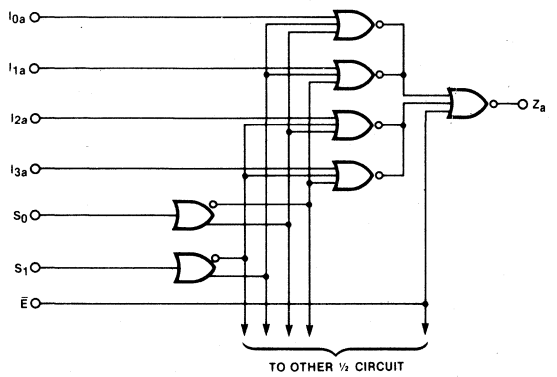
L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

LOGIC SYMBOL



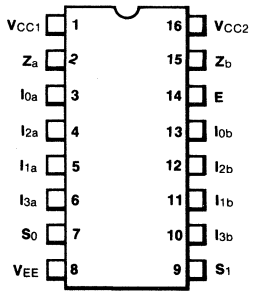
V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



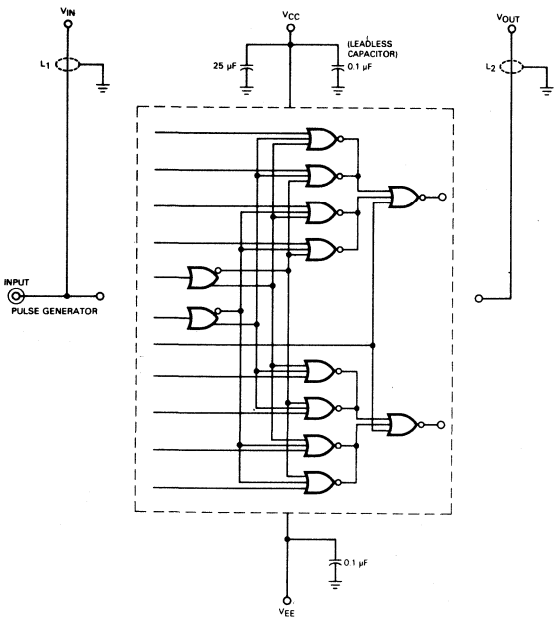
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH Data Enable			 220 330	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−50	−40		mA	25°C	Inputs and Outputs Open

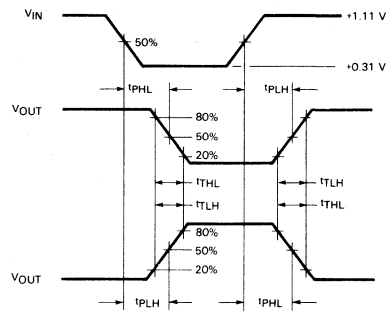
SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay Data to Output	1.5	3.0	4.5	ns	See Figure 1
t_{PLH}, t_{PHL}	Propagation Delay, Select to Output	2.0	4.0	6.0	ns	
t_{PHL}	Propagation Delay Enable to Output	1.0	2.0	2.9	ns	
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.5	2.0	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 uF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V



1) Data to Output Delay
Pulse (V_{IN}) applied to selected data input per truth table.
2) Select to Output Delay
Pulse (V_{IN}) applied to select input with one selected data input HIGH and the other selected data input LOW per address truth table.
3) Enable to Output Delay
Selected data input at V_{IH} while the input pulse (V_{IN}) is applied to the enable input.

Fig. 1

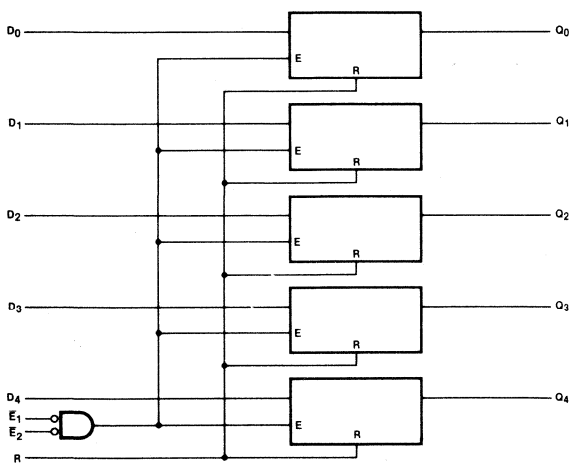
F10175 • F10575
QUINT LATCH

DESCRIPTION — The F10175 and F10575 are high-speed low-power Quint Latches. They feature five D type latches with common Reset and a common 2-input Enable. Data is transferred on the negative edge of the enable and latched on the positive edge. The two Enable inputs are OR-ed together. Propagation delays are typically 2.5 ns from each Data input to the output.

Any change on the Data input appears at the outputs while the Enable inputs are LOW. The outputs are latched on the positive transition of the Enable. While the Enable is in the HIGH state, a change in the information present at the Data inputs does not affect the output information. The Reset input is enabled only when the Enable is in the HIGH state.

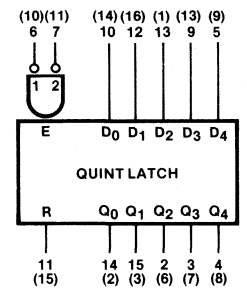
PIN NAMES

D_n	Data Inputs
$\overline{E}_n$	Enable Inputs (Active LOW)
R	Reset
Q_n	Outputs



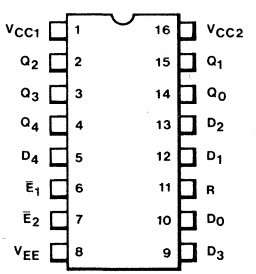
Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

LOGIC SYMBOL



V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



TRUTH TABLE

D	$\bar{E}_0$	$\bar{E}_1$	R	Q_{n+1}
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Q_n
X	X	H	L	Q_n
X	H	X	H	L
X	X	H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

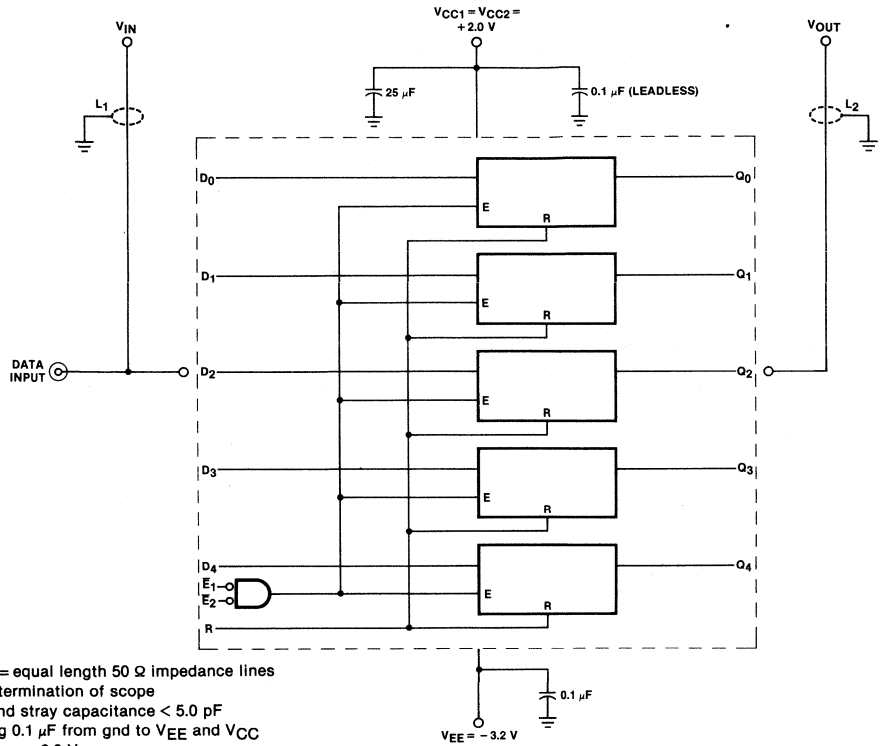
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH Data Enable Reset			 290 645	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−97			mA	25°C	Inputs and Outputs Open

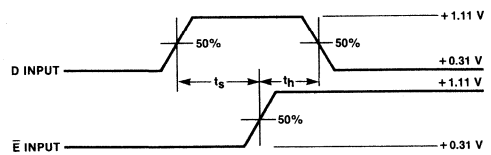
SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay Enable to Output	1.0	3.3	4.3	ns	See Figure 1
t_{PLH}, t_{PHL}	Propagation Delay Data to Output	1.0	2.5	3.5	ns	
t_{PHL}, t_{PLH}	Propagation Delay Reset to Output	1.0	2.5	3.9	ns	
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.5	2.0	3.3	ns	
t_s	Set-Up Time Data	2.5	1.5		ns	
t_h	Hold Time Data	1.5	0.5		ns	

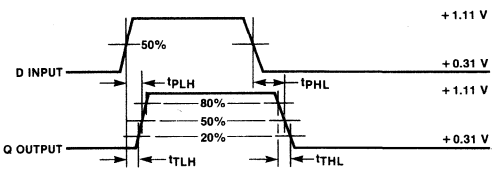
SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V



DATA TO OUTPUT (ENABLE LOW)

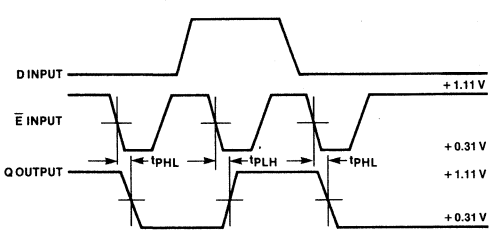


NOTE:

t_S is the minimum time before the positive transition of the enable that information must be present at the data input (D).

t_h is the minimum time after the positive transition of the enable pulse that information must remain unchanged at the data input (D).

ENABLE TO OUTPUT



RESET TO OUTPUT (DATA HIGH)

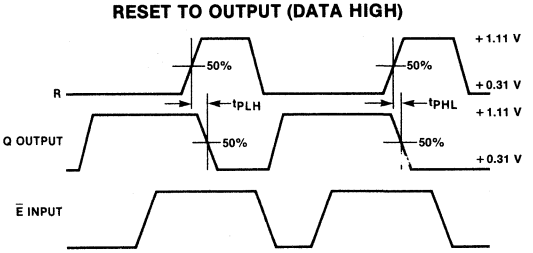


Fig. 1

F10176 • F10576

HIGH SPEED HEX D FLIP-FLOP

F10K VOLTAGE COMPENSATED ECL

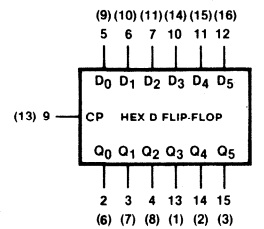
DESCRIPTION — The F10176 and F10576 contain six high-speed master/slave D type flip-flops which have a common Clock. Data is entered into the master when the Clock is LOW. Data transfer takes place on the positive-going clock transition. A change in the information present at the Data input will not affect the output information.

- **VOLTAGE COMPENSATED—NOISE MARGIN INSENSITIVE TO POWER SUPPLY VARIATIONS AND TRANSIENTS**
- **50 Ω DRIVE AND WIRED-OR CAPABILITY**
- **SEPARATE V_{CC} PINS—ELIMINATE NOISE COUPLING**
- **INTERNAL 50 kΩ INPUT PULL-DOWN RESISTORS**

PIN NAMES

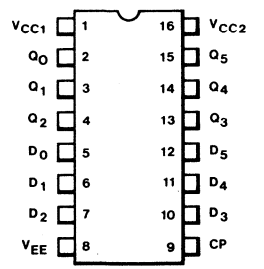
D_n	Data Inputs
CP	Clock
Q_n	Outputs

LOGIC SYMBOL

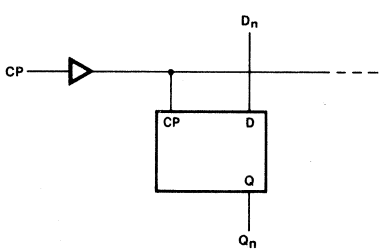


V_{CC1} = Pin 1 (5) V_{EE} = Pin 8 (12)
V_{CC2} = Pin 16 (4) ( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



LOGIC DIAGRAM (One Flip-flop shown)



CLOCKED TRUTH TABLE

CP	D	Q_{t+1}
L	X	Q_t
↓	L	L
↓	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
t, t + 1 = Time before and after CP positive transition

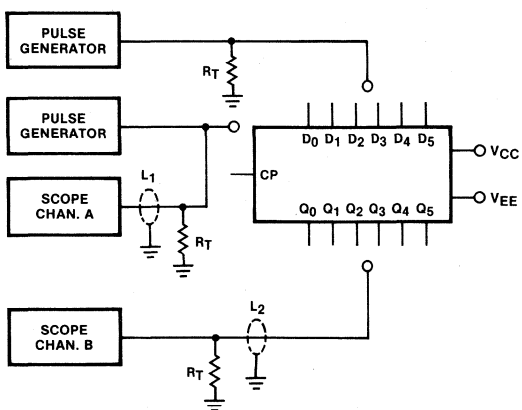
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH Data Clock			 220 310	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	−80	−88		mA	25°C	Inputs and Outputs Open

AC CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay LOW to HIGH, HIGH to LOW	1.5	3.0	4.5	ns	See Figure 1
t_{TLH}, t_{THL}	Transition Time, LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.5	2.0	3.3	ns	
t_s	Set-Up Time	2.5			ns	
t_h	Hold Time	1.5			ns	

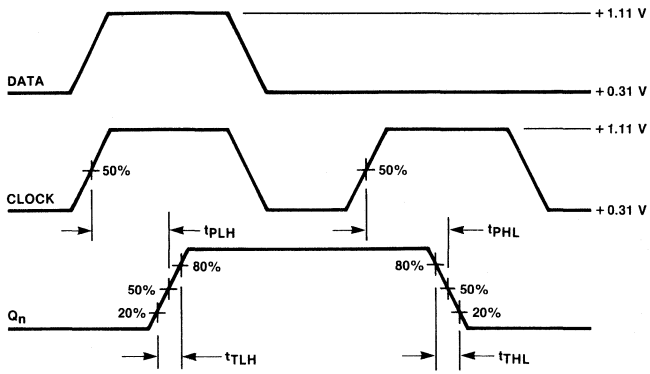
AC TEST CIRCUIT

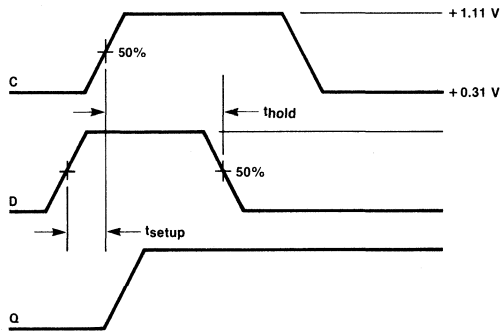


L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF

Decoupling 0.1 μF from Gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

WAVEFORMS





$t_{set\text{-}up}$ is the minimum time before the transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D). Note that t_{hold} may be a negative number.

Figure 1

F10179 • F10579

CARRY LOOKAHEAD GENERATOR

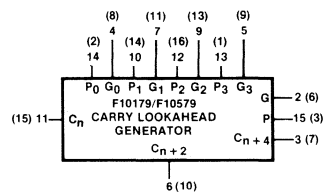
F10K VOLTAGE COMPENSATED ECL

DESCRIPTION — The F10179 and F10579 are high-speed carry generators intended for use with the F10181 4-bit ALU. Typical addition times for two 32-bit words is 30 ns when using F10181 in the ripple carry mode. When the F10179 carry lookahead generator is used, the typical add time drops to 18 ns.

PIN NAMES

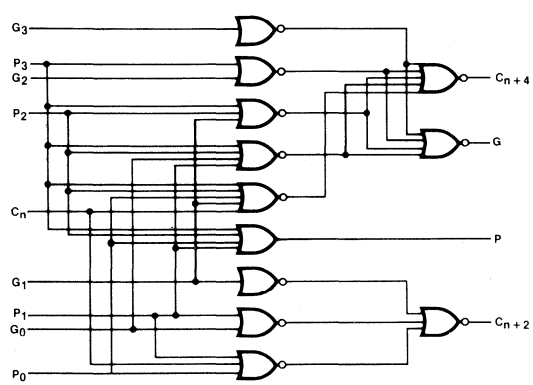
C_n	Carry In
$C_{n+2,\ +4}$	Carry Out
P	Propagate
G	Generate

LOGIC SYMBOL



V_{CC1} = 1(5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) Flatpak

LOGIC DIAGRAM



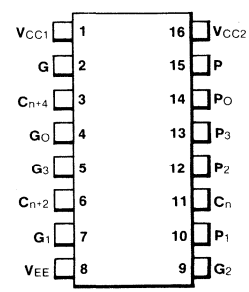
$P = P_0 + P_1 + P_2 + P_3$

$G = (G_0 + P_1 + P_2 + P_3)(G_1 + P_2 + P_3)(G_2 + P_3)G_3$

$C_{n+2} = (C_n + P_0 + P_1)(G_0 + P_1)G_1$

$C_{n+4} = (C_n + P_0 + P_1 + P_2 + P_3)(G_0 + P_1 + P_2 + P_3)(G_1 + P_2 + P_3)(G_2 + P_3)G_3$

CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



$C_{n+2} = G_1(G_0 + P_1)C_n + P_1 + P_0)$ (Product of Max terms)
or
$\overline{C}_{n+2} = \overline{G}_1 + \overline{G}_0\overline{P}_1 + \overline{C}_n\overline{P}_1\overline{P}_0$ (Complement of the sum of Min terms)

$C_{n+4} = G_3(G_2 + P_3)(G_1 + P_2 + P_3)(G_0 + P_1 + P_2 + P_3)(C_n + P_0 + P_1 + P_2 + P_3)$
or
$\overline{C}_{n+4} = \overline{G}_3 + \overline{G}_2\overline{P}_3 + \overline{G}_1\overline{P}_2\overline{P}_3 + \overline{G}_0\overline{P}_1\overline{P}_2\overline{P}_3 + \overline{C}_n\overline{P}_0\overline{P}_1\overline{P}_2\overline{P}_3$

$G_G = G_3(G_2 + P_3)(G_1 + P_2 + P_3)(G_0 + P_1 + P_2 + P_3)$
or
$\overline{G}_G = \overline{G}_3 + \overline{G}_2\overline{P}_3 + \overline{G}_1\overline{P}_2\overline{P}_3 + \overline{G}_0\overline{P}_1\overline{P}_2\overline{P}_3$

$P_G = \overline{P}_0 + \overline{P}_1 + \overline{P}_2 + \overline{P}_3$
or
$\overline{P}_G = \overline{P}_0\overline{P}_1\overline{P}_2\overline{P}_3$

TRUTH TABLE

INPUTS										OUTPUTS		
C_n	G_0	P_0	G_1	P_1	G_2	P_2	G_3	P_3	C_{n+2}	C_{n+4}	G_G	P_G
X	X	X	H	H					H			
H	H	X	H	X					H			
X	H	H	H	X					H			
X	X	X	L	X					L			
X	L	X	X	L					L			
L	X	L	X	L					L			
X	X	X	X	X	X	X	H	H		H		
X	X	X	X	X	H	H	H	X		H		
X	X	X	H	H	H	X	H	X		H		
X	H	H	H	X	H	X	H	X		H		
H	H	X	H	X	H	X	H	X		H		
X	X	X	X	X	X	X	L	X		L		
X	X	X	X	X	L	X	X	L		L		
X	X	X	L	X	X	L	X	L		L		
X	L	X	X	L	X	L	X	L		L		
L	X	L	X	L	X	L	X	L		L		
	X		X	X	X	X	H	H			H	
	X		X	X	H	H	H	X			H	
	X		H	H	H	X	H	X			H	
	H		H	X	H	X	H	X			H	
	X		X	X	X	X	L				L	
	X		X	X	L	X	X	L			L	
	X		L	X	X	L	X	L			L	
	L		X	L	X	L	X	L			L	
		H		X		X		X				H
		X		H		X		X				H
		X		X		H		X				H
		X		X		X		H				H
		L		L		L		L				L

L = LOW Voltage Level H = HIGH Voltage Level X = Don't Care

DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH G_0, G_1, C_n G_2, G_3 P_0 P_1, P_3 P_2			 270 225 355 440 395	 µA	 25 °C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−72	−59		mA	25 °C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25$ °C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay LOW to HIGH, HIGH to LOW C_n to C_{n+2}	1.0	3.0	4.5	ns	See Figure 1, 3
t_{PLH}, t_{PHL}	Propagation Delay LOW to HIGH, HIGH to LOW G_3 to G	1.0	4.0	5.5	ns	See Figure 2, 3
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	0.8	3.5	5.5	ns	See Figure 1, 3

SWITCHING CIRCUIT AND WAVEFORMS

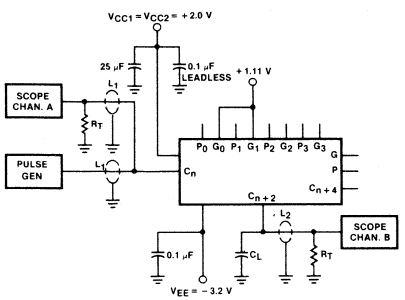


Fig. 1 For Output $C_n + 2$

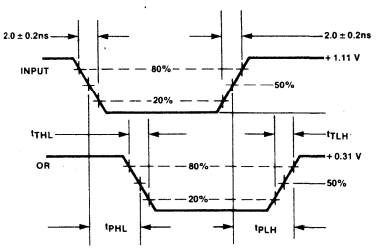


Fig. 3 For Both Outputs

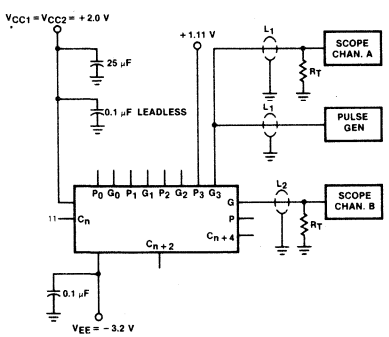


Fig. 2 For Output G

L_1 and L_2 = equal length 50 Ω impedance lines
$R_T = 50$ Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

F10180 • F10580

F10K VOLTAGE COMPENSATED ECL

DUAL 2-BIT ADDER/SUBTRACTOR

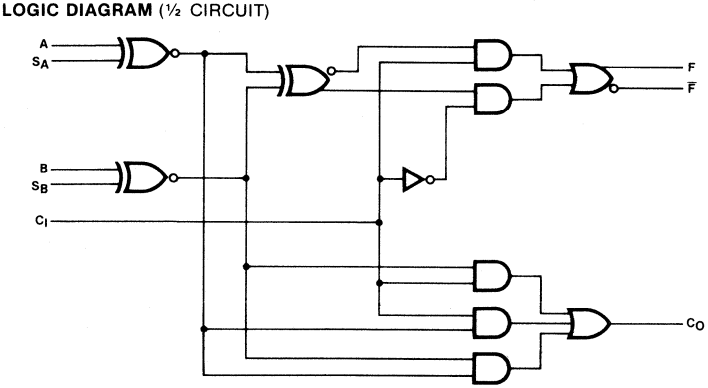
DESCRIPTION – The F10180/F10580 are high-speed, low-power Dual 2-Bit Adder/Subtractors. It is designed to be used in special purpose adder/subtractors or in high speed multiplier arrays. Inputs for each adder are Carry-in, Operand A, and Operand B; outputs are Function, Active LOW Function, and Carry-out. The common Select inputs serve as a control line to invert A and B for subtract.

- **VOLTAGE COMPENSATED . . . NOISE MARGIN INSENSITIVE TO POWER SUPPLY VARIATIONS AND TRANSIENTS, RELAXED POWER SUPPLY REQUIREMENTS**
- **INTERNAL 50 kΩ (NOMINAL) INPUT PULL DOWN RESISTORS . . . UNUSED INPUTS MAY BE LEFT OPEN**
- **OPEN EMITTER-FOLLOWER OUTPUTS DRIVE TERMINATED LINES**
- **SINGLE V_{EE} POWER SUPPLY . . . −4.7 TO 16.2 V**
- **COMPLEMENTARY, SIMULTANEOUS OUTPUTS (ON FUNCTION OUTPUTS)**
- **FULLY COMPATIBLE WITH OTHER 10,000 SERIES ECL**

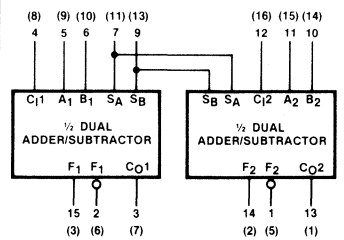
PIN NAMES

F	Function Output
$\overline{F}$	Function Output (Active LOW)
C_O	Carry-Out
C_I	Carry-In
A, B	Operands
S_A, S_B	Operand Selects

LOGIC DIAGRAM (½ CIRCUIT)

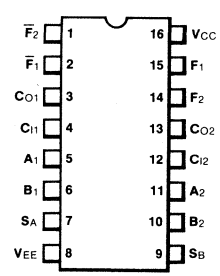


LOGIC SYMBOL



V_{EE} = Pin 8 (12)
V_{CC} = Pin 16 (1)
( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

FUNCTION	INPUTS					OUTPUTS		
	S_A	S_B	A	B	C_I	F	$\overline{F}$	C_O
A plus B plus C_I	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	L
	H	H	L	H	L	H	L	L
	H	H	L	H	H	L	H	H
	H	H	H	L	L	H	L	L
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	H
	H	H	H	H	H	H	L	H
C_I plus A minus B	H	L	L	L	L	H	L	L
	H	L	L	L	H	L	H	H
	H	L	L	H	L	L	H	L
	H	L	L	H	H	H	L	L
	H	L	H	L	L	L	H	H
	H	L	H	L	H	H	L	H
	H	L	H	H	L	H	L	L
	H	L	H	H	H	L	H	H
C_I plus B minus A	L	H	L	L	L	H	L	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	L	H	H
	L	H	L	H	H	H	L	H
	L	H	H	L	L	L	H	L
	L	H	H	L	H	H	L	L
	L	H	H	H	L	H	L	L
	L	H	H	H	H	L	H	H
C_I minus A minus B	L	L	L	L	L	L	H	H
	L	L	L	L	H	H	L	H
	L	L	L	H	L	H	L	L
	L	L	L	H	H	L	H	H
	L	L	H	L	L	H	L	L
	L	L	H	L	H	L	H	H
	L	L	H	H	L	L	H	L
	L	L	H	H	H	H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level

FUNCTION SELECT TABLE

S_A	S_B	FUNCTION
H	H	F = A plus B plus C_I
H	L	F = C_I plus A minus B
L	H	F = C_I plus B minus A
L	L	F = C_I minus A minus B

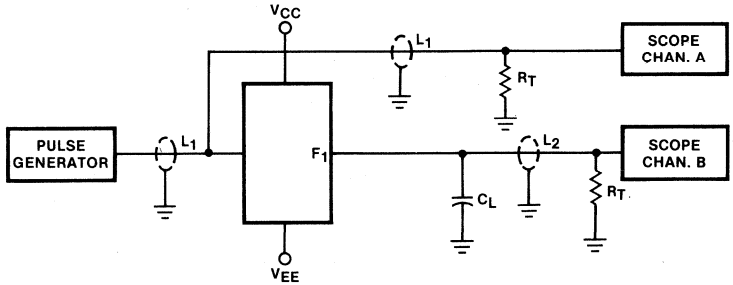
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH				μA	25°C	$V_{IN} = V_{IHA}$
	A_n, B_n			220			
	S_n			290			
	CI_1, CI_2			370			
I_{EE}	Power Supply Current	−86	−65		mA	25°C	Inputs Open

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PHL}, t_{PLH}	Propagation Delay Operands to Output Selects to Output	1.5	4.5	6.5	ns	See Figure 1
t_{PHL}, t_{PLH}	Propagation Delay, Carry-In to Output	1.5	2.2	3.7	ns	
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.5	2.0	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF (leadless) from gnd to V_{EE} and V_{CC}
V_{CC} = 2.0 V
V_{EE} = −3.2 V

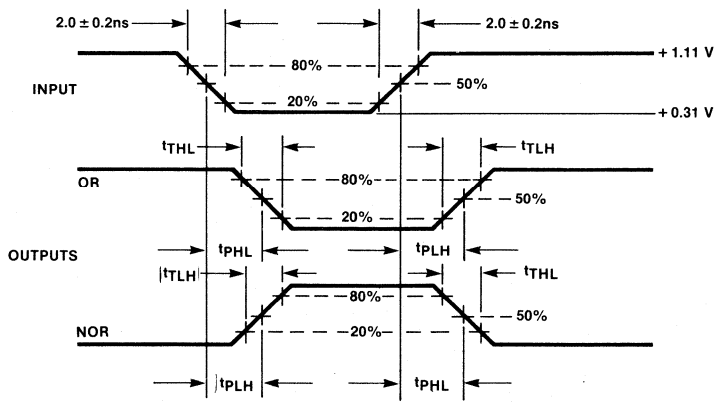


Fig. 1

F10181 • F10581

4-BIT ALU/FUNCTION GENERATOR

F10K VOLTAGE COMPENSATED ECL

DESCRIPTION — The F10181 and F10581 are high-speed arithmetic logic units capable of performing 16 logic operations and 16 arithmetic operations on two 4-bit words. Full internal carry is incorporated for ripple through operation.

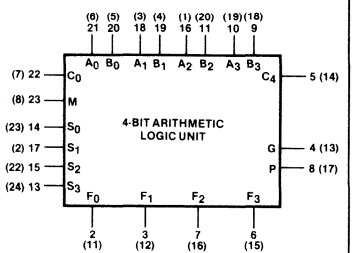
Arithmetic/logic operations are selected by applying the appropriate binary word to the select inputs (S_0 through S_3) as indicated in the tables of arithmetic/logic functions.

Group carry propagate (P) and carry generate (G) are provided to allow fast operations on very long words using a second order lookahead. The internal carry is enabled by applying a LOW level voltage to the Mode Control input (M).

When used with the F10179, full carry lookahead, as a second order lookahead block, the F10181 provides high speed arithmetic operations on very long words.

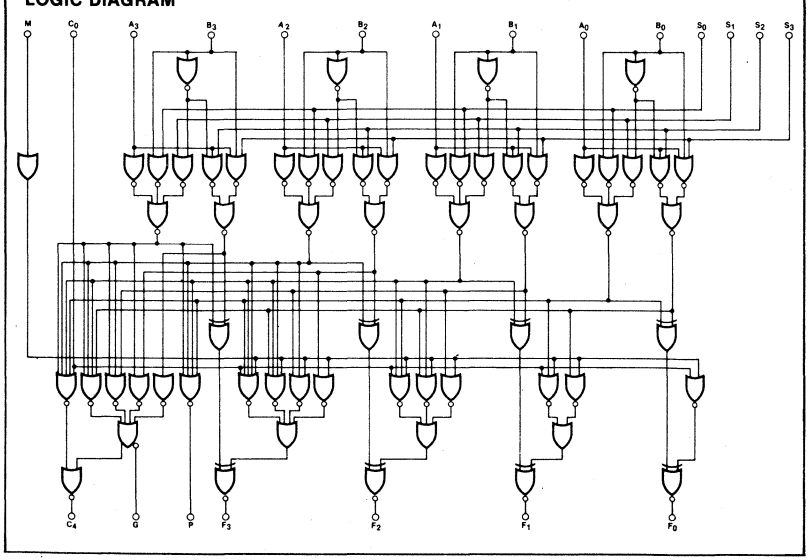
- VOLTAGE COMPENSATED—INSENSITIVE TO POWER SUPPLY VARIATIONS AND GRADIENTS
- OPEN EMITTER-FOLLOWER OUTPUTS
- SEPARATE V_{CC} PINS TO ELIMINATE NOISE COUPLING
- INTERNAL 50 kΩ (NOMINAL) INPUT PULL-DOWN RESISTORS—UNUSED INPUTS MAY BE LEFT OPEN

LOGIC SYMBOL

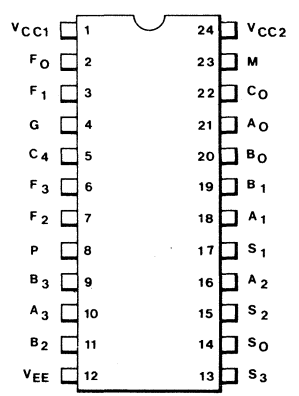


V_{CC1} = Pin 1 (10)
V_{CC2} = Pin 24 (9)
V_{EE} = Pin 12 (21)
( ) = Flatpak

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



PIN NAMES

A_n, B_n	Operand Inputs	M	Mode Control
F_n	Function Outputs	C_4	Carry Out
S_n	Select Inputs	G	Carry Generate
C_0	Carry In	P	Carry Propagate

LOGIC FUNCTIONS

				OUTPUT FUNCTION F		
FUNCTION SELECT				M = HIGH (Logic Mode)	M = LOW (Arithmetic Mode)	
S_3	S_2	S_1	S_0	C_0 = H or L	C_0 = LOW	C_0 = HIGH
L	L	L	L	$\overline{A}$	A	A plus 1
L	L	L	H	$\overline{A}+\overline{B}$	A plus $A\overline{B}$	A plus $A\overline{B}$ plus 1
L	L	H	L	$\overline{A}+B$	A plus AB	A plus AB plus 1
L	L	H	H	HIGH	A plus A (2 times A)	A plus A plus 1
L	H	L	L	$\overline{A}\overline{B}$	A + B	(A + B) plus 1
L	H	L	H	$\overline{B}$	(A + B) plus $A\overline{B}$	(A + B) plus $A\overline{B}$ plus 1
L	H	H	L	$\overline{A \oplus B}$	A plus B	A plus B plus 1
L	H	H	H	$A+\overline{B}$	(A + B) plus A	(A + B) plus A plus 1
H	L	L	L	$\overline{A}B$	$A+\overline{B}$	$(A+\overline{B})$ plus 1
H	L	L	H	$A \oplus B$	A minus B minus 1	A minus B
H	L	H	L	B	$(A+\overline{B})$ plus AB	$(A+\overline{B})$ plus AB plus 1
H	L	H	H	A + B	$(A+\overline{B})$ plus A	$(A+\overline{B})$ plus A plus 1
H	H	L	L	LOW	minus 1 (2's complement)	Zero
H	H	L	H	$A\overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
H	H	H	L	AB	AB minus 1	AB
H	H	H	H	A	A minus 1	A

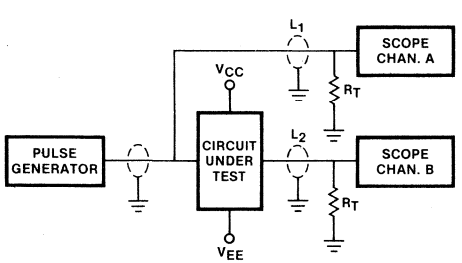
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH				μA	25°C	$V_{IN} = V_{IHA}$
	Pin M			200			
	Pins A3, A2, A1, A0			220			
	Pins B3, B2, B1, B0			245			
	Pins S3, S2, S1, S0			265			
	Pin C0			290			
I_{EE}	Power Supply Current	−145	−110		mA	25°C	Inputs Open

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	CHARACTERISTIC	OUTPUT	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS See Figure 1
t_{PHL},t_{PLH}	Propagation Delay, C – C_4	1	1.1	3.1	5.0	ns	A_0, A_1, A_2, A_3 = +1.11 V
t_{THL},t_{TLH}	Transition Time, C_4	1	1.0	2.0	3.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, C – F_1	1	2.0	4.5	7.0	ns	A_0, = +1.11 V
t_{THL},t_{TLH}	Transition Time, F_1	1	1.5	3.0	5.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, A_1 – F_1	1	3.0	6.5	10.0	ns	All Inputs = +0.31 V
t_{THL},t_{TLH}	Transition Time, F_1	1	1.5	3.0	5.0	ns	
t_{PHL},t_{PLH}	Propagation Delay, A_1 – P	1	2.0	5.0	6.5	ns	S_0, S_3, = +1.11 V
t_{THL},t_{TLH}	Transition Time, P	1	1.1	2.0	3.5	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, A_1 – G	1	2.0	4.5	7.0	ns	A_0, A_2, A_3, C = +1.11 V
t_{THL},t_{TLH}	Transition Time, G	1	1.5	4.0	5.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, A_1 – C_4	1	2.0	5.0	7.0	ns	A_0, A_2, A_3, C +1.11 V
t_{THL},t_{TLH}	Transition Time, C_4	1	1.0	2.0	3.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, B_1 – F_1	1	3.0	8.0	11.0	ns	S_3, C = +1.11 V
t_{THL},t_{TLH}	Transition Time, F_1	1	1.5	3.5	5.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, B_1 – P	1	2.0	6.0	7.5	ns	S_1, A_1, = +1.11 V
t_{THL},t_{TLH}	Transition Time, P	1	1.1	2.0	3.5	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, B_1 – G	2	2.0	6.0	8.0	ns	S_3, C = +1.11 V
t_{THL},t_{TLH}	Transition Time, G	2	1.5	3.0	5.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, B_1 – C_4	2	2.0	6.0	8.0	ns	S_3, C = +1.11 V
t_{THL},t_{TLH}	Transition Time, C_4	2	1.0	2.0	3.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, M – F_1	1	3.0	6.5	10.0	ns	All Inputs = +0.31 V
t_{THL},t_{TLH}	Transition Time, F_1	1	1.5	4.0	5.0	ns	
t_{PHL},t_{PLH}	Propagation Delay, S_1 – F_1	2	3.0	6.5	10.0	ns	A_1, B_1, = +1.11 V
t_{THL},t_{TLH}	Transition Time, F_1	2	1.5	3.0	5.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, S_1 – P	1	2.0	6.0	8.0	ns	A_3, B_3, = +1.11 V
t_{THL},t_{TLH}	Transition Time, P	1	1.1	3.0	5.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, S_1 – C_4	1	2.0	6.0	9.0	ns	A_3, B_3, = +1.11 V
t_{THL},t_{TLH}	Transition Time, C_4	1	1.1	3.0	5.0	ns	Other Inputs = +0.31 V
t_{PHL},t_{PLH}	Propagation Delay, S_1 – G	1	2.0	6.0	9.0	ns	A_3, B_3, = +1.11 V
t_{THL},t_{TLH}	Transition Time, G	1	0.8	3.0	6.0	ns	Other Inputs = +0.31 V

AC TEST CIRCUIT AND WAVEFORMS



V_{CC} = +2 V, V_{EE} – 3.2 V
R_T = 50 Ω termination of scope
L_1 = L_2 = 50 Ω transmission lines
Decoupling 0.1 μF from V_{CC} and V_{EE} to gnd

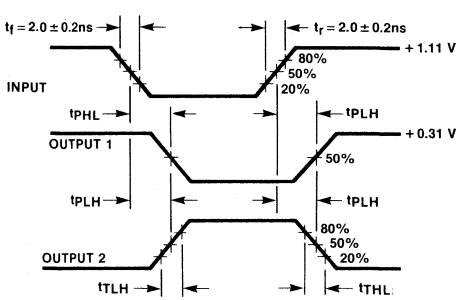


Fig. 1

F10186 • F10586

HEX D FLIP-FLOP WITH RESET

F10K VOLTAGE COMPENSATED ECL

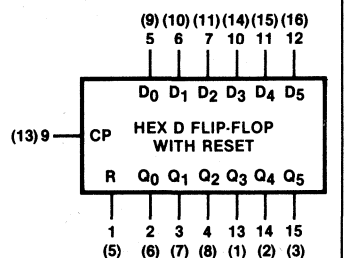
DESCRIPTION — The F10186 and F10586 contain six high-speed master/slave D-type flip-flops which have a common clock. Data is entered into the master when the Clock is LOW. Data transfer takes place on the positive-going clock transition. A change in the information present at the Data input will not affect the output information. The common reset functions only when the Clock is LOW.

- **VOLTAGE COMPENSATED—NOISE MARGIN INSENSITIVE TO POWER SUPPLY VARIATIONS AND TRANSIENTS.**
- **OPEN EMITTER-FOLLOWER OUTPUTS.**
- **50 Ω DRIVE AND WIRED-OR CAPABILITY.**
- **INTERNAL 50 kΩ INPUT PULL-DOWN RESISTORS.**

PIN NAMES

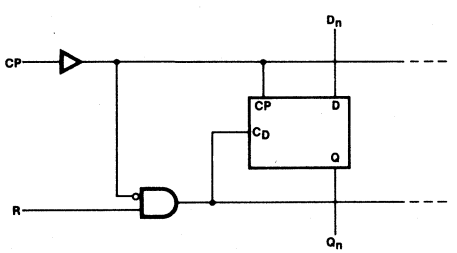
D_n	Data Inputs
CP	Clock
R	Common Reset
Q_n	Outputs

LOGIC SYMBOL



( ) = Flatpak
V_{CC} = Pin 16 (4)
V_{EE} = Pin 8 (12)

LOGIC DIAGRAM (One Flip-flop)

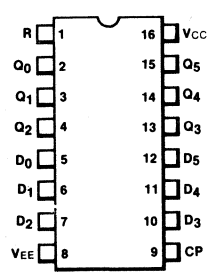


CLOCKED TRUTH TABLE

R	CP	D	Q_{t+1}
L	L	X	Q_t
L	⊓	L	L
L	⊓	H	H
H	L	X	L

X = Don't Care
H = HIGH Voltage Level
L = LOW Voltage Level
t, t + 1 = Time before and after CP positive transition

CONNECTION DIAGRAM
DIP (TOP VIEW)



DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

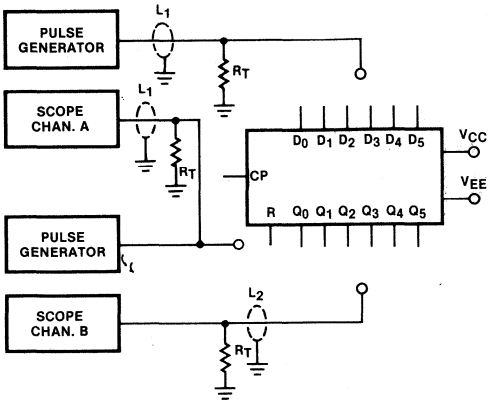
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH Data Clock Reset			 220 310 575	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	−110	−88		mA	25°C	Inputs and Outputs Open

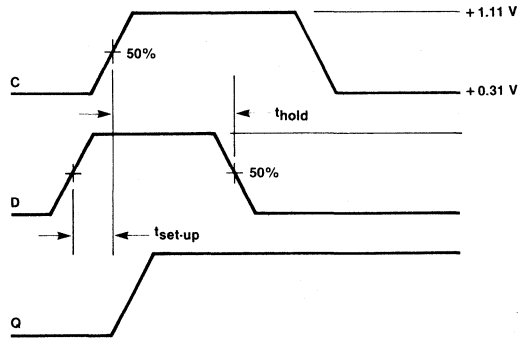
AC CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay, Reset to Q Clock to Q	 1.5 1.5	 2.5 3.5	 4.0 4.5	ns	See Figure 1
t_{TLH}, t_{THL}	Transition Time 20% to 80%, 80% to 20%	1.5	1.8	3.5	ns	
t_s	Set-Up Time	2.5			ns	
t_h	Hold Time	1.5			ns	

7

AC TEST CIRCUIT AND WAVEFORMS





L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
V_{CC} = 2.0 V
V_{EE} = −3.2 V

$t_{set\text{-}up}$ is the minimum time before the transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D). Note that t_{hold} may be a negative number.

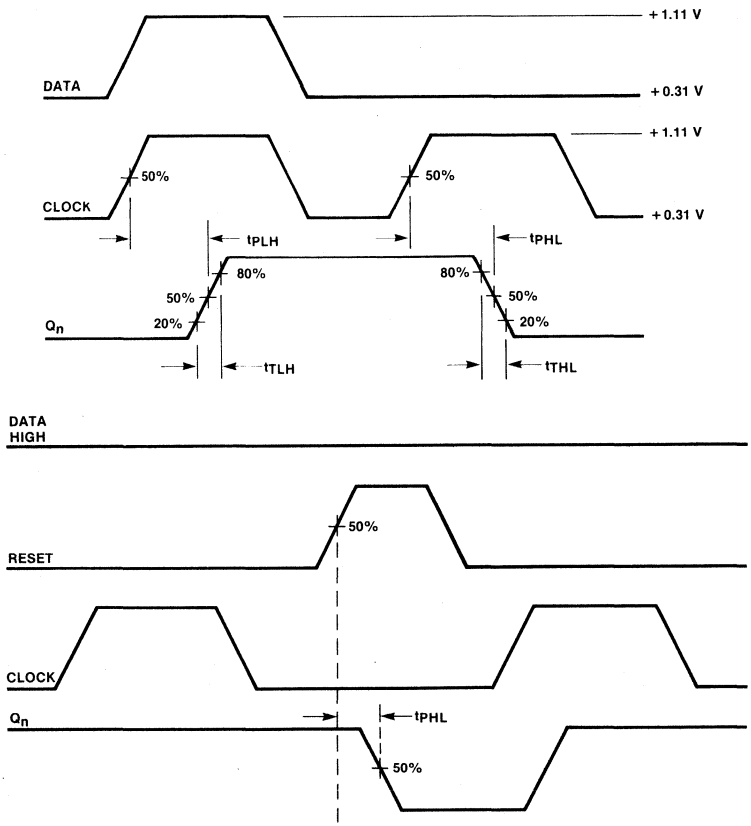


Fig. 1

F10192 • F10592

QUAD DIFFERENTIAL LINE DRIVER

F10K VOLTAGE COMPENSATED ECL

DESCRIPTION — The F10192 and F10592 contain four line drivers with complementary outputs. Each driver has a Data (D) input and shares an Enable ($\overline{E}$) input with another driver. The two driver outputs are the uncommitted collectors of a pair of npn transistors operating as a current switch. Each driver accepts 10K ECL input signals and provides a nominal signal swing of 800 mV across a 50 Ω load at each output collector. Outputs can drive higher values of load resistance, provided that the combination of IR drop and load return voltage (V_{LR}) does not cause an output collector to go more negative than −2.4 V with respect to V_{CC}. To avoid output transistor breakdown, the load return voltage should not be more positive than +5.5 V with respect to V_{CC}. When the $\overline{E}$ input is high, both output transistors of a driver are nonconducting. When not used, the $\overline{E}$ inputs, as well as the D inputs, may be left open. The F10192 is a pin compatible replacement for MC3463.

NOTE: To assure proper circuit operation during testing, as well as normal operation, a current path to a load return voltage has to be provided on all outputs.

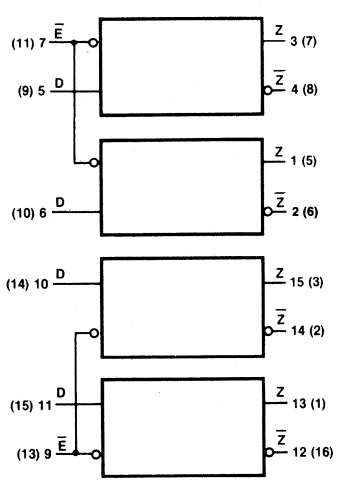
- **VOLTAGE COMPENSATED – NOISE MARGIN INSENSITIVE TO POWER SUPPLY VARIATIONS AND TRANSIENTS, RELAXED POWER SUPPLY REQUIREMENTS**
- **INTERNAL 50 kΩ (NOMINAL) INPUT PULL-DOWN RESISTORS – UNUSED INPUTS MAY BE LEFT OPEN**
- **OPEN COLLECTOR OUTPUTS DRIVE TERMINATED LINES OR TRANSFORMERS**
- **SINGLE V_{EE} POWER SUPPLY — −4.7 TO −6.2 V**
- **FULLY COMPATIBLE WITH OTHER 10,000 SERIES ECL**

TRUTH TABLE

INPUTS		OUTPUTS	
$\overline{E}$	D	Z	$\overline{Z}$
H	X	H	H
L	H	H	L
L	L	L	H

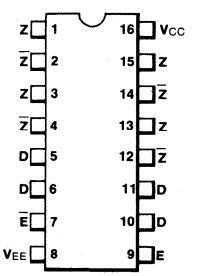
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LOGIC DIAGRAM



V_{CC} = Pin 16 (4)
V_{EE} = Pin 8 (12)
( ) = Flatpak

CONNECTION DIAGRAM
DIP
(TOP VIEW)



7

DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{OL}	Output Current LOW	13.5 14 14	16 16 16	18 18 19	mA	−55°C 25°C 125°C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table
I_{OH}	Output Current HIGH		0 0 0	2 2 2	mA	−55°C 25°C 125°C	Loading is 50 Ω to GND
I_{OHC}	Output Current HIGH			2 2 2	mA	−55°C 25°C 125°C	V_{IN} = V_{IHB} or V_{ILA} per Truth Table
I_{OLC}	Output Current LOW	13.5 14 14			mA	−55°C 25°C 125°C	Loading is 50Ω to GND
V_{LR}	Load Return Voltage Absolute Max Rating			+5.5	V	25°C	Guaranteed Max Return Voltage for Resistive Loads, Note 2
V_{OL}	Output Voltage LOW (Note 1)	−2.4			V	25°C	Guaranteed Min Output Voltage LOW
V_{IH}	Input Voltage HIGH	−1255 −1105 −1000		−880 −780 −630	mV	−55°C 25°C 125°C	Guaranteed Input Voltage HIGH for All Inputs
V_{IL}	Input Voltage LOW	−1920 −1850 −1820		−1510 −1475 −1400	mV	−55°C 25°C 125°C	Guaranteed Input Voltage LOW for All Inputs
I_{IH}	Input Current HIGH			220	μA	25°C	V_{IN} = V_{IHA}
I_L	Input Current LOW	0.5			μA	25°C	V_{IN} = V_{ILB}
I_{EE}	Power Supply Current	−140	−110		mA	25°C	Inputs Open, Outputs Loaded with 50 Ω to GND

Note 1: Limitations on combination of load resistor and load return voltage. Refer to description.
Note 2: The value listed is an absolute maximum rating, do not exceed.

DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
I_{OL}	Output Current LOW	13.5 14 14	16 16 16	18 18 19	mA	0°C 25°C 75°C	V_{IN} = V_{IHA} or V_{ILB}	
I_{OH}	Output Current HIGH		0 0 0	2 2 2	mA	0°C 25°C 75°C	per Truth Table	Loading is 50 Ω to GND
I_{OHC}	Output Current HIGH			2 2 2	mA	0°C 25°C 75°C	V_{IN} = V_{IHB} or V_{ILA}	
I_{OLC}	Output Current LOW	13.5 14 14			mA	0°C 25°C 75°C	per Truth Table	
V_{LR}	Load Return Voltage Absolute Max Rating			+5.5	V	25°C	Guaranteed Max Return Voltage for Resistive Loads, Note 2	
V_{OL}	Output Voltage LOW (Note 1)	−2.4			V	25°C	Guaranteed Min Output Voltage LOW	
V_{IH}	Input Voltage HIGH	−1145 −1105 −1045		−840 −810 −720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	

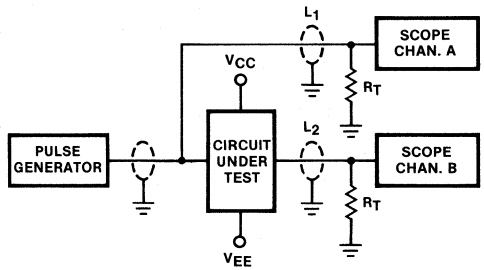
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND (Cont'd)

V_{IL}	Input Voltage LOW	– 1870 – 1850 – 1830		– 1490 – 1475 – 1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs
I_{IH}	Input Current HIGH			220	μA	25°C	$V_{IN} = V_{IHA}$
I_L	Input Current LOW	0.5			μA	25°C	$V_{IN} = V_{ILB}$
I_{EE}	Power Supply Current	– 140	– 110		mA	25°C	Inputs Open, Outputs Loaded with 50 Ω to GND

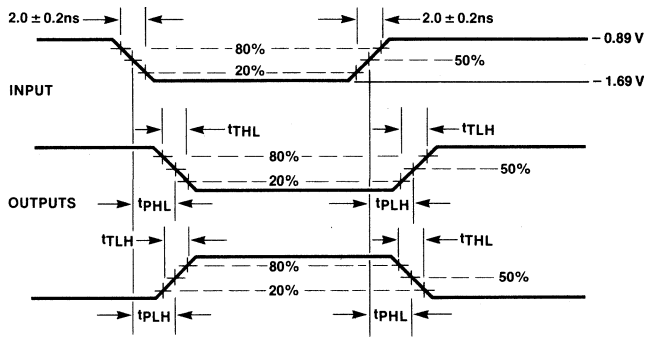
AC CHARACTERISTICS: V_{EE} = – 5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	2.5	3.5	6.0	ns	See Figure 1
t_{PHL} t_{PLH}	Propagation Delay D to Output	2.0	3.0	4.5	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)		1.5		ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)		1.5		ns	

AC TEST CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}



Jig set-up with no circuit under test
V_{CC} = GND
V_{EE} = −5.2 V

Fig 1

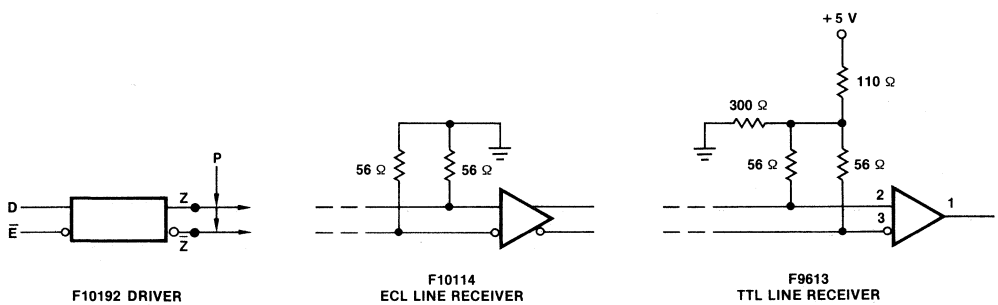


Fig. 2 Twisted Pair Interfacing with Either ECL or TTL Line Receivers

F10210 • F10211 • F10610 • F10611

DUAL 3-3 OR • DUAL 3-3 NOR

F10K VOLTAGE COMPENSATED ECL

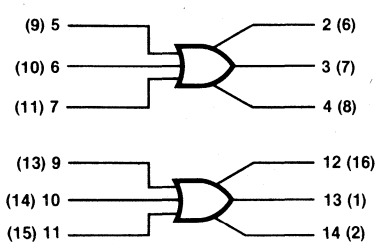
GENERAL DESCRIPTION — The F10210 and F10610 are Dual 3-Input 3-Output OR Gates and the F10211 and F10611 are Dual 3-Input 3-Output NOR Gates. Each gate has three output transistors driven in parallel, with their emitters brought out on separate leads. This provides the ability to drive three separate signal lines and minimizes propagation skew in critical timing situations, which cannot be done using three separate gates. The outputs of a gate can be paralleled to provide the extra drive required for such loads as a data bus terminated at both ends. The multiple outputs also allow each gate to participate in as many as three independent wired-OR functions, which enhances logic flexibility and minimizes package count.

- **VERY HIGH SPEED—1.5 ns TYP PER GATE**
- **VOLTAGE COMPENSATED—INSENSITIVE TO POWER SUPPLY VARIATIONS AND TRANSIENTS**
- **EMITTER-FOLLOWER OUTPUTS TO DRIVE TERMINATED LINES**
- **EXTRA V_{CC} PIN TO ELIMINATE NOISE COUPLING AND CROSSTALK**
- **INTERNAL 50 kΩ (NOMINAL) INPUT PULLDOWN RESISTORS—UNUSED INPUTS MAY BE LEFT OPEN**

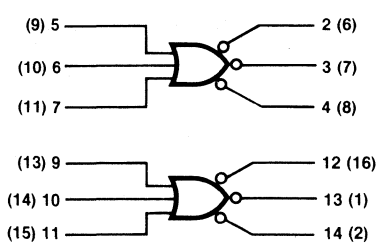
7

LOGIC DIAGRAMS

F10210/F10610



F10211/F10611



V_{CC1} = Pin 1, 15 (5, 3)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
( ) = Flatpak

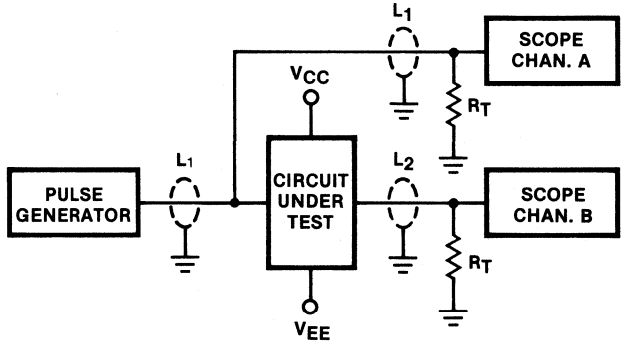
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

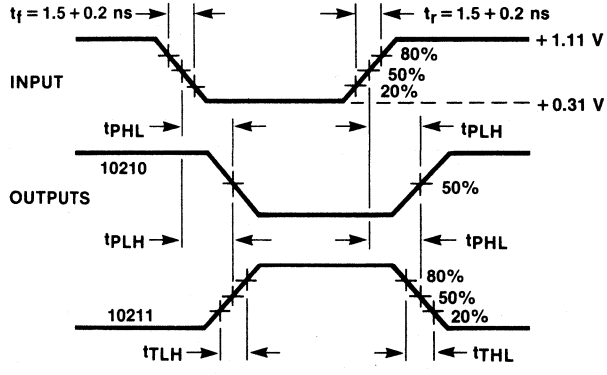
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH			410	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	−38	−31		mA	25°C	Inputs Open

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay	1.0	1.5	2.5	ns	See Figure 1
t_{TLH}, t_{THL}	Transition Time	1.0	1.5	2.5	ns	

SWITCHING TEST CIRCUIT AND WAVEFORMS





$V_{CC} = +2$ V, $V_{EE} = -3.2$ V
$R_T = 50\ \Omega$ termination of scope
$L_1 = L_2$ = equal length 50 Ω impedance lines
Decoupling 0.1 μF from V_{CC} and V_{EE} to gnd
Connect unused outputs through 50 Ω to gnd

Figure 1

F10231 • F10631

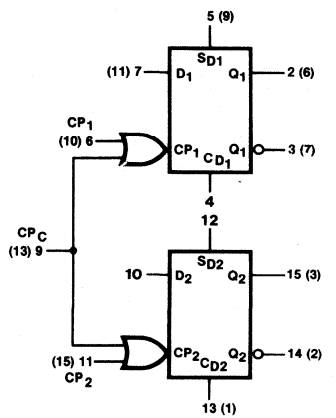
HIGH SPEED DUAL D FLIP-FLOP

F10K VOLTAGE COMPENSATED ECL

DESCRIPTION – The F10231/F10631 contains two master/slave D-type flip-flops. The internal clock is the OR of two clock inputs, one common to both flip-flops. The OR clock permits the use of one input as a clock pulse and the other as an active LOW enable. While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times.

Each flip-flop has separate set and clear inputs which asynchronously determine the state of the output independent of the clock levels. Note that the output voltage levels of a flip-flop are unpredictable if both set and clear signals are HIGH.

LOGIC SYMBOL



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
( ) = Flatpak

PIN NAMES

D_n	Data Input to Master
CP_n	Clock Input
CP_C	Common Clock Input
Q_n	Output
$\overline{Q}_n$	Complement Output
S_D	Set Direct Input
C_D	Clear Direct Input

TRUTH TABLES

SYNCHRONOUS OPERATION
D TABLE

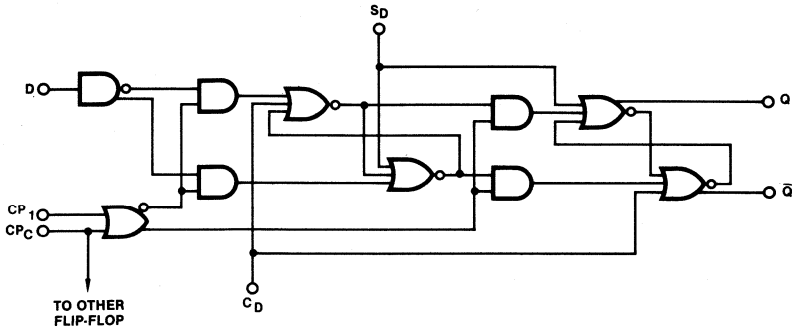
D	$Q_{(t+1)}$
L	L
H	H
$S_D = C_D$ = LOW	

(t + 1) = Time after positive going clock transition

ASYNCHRONOUS OPERATION
S_D C_D TABLE

C_D	S_D	Q	$\overline{Q}$
L	L	See D Table	See D Table
L	H	H	L
H	L	L	H
H	H	undetermined	

LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays, as many gate functions are achieved internally without incurring a full gate delay.

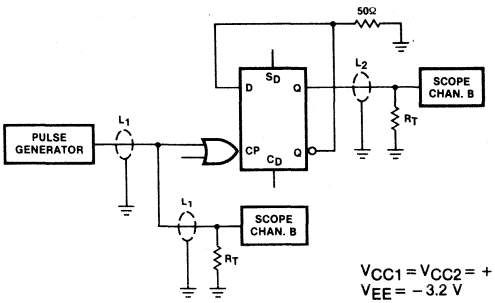
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

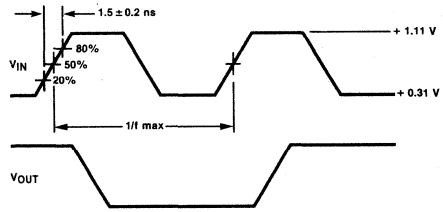
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH				μA	25°C	$V_{IN} = V_{IHA}$
	CP			220			
	CP_C			290			
	D			220			
	S_D & C_D			410			
I_{EE}	Power Supply Current	−65	−52		mA	25°C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
f_{TOG}	Toggle Frequency	200	225		MHz	See Figure 1
t_{PLH}, t_{PHL}	Propagation Delay, Clock to Output	1.5	2.0	3.3	ns	See Figures 2 & 3
t_{PLH}, t_{PHL}	Propagation Delay, S_D to Q, C_D to Q	1.1	2.0	3.3	ns	
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.0	1.3	3.1	ns	
t_s	Set-Up Time	1.0			ns	
t_h	Hold Time	0.75			ns	

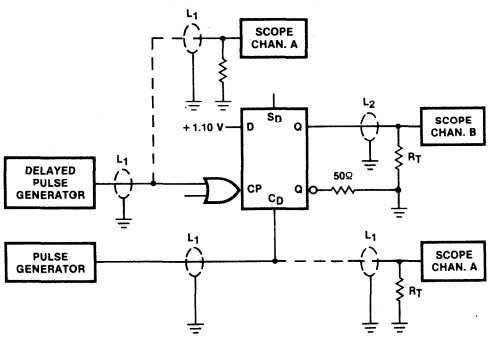
SWITCHING CIRCUITS AND WAVEFORMS

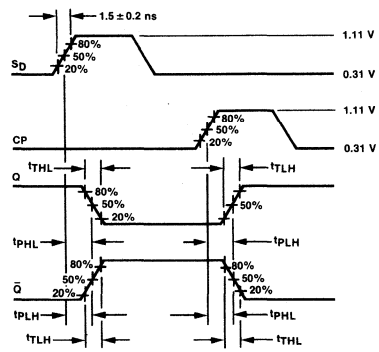




$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\ \Omega$ termination of scope
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}

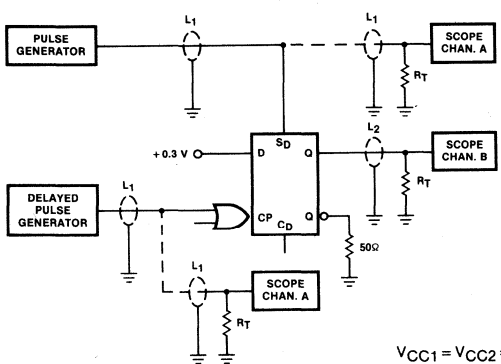
Fig. 1. Toggle Rate Test Circuit

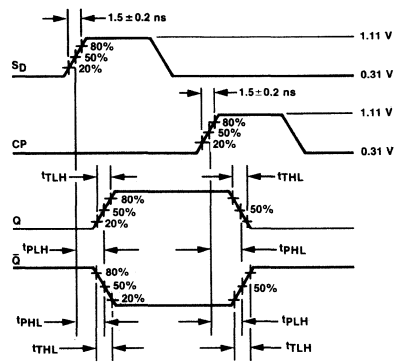




$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\ \Omega$ termination of scope
$L_1 = L_2$ = equal length 50 Ω impedance lines
All input transition times are 1.5 ± 0.2 ns

Fig. 2. Propagation Delay and C_D Test Circuit





$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\ \Omega$ termination of scope
$L_1 = L_2$ = equal length 50 Ω impedance lines
All input transition times are 1.5 ± 0.2 ns

Fig. 3. Propagation Delay and S_D Test Circuit

INTRODUCTION

1 ECL FOR HIGH PERFORMANCE SYSTEMS

2 ECL CIRCUIT BASICS

3 ECL LOGIC DESIGN

4 TRANSMISSION LINE CONCEPTS

5 ECL INTERCONNECTIONS

6 POWER DISTRIBUTION AND THERMAL CONSIDERATIONS

7 F10K SERIES DATA SHEETS

8 F95K SERIES DATA SHEETS

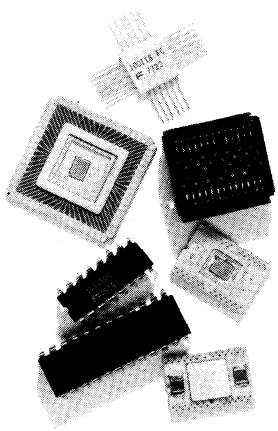
9 11C SERIES DATA SHEETS

10 F100K SERIES DATA SHEETS

11 ECL MEMORY DATA SHEETS

12 ORDER AND PACKAGE INFORMATION

13 FAIRCHILD FIELD SALES OFFICES, REPRESENTATIVES AND DISTRIBUTORS



F95K FULLY COMPENSATED ECL SERIES

GENERAL DESCRIPTION — Fairchild F95K Series Emitter Coupled Logic (ECL) circuits are high speed, low power logic intended for use in high speed systems such as central processors, memory controllers, peripheral equipment, instrumentation and digital communication systems.

The fully compensated F95K logic elements employ unique compensation networks which ensure that significant parameters such as logic levels, noise margin and propagation delay remain constant over a wide range of temperature and power supply variations.

The 95K series elements have the same lead assignments and logic functions as their 10,000 series counterparts, allowing either selective substitution of F95K elements to eliminate problems in thermal hot-spots or total substitution to upgrade overall system performance.

The series employs Emitter Coupled Logic to achieve typical gate delays of 2 ns at typical power levels of 25 mW/gate. The nominal power supply is specified as V_{EE} equal to −5.2 V. All devices, however, may be operated over V_{EE} ranges of −4.7 to −6.2 V with negligible loss of noise immunity. Some SSI gates may be operated over a V_{EE} range of −3.5 to −6.2 V, again with a negligible loss of noise immunity, due to the built-in voltage regulator.

High input impedance (typically 50 kΩ) and open outputs allow effective usage of series or parallel terminated line techniques and large numbers of OR-ties.

In accordance with standard IC practice, commercial F95K devices are specified over 0°C to 75°C temperature range.

- **Very high speed . . . typically 2 ns per gate.**
- **Low power dissipation . . . typically 25 mW per gate.**
- **Voltage compensated . . . noise margin insensitive to power supply variations and transients, relaxed power supply requirements.**
- **Internal 50 kΩ (nominal) input pull down resistors . . . unused inputs may be left open.**
- **Open emitter-follower outputs drive terminated lines.**
- **Separate V_{CC} pins eliminate noise coupling.**
- **Single V_{EE} power supply . . . −4.7 to −6.2 V.**
- **Wired-OR capability.**
- **Complementary, simultaneous outputs.**
- **Temperature compensated . . . logic levels, noise margins and propagation delays remain constant over a wide range of temperature variations and gradients.**
- **Simplified customer and vendor specification and testing . . . air flow and warm-up not required to guarantee proper logic levels.**
- **Lowered cooling cost . . . wide temperature gradients between devices does not affect logic levels and noise margin.**

RECOMMENDED OPERATING AND TEST CONDITIONS — The Fairchild F95K series operates in both still or forced air systems where an ambient temperature of 0°C to 75°C is maintained. The required cooling is determined solely by this ambient temperature requirement. There is no need to maintain a constant temperature throughout the system.

The required system voltage at V_{EE} pins is −4.7 to −6.2 V. With a load on all outputs of 50Ω to −2.0 V and a 0°C to a 75°C temperature range, the device dc parameters are guaranteed for a nominal V_{EE} of −5.2 V. With the same operation conditions, the worst case dc parameters are guaranteed for any V_{EE} value from −4.7 to −6.2 V.

The F95K ac switching characteristics are guaranteed at V_{EE} = −5.2 V over the operating ambient temperature range of 0°C to 75°C. The ac test parameters shown use a 50Ω load to −2.0 V.

Since the F95K devices are relatively insensitive to variations in junction temperature, testing may be performed on almost any available digital integrated circuit tester. No power warm-up or moving air cooling is required to assure the specified device characteristics.

ABSOLUTE MAXIMUM RATINGS

(Non-operating, above which usefull life may be impaired)

Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−8 V
Input Voltage	Gnd to V_{EE}
Output Current	−50 mA

FUNCTIONAL DESCRIPTION

F95K offers many high speed system design advantages. High speed is achieved by using small, low capacitance device geometries and operating the transistors between the active and off modes, thereby avoiding saturation. The basic ECL gate is shown in *Figure 1.*

If the input voltages are more negative than V_{BB}, Q1 and Q2 are cut off and Q3 conducts, holding the collector of Q3 LOW. If either input is more positive than V_{BB}, Q1 or Q2 will conduct and Q3 will be cut off, raising its collector voltage. Since one or more transistors are always conducting, there is a constant current drain, independent of frequency which eliminates sharp switching transients and frequency dependent power dissipation effects. The outputs of the circuit are emitter-followers, Q4 and Q5. They provide low impedance drive to terminated lines and voltage shifting to levels compatible with the inputs. The basic gate simultaneously performs the positive logic OR and NOR functions, providing both true and complement outputs within a single gate delay period. The outputs of several gates may be tied to provide a wired-OR function. An external load resistor must be provided in all cases.

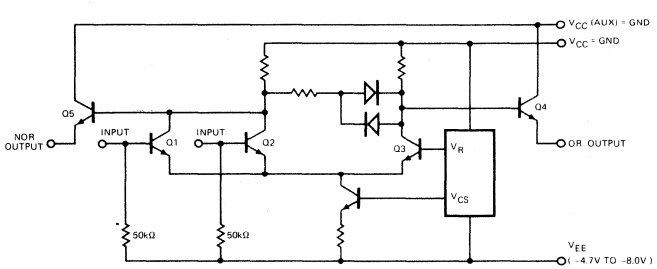


Fig. 1

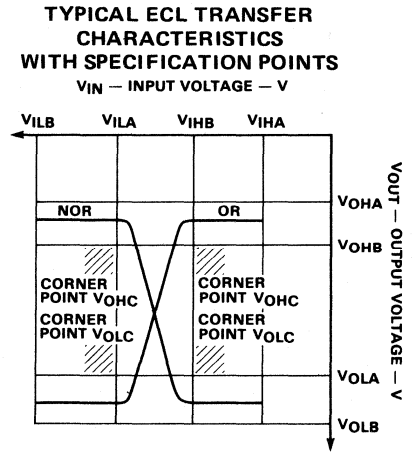
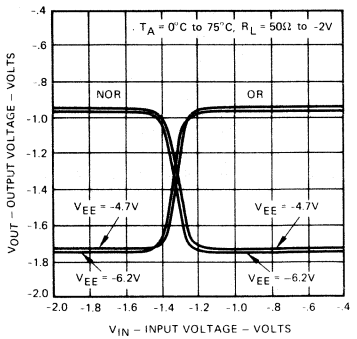


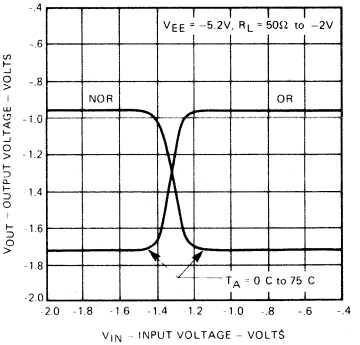
Fig. 2

TYPICAL F95K SERIES CHARACTERISTICS

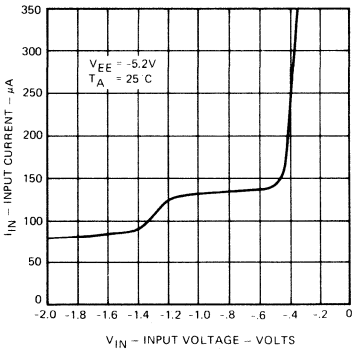
INPUT/OUTPUT TRANSFER CHARACTERISTICS VERSUS SUPPLY VOLTAGE



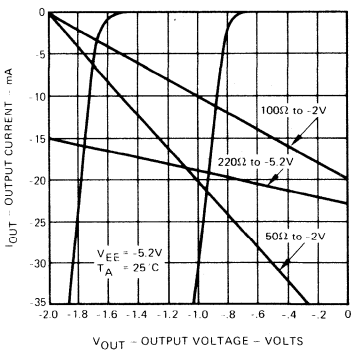
INPUT/OUTPUT TRANSFER CHARACTERISTICS VERSUS TEMPERATURE



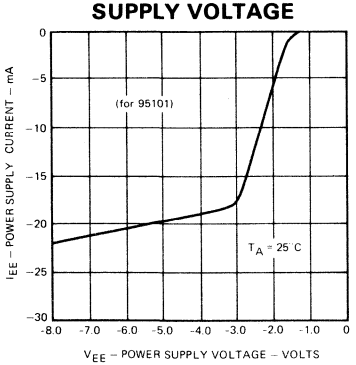
INPUT CHARACTERISTIC



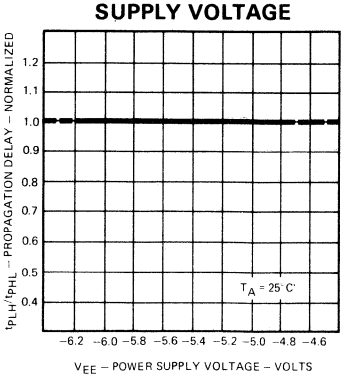
OUTPUT CHARACTERISTICS VERSUS TYPICAL OUTPUT TERMINATIONS



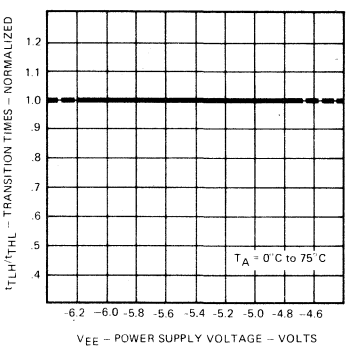
CHANGE IN POWER SUPPLY CURRENT WITH RESPECT TO CHANGE IN POWER SUPPLY VOLTAGE



PROPAGATION DELAY VARIATION VERSUS SUPPLY VOLTAGE



OUTPUT TRANSITION TIME VARIATION VERSUS SUPPLY VOLTAGE

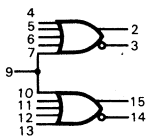


8

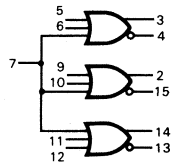
LOGIC DIAGRAMS

V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

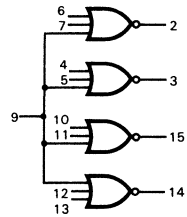
F95002



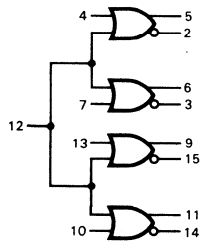
F95003



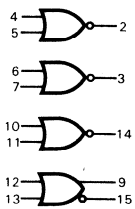
F95004



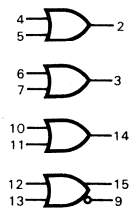
F95101



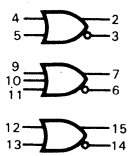
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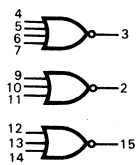
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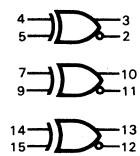
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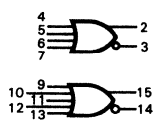
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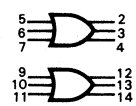
F95107



F95109

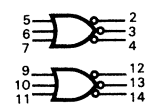


F95110



NOTE: V_{CC1} = 1, 15
V_{CC2} = 16

F95111



NOTE: V_{CC1} = 1, 15
V_{CC2} = 16

F95002 • F95003 • F95004 • F95101 • F95102 • F95103 • F95105 • F95106 • F95107 • F95109 • F95110 • F95111

DC CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1025	-965	-880	mV	V_{IN} = V_{IHA} or V_{ILB} per Logic Function	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	V_{IN} = V_{IHB} or V_{ILA} per Logic Function	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input LOW for All Inputs	
I_H	Input Current HIGH F95002 Pin 9 F95003 Pin 7 F95004 Pin 9 F95101 Pin 16 F95110,F95111 All Inputs			265 345 430 550 550 430	μA	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			μA	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current F95002,F95109 F95003,F95105,F95106 F95004,F95101,F95102,F95103 F95107 F95110 F95111	 -14 -21 -26 -28 -35 -38	 -10 -15 -18 -19 -25 -27		mA	Inputs & Outputs Open	

DC CHARACTERISTICS: V_{EE} = -4.7 to -6.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS	
V_{OHC}	Output Voltage HIGH	-1050			mV	V_{IN} = V_{IHB} or V_{ILA} per Logic Function	Loading is 50 Ω to -2.0 V
V_{OLC}	Output Voltage LOW			-1595	mV		
V_{IH}	Input Voltage HIGH	-1155			mV	Guaranteed input HIGH for All Inputs	
V_{IL}	Input Voltage LOW			-1500	mV	Guaranteed Input LOW for All Inputs	
I_{EE}	Power Supply Current F95002,F95109 F95003,F95105,F95106 F95004,F95101,F95102,F95103 F95107 F95110,F95111	 -15 -22.5 -27.5 -30 -41	 -11 -11 -19 -21 -28		mA	Inputs & Outputs Open V_{EE} = -6.2 V	

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SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND, T_A = 0°C to 75°C

F95002 • F95003 • F95004 • F95101 • F95102 • F95103 • F95105 • F95106 • F95109

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay, LOW to HIGH	1.0	2.0	3.1	ns	See Figure 1.
t_{PHL}	Propagation Delay, HIGH to LOW	1.0	2.0	3.1	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.0	3.6	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.0	3.6	ns	

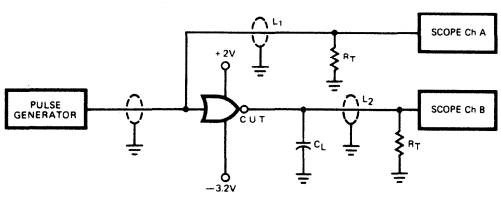
SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C **F95107**

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay LOW to HIGH	1.1	2.5	4.0	ns	See Figure 1.
t_{PHL}	Propagation Delay HIGH to LOW	1.1	2.5	4.0	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.5	3.8	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.5	3.8	ns	

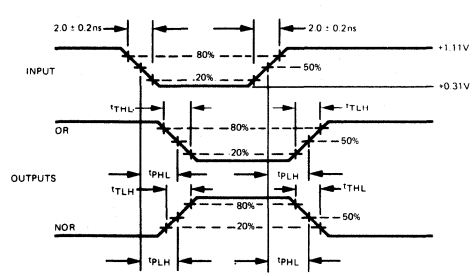
SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C **F95110 • F95111**

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}	Propagation Delay LOW to HIGH	1.4	2.5	3.8	ns	See Figure 1.
t_{PHL}	Propagation Delay HIGH to LOW	1.4	2.4	3.8	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.2	3.8	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.2	3.8	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}



Jig set-up with no circuit under test
$V_{CC1} = V_{CC2}$ = +2.0 V
V_{EE} = -3.2 V

Fig. 1.

F95000

4-BIT SHIFT REGISTER

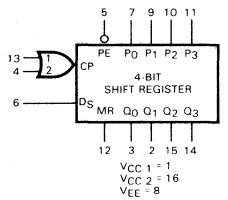
GENERAL DESCRIPTION — The F95000 is a 4-Bit Parallel/Serial In, Parallel/Serial Out Shift Register. High Speed ECL technology permits storage, shifting, counting and serial code conversion at rates in excess of 200 MHz.

Features include assertion outputs for each stage, overriding asynchronous master reset, serial and parallel D type inputs and a gated clock. Availability of these features on one chip significantly improves the reliability, performance, and power consumption of high speed systems.

The F95000 incorporates a unique temperature and voltage compensation network which ensures that significant parameters such as logic levels, noise margins and speed remain constant over a wide range of temperature and power supply voltage.

- **HIGH SPEED . . . 200 MHz TYPICAL SHIFT FREQUENCY**
- **D TYPE INPUTS SERIAL AND PARALLEL**
- **GATED CLOCK INPUT**
- **ASYNCHRONOUS MASTER RESET**
- **TERMINATED LINE DRIVE CAPABILITY**
- **WIRED-OR CAPABILITY**
- **SEPARATE V_{CC} PINS ELIMINATE NOISE COUPLING**
- **50 kΩ INPUT PULL DOWNS . . . UNUSED INPUTS MAY BE LEFT OPEN**
- **SINGLE V_{EE} POWER SUPPLY . . . -4.7 V TO -6.2 V**
- **NOISE MARGINS INSENSITIVE TO POWER SUPPLY OR TEMPERATURE VARIATIONS AND GRADIENTS**

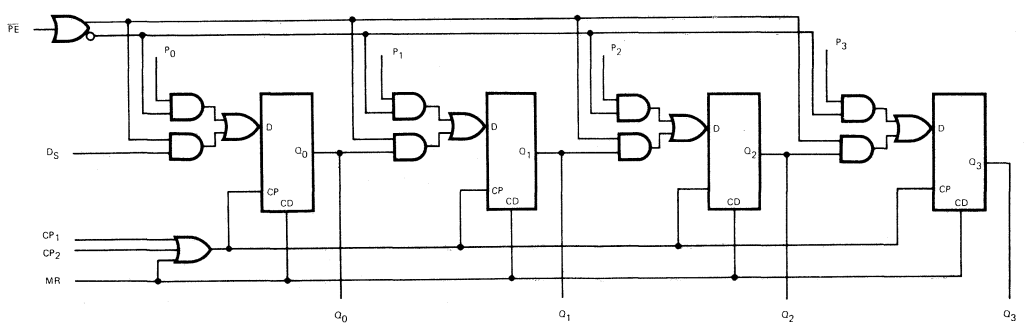
LOGIC SYMBOL



PIN NAMES

P_n	Parallel Data Inputs
$\overline{PE}$	Parallel Enable (Active LOW)
CP_n	Clock In, Shifts on Positive Transition
MR	Asynchronous Master Reset (Active HIGH)
D_S	Data Input, Serial
Q_n	Register Outputs

LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

FUNCTIONAL DESCRIPTION — The F95000 is a high speed 4-Bit Shift Register. It consists of four master/slave flip-flops and four 2-input multiplexers interconnected so as to permit loading of the masters from either a preceding slave output (Q_{n-1}) or an external (P_n) input. The function desired is selected by the Parallel Enable ($\overline{PE}$) input.

The masters are loaded during the LOW period of the clock ($CP_{1,2}$). As the clock changes from LOW to HIGH, the masters are inhibited from change followed by the enabling of the data path from master to slave. This data is then presented at the outputs (Q_n). While the clock is HIGH, the masters are inhibited from change and the master/slave data path remains open. During the HIGH to LOW transition of the clock, the master/slave data path is inhibited. This is followed by the enabling of the masters for the acceptance of data from the parallel or serial logic inputs.

As the two clock inputs ($CP_{1,2}$) are ORed together, both must be LOW for the masters to accept new data. If either is raised to a HIGH, the register is clocked.

A HIGH on one clock input can prevent the register from shifting, providing a hold condition. To prevent false triggering, this input must change from LOW to HIGH while the clock is HIGH.

The Master Reset (MR) function is asynchronous. When held HIGH, it overrides all other commands and forces all outputs (Q_n) LOW.

TRUTH TABLES

MODE SELECT

MR	$\overline{PE}$	CP_1	CP_2	MODE
H	X	X	X	RESET (ALL OUTPUTS LOW)
L	L	L	⌐¬	PARALLEL LOAD
L	L	⌐¬	L	PARALLEL LOAD
L	H	L	⌐¬	SHIFT RIGHT (SERIAL LOAD)
L	H	⌐¬	L	SHIFT RIGHT (SERIAL LOAD)
L	X	H	X	HOLD
L	X	X	H	HOLD

SERIAL LOAD

D_S	$Q_{O(t+1)}$
H	H
L	L

PARALLEL LOAD

P_n	$Q_{n(t+1)}$
H	H
L	L

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

⌐¬ = Clock Pulse (LOW to HIGH)

(t+1) = Time after positive going clock transition

DC CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1025	-965	-880	mV	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input LOW Voltage for All Inputs	
I_{IH}	Input Current HIGH MR (Lead 12)			265 700	μA	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			μA	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	-85	-66		mA	Outputs Open, Pins 12 & 13 Tied to V_{IH}	

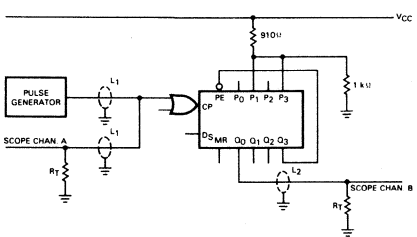
DC CHARACTERISTICS: V_{EE} = -4.7 to -6.2 V, T_A = 0°C to 75°C, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	-1050			mV	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW			-1595	mV		
V_{IH}	Input Voltage HIGH	1155			mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW			-1500	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{EE}	Power Supply Current	-95	-80		mA	Outputs Open, Pins 12 & 13 Tied to V_{IH}, V_{EE} = -6.2 V	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
f_{count}	Shift Right Frequency	150	200		MHz	See Figure 3
t_{PLH}	Propagation Delay Clock to Output	2.0	3.2	5.0	ns	See Figure 1
t_{PHL}	Propagation Delay Clock to Output	2.0	3.2	5.0	ns	
t_{PHL}	Propagation Delay Master Reset to Output		2.5		ns	See Figure 2
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.3	2.0	3.5	ns	See Figure 1
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.3	2.0	3.5	ns	
t_w	Clock Pulse Width		2.5		ns	See Figure 3
t_w	MR Pulse Width		3.5		ns	
t_s	Set-Up Time Prior to Clock D_S to CP, P_n to CP	1.5	0.5		ns	
t_h	Hold Time After Clock D_S to CP, P_n to CP	1.0	-0.5		ns	
t_s	Set-Up Time Prior to Clock $\overline{PE}$ to CP	5.4	3.2		ns	
t_h	Hold Time After Clock $\overline{PE}$ to CP	0	-3.2		ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 = L_2 = 50Ω impedence lines
V_{CC} = +2.0 V, pins 1 and 16
V_{EE} = -3.2 V, pins 8
R_T = 50Ω termination of scope
f = 10 MHz
Pulse Width = 10 ns

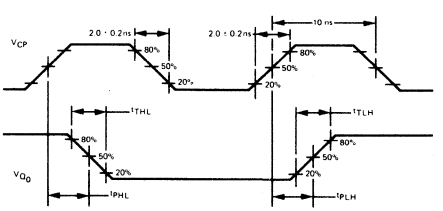
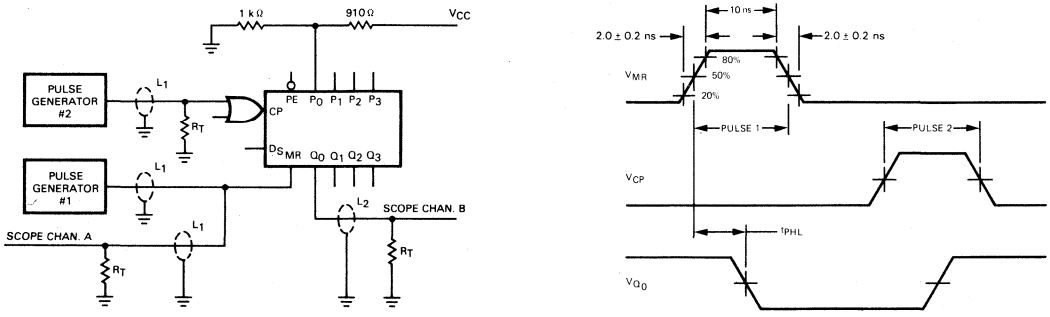


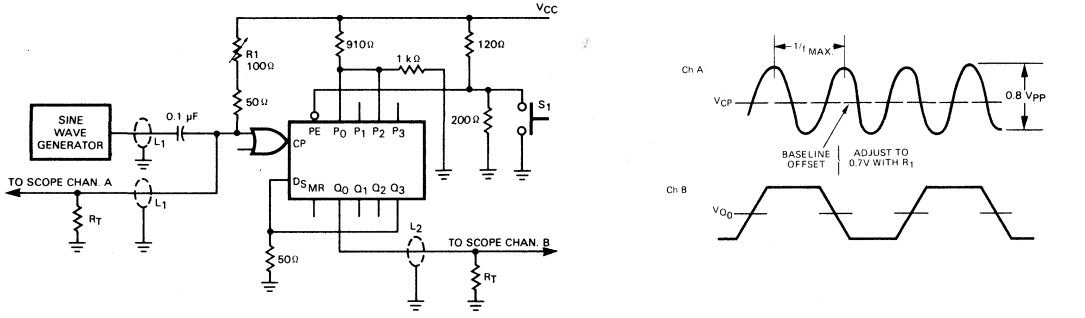
Fig. 1. Clock to Output, Output Transition Time

SWITCHING CIRCUIT AND WAVEFORMS (Cont'd)



$L_1 = L_2 = 50\Omega$ impedance lines.
$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\Omega$ termination of scope
f = 10 MHz
Pulse 2 ≃ Pulse 1

Fig. 2. Master Reset to Output

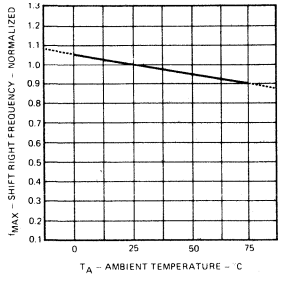


$L_1 = L_2 = 50\Omega$ impedance lines
$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\Omega$ termination of scope
$f = f_{MAX}$
Load the register by closing S_1

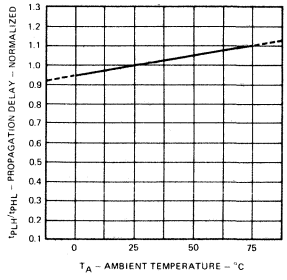
Fig. 3. Shift Frequency

TYPICAL ELECTRICAL CHARACTERISTICS

SHIFT RIGHT FREQUENCY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS TEMPERATURE



F95010 • F95016

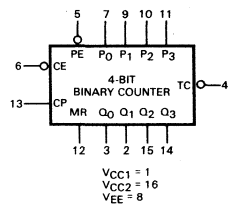
BCD DECADE COUNTER/4-BIT BINARY COUNTER

GENERAL DESCRIPTION — The F95010 is a high speed synchronous, presettable, cascadable BCD Decade Counter and the F95016 is a high speed synchronous, presettable, cascadable 4-Bit Binary Counter. They are multifunction MSI building blocks useful for a large number of counting, digital integration, and conversion applications. Up to nine devices can be cascaded with no speed degradation using standard 95K gates. A multidecade synchronous counter up to 150 MHz can be built. Typical count frequency is 200 MHz.

Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.

- **HIGH SPEED COUNT . . . 200 MHz TYPICAL COUNT FREQUENCY**
- **INTERNAL COUNT ENABLE — FOR HIGHEST SPEED EXPANSION**
- **ASYNCHRONOUS MASTER RESET**
- **50Ω DRIVE CAPABILITY**
- **WIRED-OR CAPABILITY**
- **SEPARATE V_{CC} PINS — ELIMINATE NOISE COUPLING**
- **INTERNAL 50 kΩ INPUT PULL DOWNS**
- **SINGLE -5.2 V POWER SUPPLY**

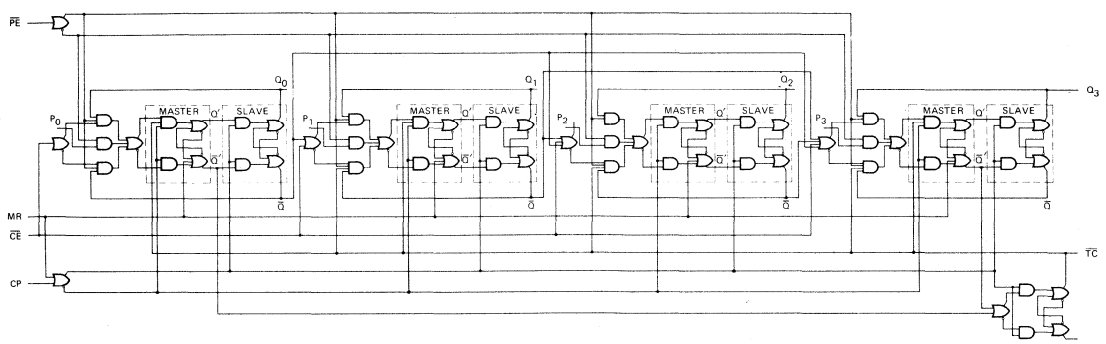
LOGIC SYMBOL



PIN NAMES

$\overline{PE}$	Parallel Load Enable (Active LOW)
P_n	Parallel Inputs
CP	Clock Input (Clocks on Positive Transition)
$\overline{CE}$	Count Enable (LOW to Count)
MR	Master Reset (HIGH Forces all Q Outputs LOW)
$\overline{TC}$	Terminal Count (95010, LOW at HLLH; 95016 LOW at HHHH)
Q_n	Counter Outputs

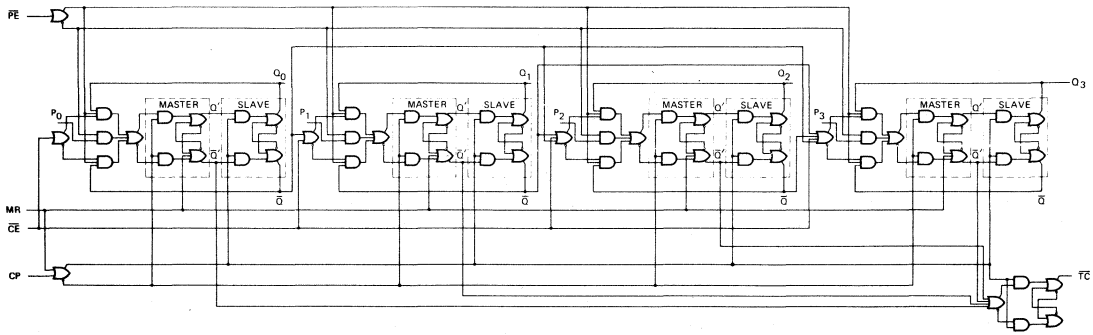
LOGIC DIAGRAM F95010



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

8

LOGIC DIAGRAM F95016



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

FUNCTIONAL DESCRIPTION — The F95010 is a high speed BCD Decade Counter and the F95016 is a high speed Binary Counter. The four master/slave flip-flops are fully synchronous and are driven in parallel through a clock driver. The masters are loaded during the LOW period of the clock pulse. During the LOW to HIGH transition of the clock, the master is disabled from the input and data is transferred to the slaves and then to the outputs. When the clock is HIGH, the masters are inhibited from changing and the master/slave data path remains open. During the HIGH to LOW transition of the clock, the master/slave data path is inhibited, followed by the enabling of the masters for the acceptance of inputs from the counting logic, parallel entry, or count hold logic.

The Terminal Count ($\overline{TC}$) is generated at count 9 (HLLH) on the 95010 and at count 15 (HHHH) on the 95016.

The $\overline{TC}$ output is available simultaneously with the Q outputs through the use of unique lookahead logic and a fifth slave which is loaded during the LOW portion of the clock cycle. This feature, in conjunction with the triggered Count Enable ($\overline{CE}$) and the Parallel Enable ($\overline{PE}$) select the mode of operation as shown in the table below. The status of these control lines is sampled only during the LOW to HIGH transition of the clock.

The Master Reset (MR) function is asynchronous. When HIGH, it overrides all other commands and forces all Q outputs LOW and the $\overline{TC}$ HIGH.

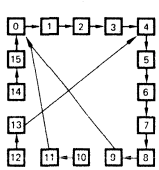
TRUTH TABLE

$\overline{CE}$	$\overline{PE}$	MR	CP	Function
L	L	L	⎍	Load Parallel (P_n to Q_n)
H	L	L	⎍	Load Parallel (P_n to Q_n)
L	H	L	⎍	Count
H	H	L	⎍	Hold
X	X	L	⎏	Masters Respond, Slaves Hold
X	X	H	X	Reset (Q_n = LOW, $\overline{TC}$ = HIGH)

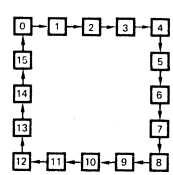
L = LOW
H = HIGH Voltage Level
X = Don't Care
⎍ = Clock Pulse (LOW to HIGH)
⎏ = Clock Pulse (HIGH to LOW)

STATE DIAGRAMS

F95010



F95016



NOTE: The 95010 can be preset to any state, but will not count beyond 9 (HLLH). If preset to state 10, 11, 12, 13, 14 or 15, it will return to its normal sequence within two clock pulses.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE: V_{EE} = -5.2 V, T_A = 0°C to 75°C

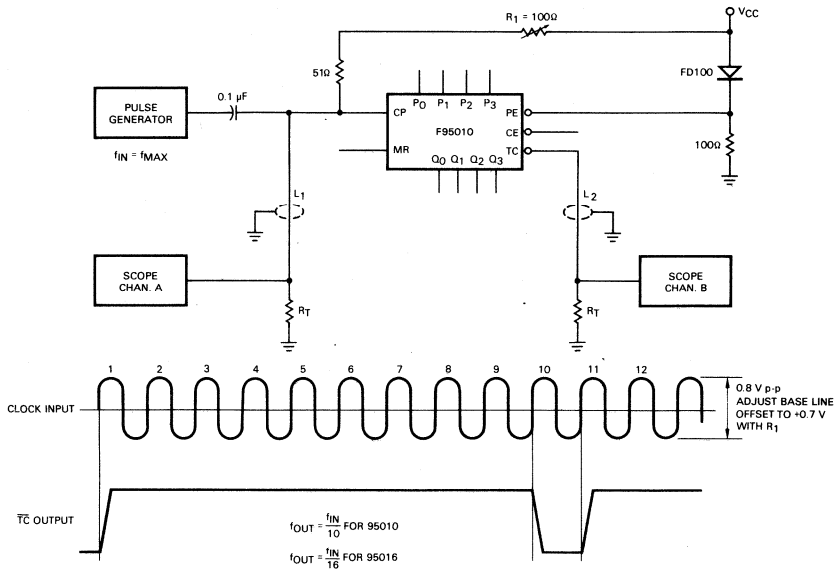
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	-1025	-965	880	mV	50 Ω to -2.0 V	V_{IN} = V_{IHA} or V_{ILB} per Truth Table
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV	50 Ω to -2.0 V	
V_{OHC}	Output Voltage HIGH	-1035			mV	50 Ω to -2.0 V	V_{IN} = V_{IHB} or V_{ILA} per Truth Table
V_{OLC}	Output Voltage LOW			-1610	mV	50 Ω to -2.0 V	
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input LOW for All Inputs	
I_{IH}	Input Current HIGH, MR (Pin 12)			265 700	μA μA	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			μA	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	-115	-80		mA	MR to V_{IH}, Other Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
f_{count}	Count Frequency	140	200		MHz	See Figure 1
t_{PLH}	Propagation Delay Clock to Output (Q_n or $\overline{TC}$)	2.0	3.6	5.0	ns	See Figure 2
t_{PHL}	Propagation Delay Clock to Output (Q_n or $\overline{TC}$)	2.0	3.6	5.0	ns	
t_{PHL}	Propagation Delay Master Reset to Output		4.0		ns	See Figure 3
T_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.3	2.5	3.3	ns	See Figure 2
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.3	2.5	3.3	ns	
t_w	Clock Pulse Width		2.3		ns	See Figure 2
t_w	MR Pulse Width		2.8		ns	See Figure 3
t_s	Set-Up Time Prior to Clock P_n to CP	2.0			ns	
t_s	Set-Up Time Prior to Clock $\overline{PE}$ or $\overline{CE}$ to CP	2.5			ns	
t_h	Hold Time After Clock $\overline{PE}$ or $\overline{CE}$ to CP	0.5			ns	

8

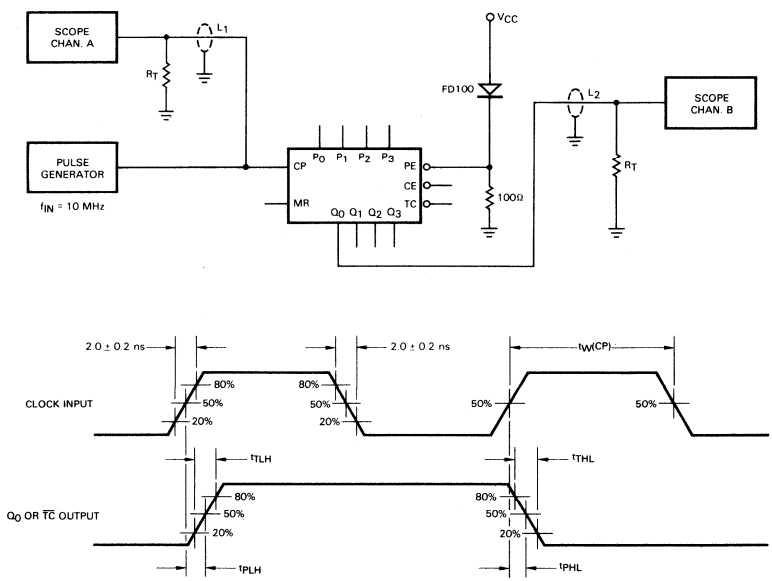
SWITCHING CIRCUITS AND WAVEFORMS



L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 1. Maximum Count Frequency

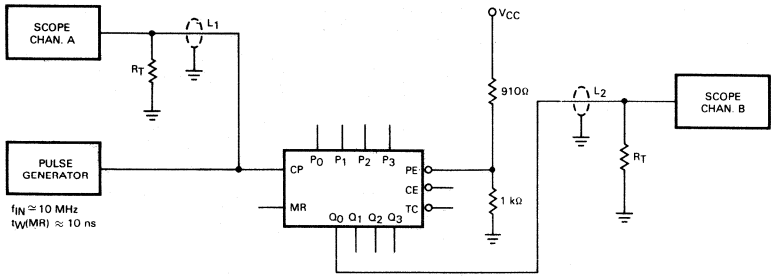


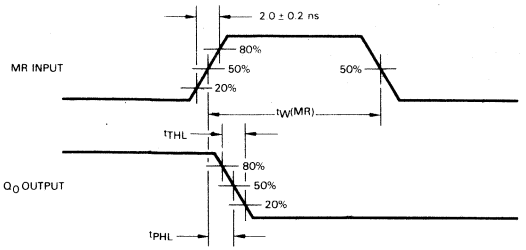
L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 2. Clock to Output

SWITCHING CIRCUITS AND WAVEFORMS (Cont'd.)



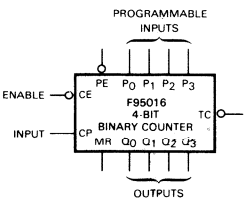


L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

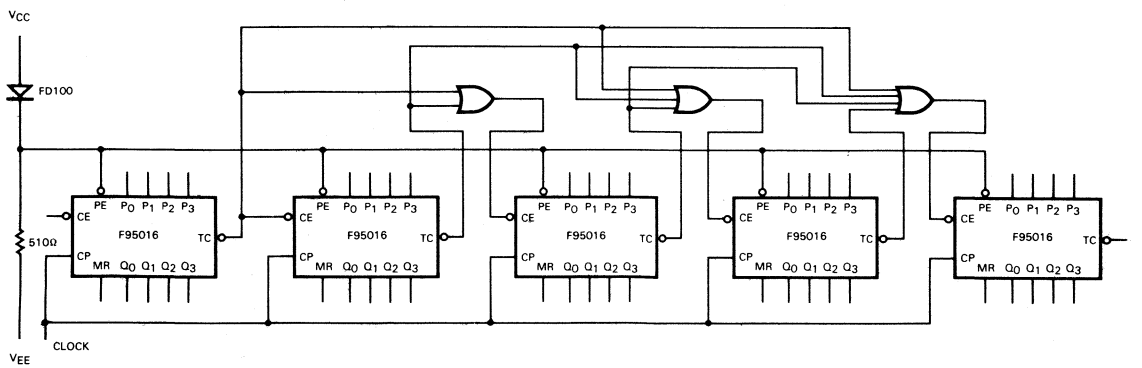
Fig. 3. Master Reset to Output

APPLICATION INFORMATION



DIVIDE RATIO	INPUT REQUIRED P_0	P_1	P_2	P_3
2	L	H	H	H
3	H	L	H	H
4	L	L	H	H
5	H	H	L	H
6	L	H	L	H
7	H	L	L	H
8	L	L	L	H
9	H	H	H	L
10	L	H	H	L
11	H	L	H	L
12	L	L	H	L
13	H	H	L	L
14	L	H	L	L
15	H	L	L	L
16	L	L	L	L

The F95016 may be connected to divide by any modulo from 2 to 16. The table illustrates the inputs required for each modulo. The terminal count output is utilized to load the parallel data, this in turn determines the number of clock pulses which will occur before $\overline{TC}$ goes LOW again.



CASCADE COUNTERS USING OR GATES FOR CARRY PROPAGATION

F95029

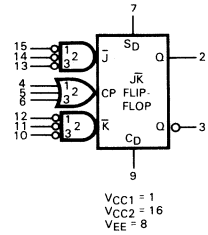
EDGE-TRIGGERED $\overline{J}$ $\overline{K}$ FLIP-FLOP

DESCRIPTION — The F95029 is a very high speed Edge-Triggered $\overline{J}$ $\overline{K}$ Flip-Flop designed for maximum speed. The multiple $\overline{J}$, $\overline{K}$, and clock inputs permit its use in most register and counter applications without extra gates. Careful control of clock pulse rise and fall times is not required, as the master/slave design has a dc threshold on the clock input which initiates the transition on the output.

Data is accepted by the master while the clock is LOW. Data present just prior to the rising edge of the clock (as specified by the set-up and hold times) is trapped in the master and transferred to the slave on the rising edge of the clock. Although this device uses a master/slave design, it is not "ones catching" (it responds only to the rising edge of the clock pulse).

The asynchronous inputs provide ability to control the state of the flip-flop independent of the conditions of the clock and synchronous inputs. Both asynchronous set and clear are provided.

LOGIC SYMBOL



PIN NAMES

$\overline{J}$	Synchronous Set Input (Active LOW)
$\overline{K}$	Synchronous Reset Input (Active LOW)
CP	Clock Input
S_D	Asynchronous Set Input
C_D	Asynchronous Clear Input
Q	True Output
$\overline{Q}$	Complement Output

TRUTH TABLES

SYNCHRONOUS

$\overline{J}_1$	$\overline{J}_2$	$\overline{J}_3$	$\overline{K}_1$	$\overline{K}_2$	$\overline{K}_3$	Q_{t+1}
L	L	L	L	L	L	$\overline{Q}_t$
L	L	L	One or More HIGH			H
One or More HIGH			L	L	L	L
One or More HIGH			One or More HIGH			Q_t

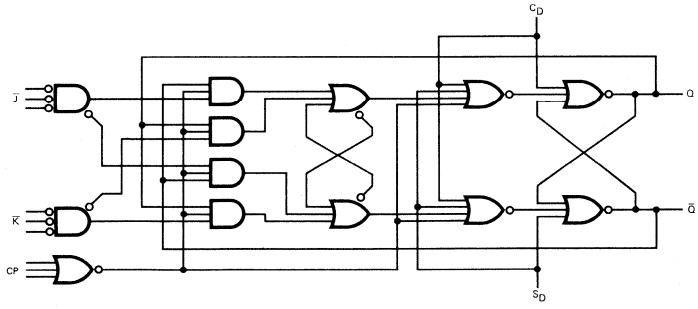
ASYNCHRONOUS

C_D	S_D	Q
L	L	Sync
L	H	H
H	L	L
H	H	Undetermined

L = LOW Voltage Level
H = HIGH Voltage Level

Q_t = Present Output State
Q_{t+1} = Output State after next Clock

LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays, as many gate functions are achieved internally without incurring a full gate delay.

DC CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	-1025	-965	-880	mV	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			340	µA	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			µA	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	-46	-36		mA	CP to V_{IL}, Other Inputs & Outputs Open	

DC CHARACTERISTICS: V_{EE} = -4.7 to -6.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OHC}	Output Voltage HIGH	-1050			mV	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	Loading is 50Ω to -2.0 V
V_{OLC}	Output Voltage LOW			-1595	mV		
V_{IH}	Input Voltage HIGH	-1155			mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW			-1500	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{EE}	Power Supply Current	-52	-40		mA	CP to V_{IL}, Other Inputs & Outputs Open V_{EE} = -6.2 V	

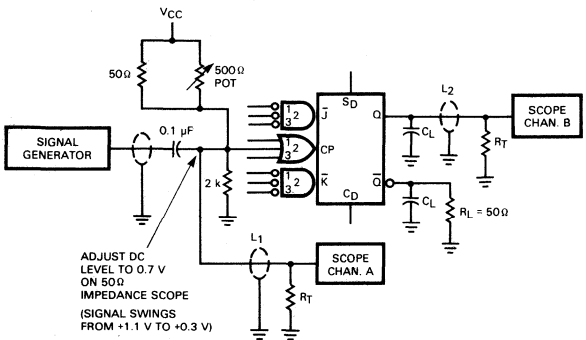
SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 75°C

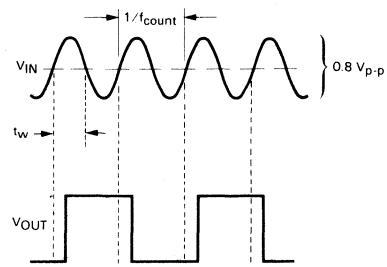
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
f_{count}	Toggle Frequency	160	250		MHz	See Figure 1
t_{PHL}, t_{PHL}	Propagation Delay Clock to Output	1.6	2.8	4.4	ns	See Figure 2
t_{PLH}, t_{PHL}	Propagation Delay S_D, C_D to Output	1.1	3.6	6.3	ns	See Figure 3
t_{TLH} t_{THL}	Output Transition Time 20% to 80%, 80% to 20%	0.9	2.0	3.3	ns	See Figure 2

SWITCHING SET-UP REQUIREMENTS: V_{EE} = -5.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_s	Set-up Time, $\overline{J}$ or $\overline{K}$ to Clock	1.0	0		ns	See Figure 4
t_h	Hold Time, $\overline{J}$ or $\overline{K}$ to Clock	1.0	0		ns	
t_w	Clock Pulse Width		2.0		ns	See Figure 1

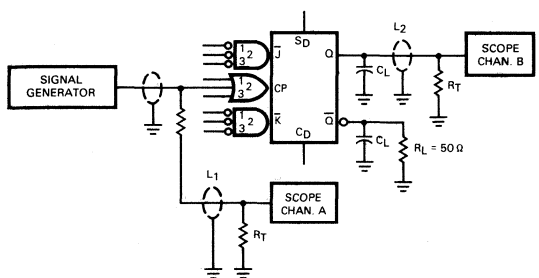
SWITCHING CIRCUITS AND WAVEFORMS

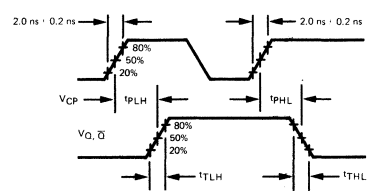




L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2}$ = 2.0 V
V_{EE} = -3.2 V

Fig. 1. Minimum Clock Frequency





L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2}$ = 2.0 V
V_{EE} = -3.2 V

Fig. 2. Clock Input to Output

SWITCHING CIRCUITS AND WAVEFORMS (Cont'd.)

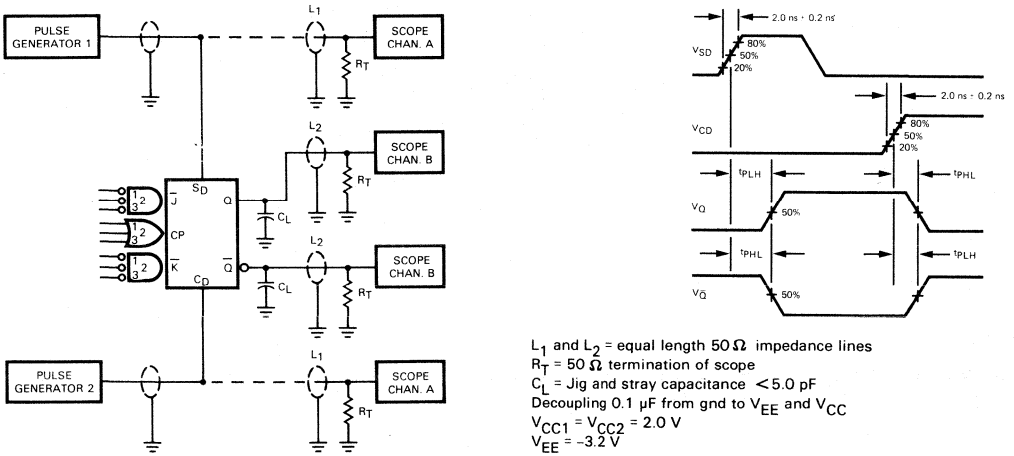


Fig. 3. Asynchronous Input to Output

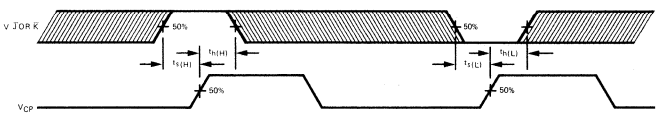
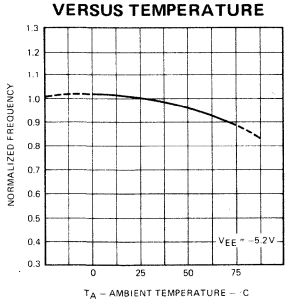


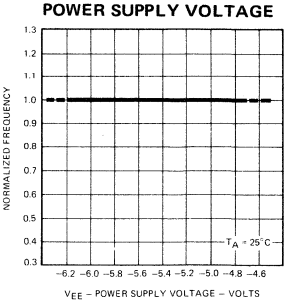
Fig. 4. Set-Up and Hold Time Waveforms

TYPICAL ELECTRICAL CHARACTERISTICS

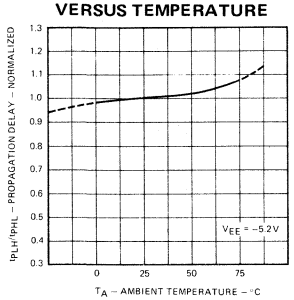
TOGGLE RATE VERSUS TEMPERATURE



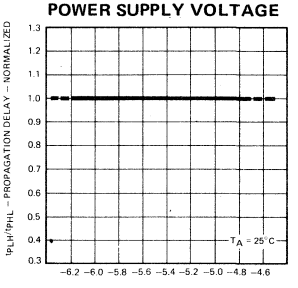
TOGGLE RATE VERSUS POWER SUPPLY VOLTAGE



PROPAGATION DELAY VERSUS TEMPERATURE



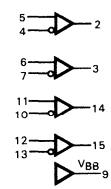
PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE



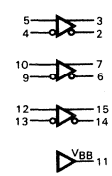
F95115 · F95116
LINE RECEIVERS

DESCRIPTION — The F95115 and F95116 are differential amplifiers with low impedance emitter-follower outputs. An internal reference supply (V_{BB}) is available for added versatility. Active current sources provide improved common mode rejection. The F95115 is a quad line receiver with single ended outputs. The F95116 is a triple line receiver with complementary outputs. The devices are voltage and temperature compensated and are fully compatible with other F95K devices. The line receivers are used primarily to receive data from balanced twisted pair lines, however, with appropriate connections and feedback, they may operate as Schmitt triggers, high speed comparators, oscillators or broadband amplifiers.

LOGIC DIAGRAM



F95115



F95116

TRUTH TABLES

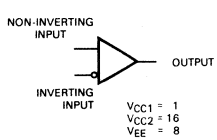
F95115 Quad Line Receiver

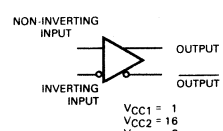
NON-INVERTING INPUT	INVERTING INPUT	OUTPUT
L	H	L
H	L	H
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	H	L
V_{BB}	L	H

F95116 Triple Differential Line Receiver

NON-INVERTING INPUT	INVERTING INPUT	OUTPUT	$\overline{\text{OUTPUT}}$
L	H	L	H
H	L	H	L
L	V_{BB}	L	H
H	V_{BB}	H	L
V_{BB}	H	L	H
V_{BB}	L	H	L

FUNCTIONS





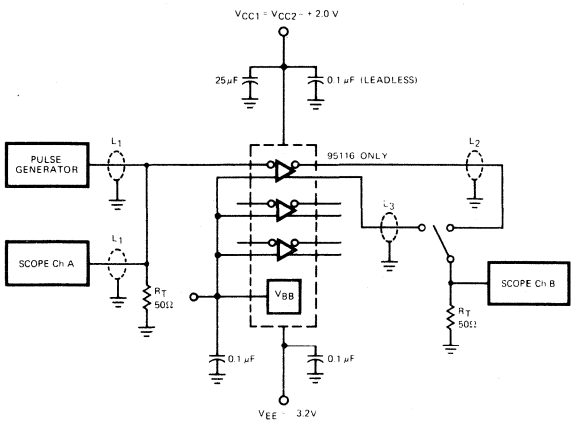
DC CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C

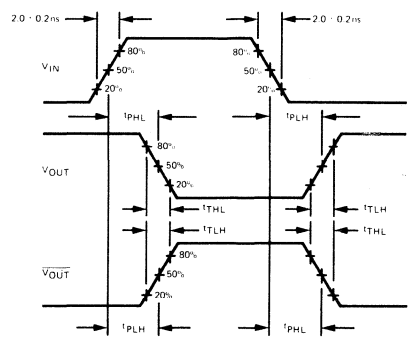
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	-1025	-965	-880	mV	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			95	µA	V_{IN} = V_{IHA}	
I_{CBO}	Input Collector-Base Leakage Current	-1.0			µA	V_{IN} = -5.2 V	
I_{EE}	Power Supply Current · F95115	-26	-18		mA	Pins 4,7,10,13 = V_{ILB} Pins 5,6,11,12 = V_{BB}	
	F95116	-21	-14		mA	Pins 4,9,12 = V_{ILB} Pins 5,10,13 = V_{BB}	
V_{BB}	Reference Voltage	-1380	-1320	-1260	mV	F95115,Connect Pins 5,6,11,12 to Pin 9 F95116,Connect Pins 5,10,13 to Pin 11	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay	1.0	2.0	3.1	ns	See Figure 1
t_{TLH}, t_{THL}	Output Transition Time 20% to 80%, 80% to 20%	1.5	2.0	3.5	ns	

SWITCHING CIRCUIT AND WAVEFORMS





Unused outputs connected to a 50Ω resistor to ground.

One input from each gate must be tied to V_{BB} during testing.

L_1, L_2, L_3 = equal length 50Ω impedance lines.

R_T = 50Ω termination of scope

Fig. 1

A line receiver is shown in *Figure 2*. The line is normally terminated in its characteristic impedance (typically 100 Ω) and output pull down resistors (typically 510 Ω) are used. The voltage across the terminating resistor V_T may be calculated as follows:

$$V_T = \frac{(V_{EE} - V_{OH})\, R_T}{R_E + R_T + R_{LINE}}$$

Where V_{OH} is the output voltage HIGH of the driving gate, R_{LINE} is the resistance and R_T is the terminating resistor. With typical values, V_T is 620 mV. The line receivers have a minimum differential input voltage gain of 7 V/V allowing very long twisted pairs to be driven. The line receivers employ active current sources which allow them to reject common mode inputs between -0.55 and -3 V.

Information transfer is often organized with a data bus approach, where many sources may input and receive data on a common bus as illustrated in *Figure 3*. This configuration is a special case of wired-OR and the line receiver inputs are essentially single ended which reduces worst case voltage gain to 3.5 V/V. In practice it is possible to transmit data at rates in excess of 100 MHz over bus lengths of 10 feet, having 10 or more receivers and transmitters on the line.

Twisted pair differential lines are recommended for clock distribution since clock skew may be balanced by adjusting line lengths. Propagation time is approximately 1 ns per eight inches of line.

TWISTED-PAIR CONNECTIONS

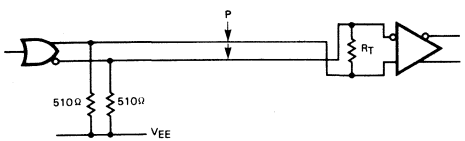


Fig. 2. Differential Transmission and Reception

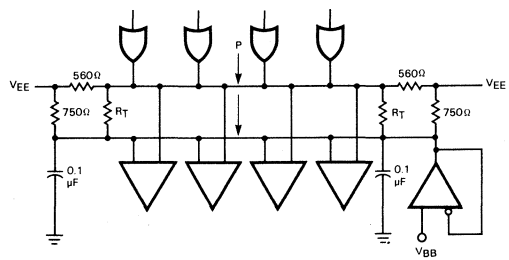


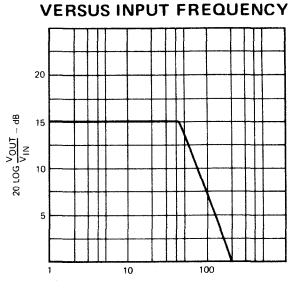
Fig. 3. Backplane Data Bus

CHARACTERISTICS FOR LINEAR APPLICATIONS

V_{EE} = -5.2 V, V_{CC} = GND, T_A = 25°C

CHARACTERISTIC	LIMITS			UNITS
	B	TYP	A	
Voltage Gain	3.5	5.0	6.0	V/V
Bandwidth		60		MHz
Input Resistance	4	6		kΩ
Input Capacitance		3		pF
Input Offset Current	0	2		μA
Input Bias Current		17	30	μA
Common Mode Input Voltage Range	-3.0		-0.55	V
Common Mode Rejection Ratio	50			dB
Supply Voltage Rejection Ratio		35		dB
Output Voltage Swing		0.40		Vpp
Output Source Current			50	mA
Output Resistance		9		Ω

TYPICAL LINE RECEIVER DIFFERENTIAL GAIN VERSUS INPUT FREQUENCY



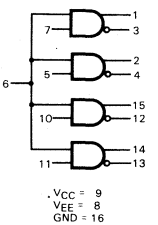
F95124

QUAD TTL TO ECL TRANSLATOR

DESCRIPTION — The F95124 is a Quad Translator for converting TTL logic levels to 95K ECL logic levels. The inputs are compatible with standard or with Schottky TTL. A Common Enable input (E_C), when LOW, holds all inverting outputs HIGH and holds all True outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator or as a differential line driver. The output levels are voltage and temperature compensated.

When the circuit is used in the differential mode, the F95124, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems.

LOGIC DIAGRAM



Logic Equations

$2 = \overline{5 \bullet 6}$

$4 = \overline{5 \bullet 6}$

DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = +5.0 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	-1025		-880	mV	V_{IN} = +4.0 V or +0.4 V per Logic Function	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810		-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	V_{IN} = V_{IHB} or V_{ILA} per Logic Function	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	1.8		5.0	V	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	0		1.0	V	Guaranteed Input Voltage LOW for All Inputs	
V_{CD}	Input Clamp Voltage	-1.5			V	I_{IN} = -10.0 mA	
V_{BD}	Input Breakdown Voltage	+5.5			V	I_{IN} = +1.0 mA, Other Inputs V_{IN} = GND	
I_{IH}	Input Current HIGH			50	µA	V_{IN} = +2.4 V, E_C V_{IN} = +0.4 V	
I_{IHX}	Input Current HIGH E_C			200	µA	E_C V_{IN} = +2.4 V, All Other Inputs V_{IN} = +0.4 V	
I_{IL}	Input Current LOW	-3.2			mA	V_{IN} = +0.4 V, E_C V_{IN} = +4.0 V	
I_{ILX}	Input Current LOW E_C	-12.8			mA	E_C V_{IN} = +0.4 V, All Other Inputs V_{IN} = +4.0 V	
I_{EE}	Power Supply Current	-34	-26		mA	Inputs and Outputs Open	
I_{CC}	Power Supply Current		+18	+25	mA	All Inputs, V_{IN} = GND	

8

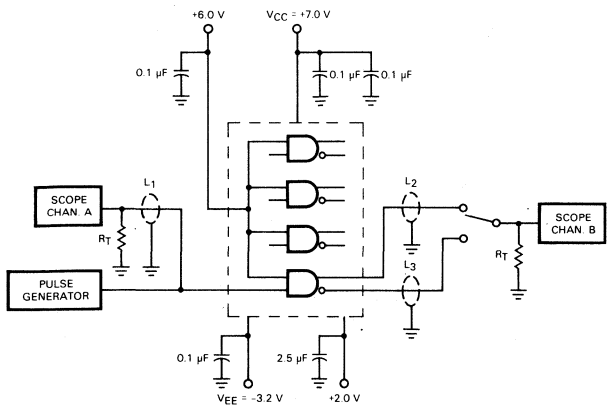
DC CHARACTERISTICS: V_{EE} = -4.7 to -6.2 V, V_{CC} = +4.75 to +5.25 V, T_A = 0°C to 75°C

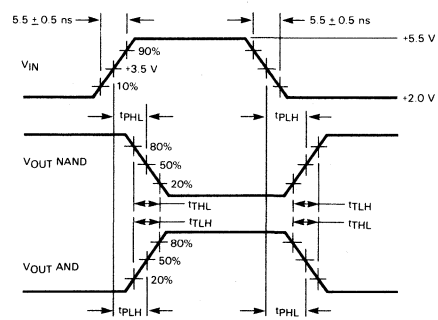
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS	
V_{OHC}	Output Voltage HIGH	-1050			mV	$V_{IN} = V_{IHB}$ or V_{ILA} per Logic Function	Loading is 50 Ω to -2.0 V
V_{OLC}	Output Voltage LOW			-1595	mV		
V_{IH}	Input Voltage HIGH	+2.0			V	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW			+0.85	V	Guaranteed Input Voltage LOW for All Inputs	
I_{EE}	Power Supply Current	-38	-29		mA	Inputs and Outputs Open, V_{EE} = -6.2 V	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = +5.0 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay, LOW to HIGH	1.0	3.0	6.0	ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW	1.0	3.0	6.0	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.5	3.9	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.5	3.9	ns	

SWITCHING CIRCUIT AND WAVEFORMS





NOTES:

Connect unused outputs through 50Ω resistor to ground.
L_1, L_2 and L_3 are equal lengths of 50Ω impedance lines.
R_T equals 50 Ω termination of scope

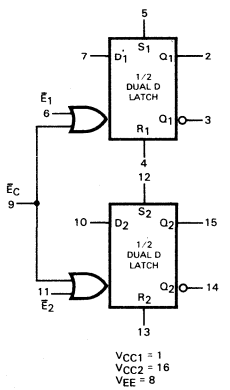
Fig. 1

F95130
DUAL D LATCH

DESCRIPTION — The F95130 contains a pair of D type latches with a Common Enable ($\overline{E}_C$) input. Each latch has its own Enable ($\overline{E}_n$), Set (S) and Reset (R) inputs. For each latch, the data present on the D input appears on the Q output when both $\overline{E}_n$ and $\overline{E}_C$ are LOW, as indicated in the truth table. As long as $\overline{E}_n$ and $\overline{E}_C$ remain LOW, the Q output follows the D input signal each time it changes. When either $\overline{E}_n$ or $\overline{E}_C$ (or both) go HIGH, the latch no longer responds to changes on the D input, but retains the last valid data present at D before $\overline{E}_n$ or $\overline{E}_C$ go HIGH. The two latches can be strobed individually by using the $\overline{E}_n$ inputs, or simultaneously by using the $\overline{E}_C$ input.

The Set and Reset inputs are effective only if $\overline{E}_n$ or $\overline{E}_C$ (or both) are HIGH. Note that in this mode of operation the output voltage levels of a latch are unpredictable if both the S and R signals are HIGH.

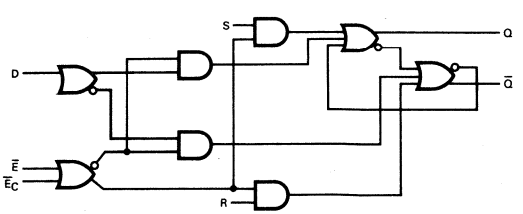
LOGIC SYMBOL



PIN NAMES

$\overline{E}_n$	Enable Inputs (Active LOW)
$\overline{E}_C$	Common Enable (Active LOW)
S_n	Set
R_n	Reset
D_n	Data Inputs
Q_n	Output
$\overline{Q}_n$	Output (Active LOW)

LOGIC DIAGRAM



(1/2 OF CIRCUIT SHOWN)

TRUTH TABLE

D	$\overline{E}_n$	$\overline{E}_C$	S	R	Q_{n+1}	OPERATION
L	L	L	X	X	L	D Function
H	L	L	X	X	H	D Function
X	H	X	L	L	Q_n	Memory
X	X	H	L	L	Q_n	Memory
X	H	X	H	L	H	Set
X	X	H	H	L	H	Set
X	H	X	L	H	L	Reset
X	X	H	L	H	L	Reset
X	H	X	H	H	-	Electrically Indeterminate
X	X	H	H	H	-	Electrically Indeterminate

L = LOW Voltage Level X = Don't Care

H = HIGH Voltage Level Q_n = Output

DC CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	-1025		-880	mV	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810		-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH S_n and R_n $\overline{E}_n$ D_n $\overline{E}_C$			 285 220 285 265	µA	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	-35	-25		mA	Inputs & Outputs Open	

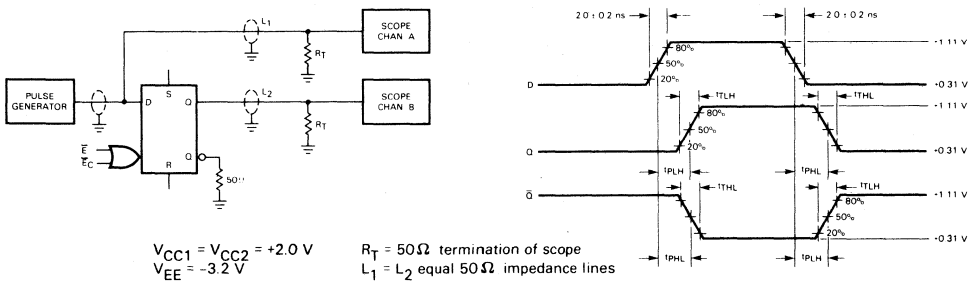
DC CHARACTERISTICS: V_{EE} = -4.7 to -6.2 V, T_A = 0°C to 75°C

V_{OHC}	Output Voltage HIGH	-1050			mV	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table Loading is 50 Ω to -2.0 V
V_{OLC}	Output Voltage LOW			-1595	mV	
V_{IH}	Input Voltage HIGH	-1155			mV	Guaranteed Input Voltage HIGH for All Inputs
V_{IL}	Input Voltage LOW			-1500	mV	Guaranteed Input Voltage LOW for All Inputs
I_{EE}	Power Supply Current	-38	-26		mA	Inputs & Outputs Open V_{EE} = -6.2 V

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL} t_{PLH}	Propagation Delay Data to Output	1.0	2.5	3.5	ns	See Figure 1
t_{PLH}	Propagation Delay Set to Output	1.0	2.7	3.5	ns	See Figure 2
t_{PHL}	Propagation Delay Clear to Output	1.0	2.7	3.5	ns	See Figure 3
t_{TLH}	Output Transition Time LOW to HIGH (20%–80%)	1.5	2.5	3.5	ns	See Figures 1, 2, and 3
t_{THL}	Output Transition Time HIGH to LOW (80%–20%)	1.5	2.5	3.5	ns	
t_s	Set-Up Time Data to Enable	2.5			ns	
t_h	Hold Time Data to Enable	1.5			ns	

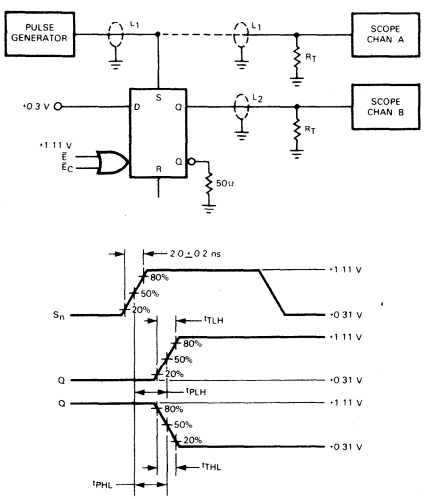
SWITCHING CIRCUITS AND WAVEFORMS



$V_{CC1} = V_{CC2}$ = +2.0 V
V_{EE} = -3.2 V

R_T = 50Ω termination of scope
$L_1 = L_2$ equal 50Ω impedance lines

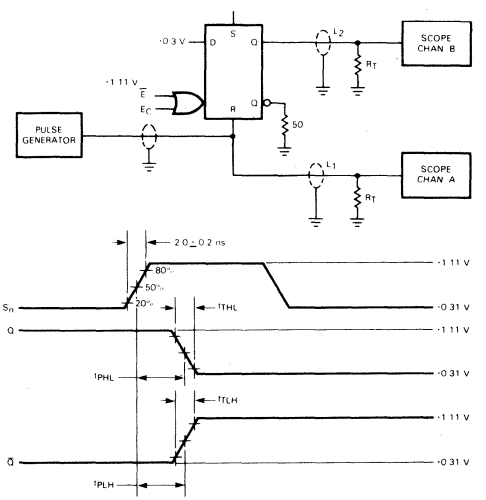
Fig. 1



$V_{CC1} = V_{CC2}$ = +2.0 V
V_{EE} = -3.2 V

R_T = 50Ω termination of scope
$L_1 = L_2$ equal 50Ω impedance lines

Fig. 2



$V_{CC1} = V_{CC2}$ = +2.0 V
V_{EE} = -3.2 V

R_T = 50Ω termination of scope
$L_1 = L_2$ equal 50Ω impedance lines

Fig. 3

F95231

HIGH SPEED DUAL D FLIP-FLOP

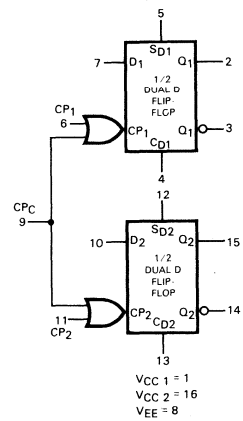
DESCRIPTION — The F95231 contains two master/slave D type flip-flops. The internal clock is the OR of two clock inputs, one common to both flip-flops The OR clock permits the use of one input as a clock pulse and the other as an active LOW enable. While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times.

Each flip-flop has separate set and clear inputs which asynchronously determine the state of the output independent of the clock levels. Note that the output voltage levels of a flip-flop are unpredictable if both set and clear signals are HIGH.

PIN NAMES

D	Data Input to Master
CP	Clock Input
CP_C	Common Clock Input
Q	Output
$\overline{Q}$	Complement Output
S_D	Set Direct Input
C_D	Clear Direct Input

LOGIC SYMBOL



SYNCHRONOUS OPERATION

D TABLE

D	$Q_{(t+1)}$
L	L
H	H
$S_D = C_D$ = LOW	

(t+1) = Time after positive going clock transition

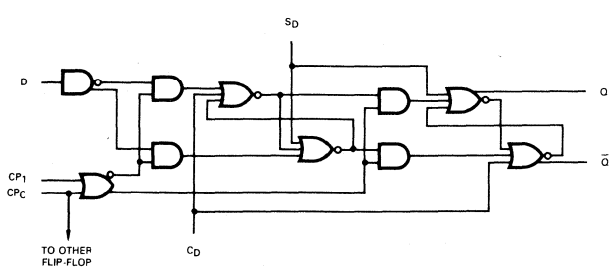
TRUTH TABLES

ASYNCHRONOUS OPERATION

S_D C_D TABLE

C_D	S_D	Q	$\overline{Q}$
L	L	See D Table	See D Table
L	H	H	L
H	L	L	H
H	H	undetermined	

LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays, as many gate functions are achieved internally without incurring a full gate delay.

DC CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1025	-965	-880	mV	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH C_{D1} and C_{D2} S_{D1} and S_{D2} CP_1 and CP_2 D_1 and D_2 CP_C			 330 330 220 245 265	µA	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			µA	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	-56	-45		mA	Inputs & Outputs Open	

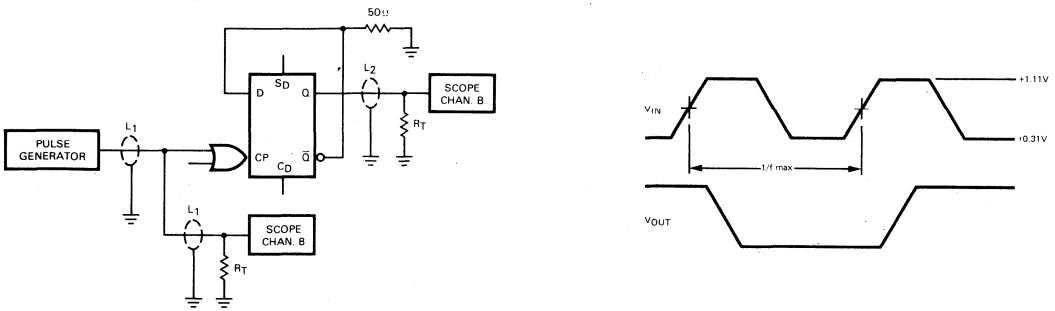
DC CHARACTERISTICS: V_{EE} = -4.7 to -6.2 V, T_A = 0°C to +75°C

V_{OHC}	Output Voltage HIGH	-1050			mV	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	Loading is 50Ω to -2.0 V
V_{OLC}	Output Voltage LOW			-1595	mV		
V_{IH}	Input Voltage HIGH	-1155			mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW			-1500	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{EE}	Power Supply Current		-47		mA	Inputs & Outputs Open V_{EE} = -6.2 V	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 75°C

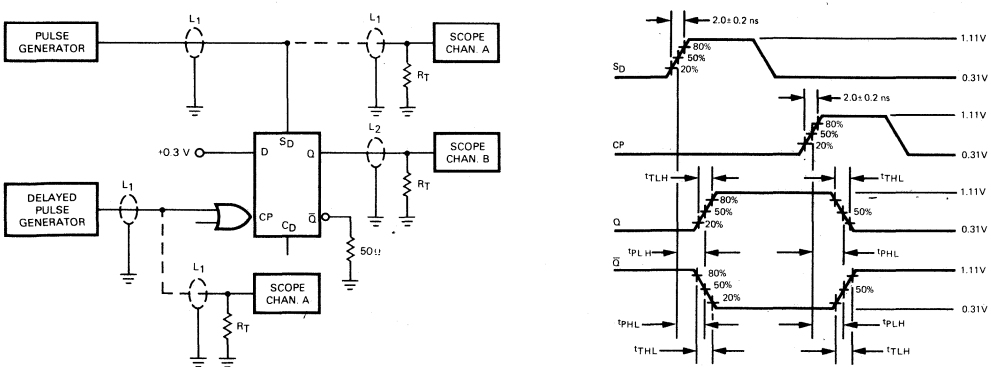
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
f_{count}	Toggle Frequency	200			MHz	See Figure 1
t_{PLH}	Propagation Delay Clock to Output	1.5	2.8	3.5	ns	See Figures 2 and 3
t_{PLH}, t_{PHL}	Propagation Delay Set to Q, Clear to Q	1.5	2.8	3.7	ns	
t_{TLH} t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.0	1.8	3.1	ns	
t_s	Set-up Time Data to Clock	1.5	0.5		ns	
t_h	Hold Time Data to Clock	0.75	-0.5		ns	

SWITCHING CIRCUITS AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

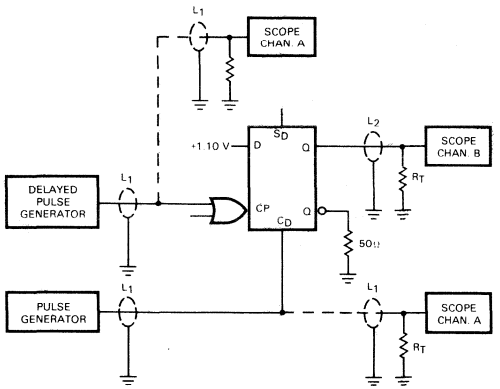
Fig. 1. Toggle Rate Test Circuit and Waveforms

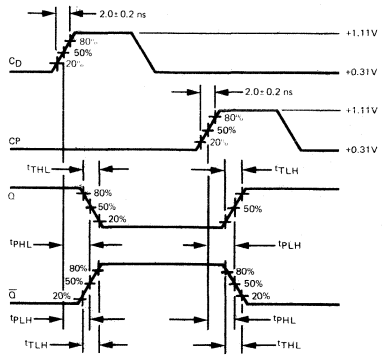


L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 2. Propagation Delay and S_D Test Circuit

SWITCHING CIRCUITS AND WAVEFORMS (Cont'd.)





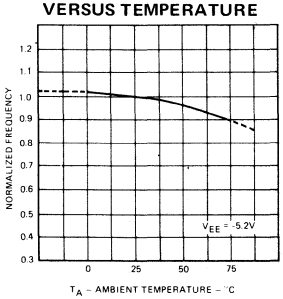
L_1 and L_2 = equal length 50Ω impedance lines
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C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 3. Propagation Delay and C_D Test Circuit

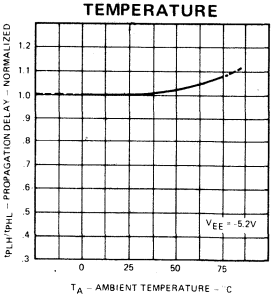
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TYPICAL ELECTRICAL CHARACTERISTICS

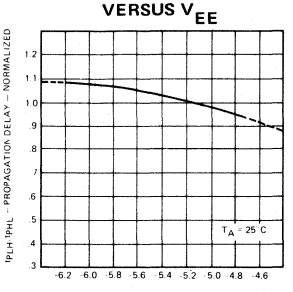
TOGGLE RATE VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS V_{EE}



INTRODUCTION

1 ECL FOR HIGH PERFORMANCE SYSTEMS

2 ECL CIRCUIT BASICS

3 ECL LOGIC DESIGN

4 TRANSMISSION LINE CONCEPTS

5 ECL INTERCONNECTIONS

6 POWER DISTRIBUTION AND THERMAL CONSIDERATIONS

7 F10K SERIES DATA SHEETS

8 F95K SERIES DATA SHEETS

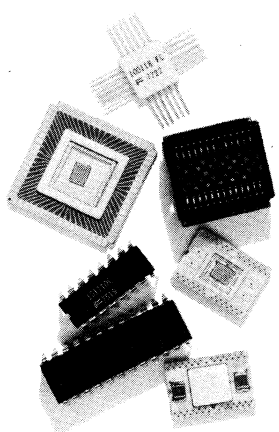
9 11C SERIES DATA SHEETS

10 F100K SERIES DATA SHEETS

11 ECL MEMORY DATA SHEETS

12 ORDER AND PACKAGE INFORMATION

13 FAIRCHILD FIELD SALES OFFICES, REPRESENTATIVES AND DISTRIBUTORS



11C01

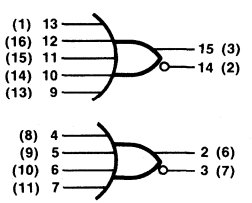
DUAL 5-4 INPUT OR/NOR GATE

11C00 SERIES

DESCRIPTION — The 11C01 is a voltage compensated ECL dual 5-4 input OR/NOR gate using the Isoplanar II process. The circuit has standard internal voltage compensation with dc parameters identical to F10K ECL devices.

- **VERY HIGH SPEED. . .TYPICALLY 700 ps PER GATE**
- **VOLTAGE COMPENSATED**
- **OPEN EMITTER FOLLOWER OUTPUTS**
- **COMPLEMENTARY, SIMULTANEOUS OUTPUTS**
- **SEPARATE V_{CC} PINS**
- **WIRED-OR CAPABILITY**
- **FABRICATED USING ISOPLANAR II TECHNOLOGY**

LOGIC DIAGRAM



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
( ) = Flatpak

TRUTH TABLE

	INPUTS									OUTPUTS			
DIP	4	5	6	7	13	9	12	11	10	2	3	15	14
FLT	8	9	10	11	1	13	14	15	16	6	7	3	2
	L	L	L	L	L	L	L	L	L	L	H	L	H
	H	X	X	X	H	X	X	X	X	H	L	H	L
	X	H	X	X	X	H	X	X	X	H	L	H	L
	X	X	H	X	X	X	H	X	X	H	L	H	L
	X	X	X	H	X	X	X	H	X	H	L	H	L
	—	—	—	—	X	X	X	X	H	—	—	H	L

X = Don't Care

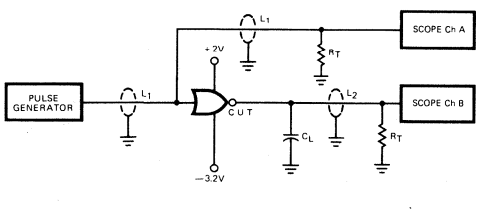
DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	V_{IN} = V_{IHB} or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			350	µA	25°C	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			µA	25°C	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	-30	-24		mA	25°C	Inputs and Outputs Open	

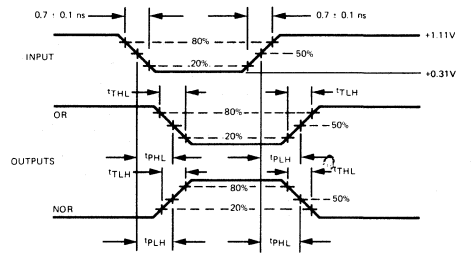
AC CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS (Flatpak) B	LIMITS (Flatpak) TYP	LIMITS (Flatpak) A	LIMITS (DIP) B	LIMITS (DIP) TYP	LIMITS (DIP) A	UNITS	CONDITIONS
t_{PLH}	Propagation Delay, LOW to HIGH	0.45	0.7	0.95	0.60	0.90	1.15	ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW	0.45	0.7	0.95	0.60	0.90	1.15	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)		0.7	0.95		0.90	1.15	ns	
t_{PHL}	Output Transition Time HIGH to LOW (80% to 20%)		0.7	0.95		0.90	1.15	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance line
R_T = 50 Ω Termination of scope
Decoupling 0.1 µF from GND to V_{EE} and V_{CC}



Jig set-up with no circuit under test
V_{CC} = V_{CC} (AUX) = +2.0 V
V_{EE} = -3.2 V

Fig. 1

11C05

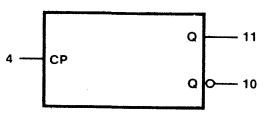
1 GHz DIVIDE-BY-FOUR COUNTER

11C00 SERIES

DESCRIPTION — The 11C05 is an ECL Divide-by-Four Counter with a maximum operating frequency above 1 GHz over the 0°C to +75°C temperature range. The input may be dc or ac (capacitively) coupled to the signal source. The emitter follower outputs (Q and $\overline{Q}$) are capable of driving 50 Ω lines. The outputs are voltage compensated and provide standard ECL output levels.

- **DC TO 1 GHz OPERATION, GUARANTEED OVER 0°C TO +75°C**
- **AC OR DC COUPLED INPUT**
- **VOLTAGE COMPENSATED**
- **USES STANDARD TTL OR ECL POWER SUPPLY VOLTAGE**
- **TRUE AND COMPLEMENT OUTPUTS**
- **50 Ω DRIVE CAPABILITY**
- **FABRICATED USING ISOPLANAR II TECHNOLOGY**

LOGIC SYMBOL

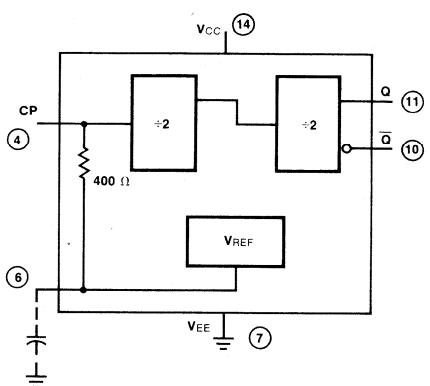


V_{CC} = Pin 14
V_{EE} = Pin 7
Bias Filter = Pin 6

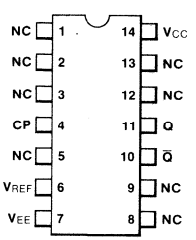
FUNCTIONS

CP	Clock Input
$\overline{Q}$, Q	Counter Outputs

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



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COMMERCIAL RANGE DC CHARACTERISTICS: V_{EE} = -5.0 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
V_{OH}	Output Voltage HIGH	-1060 -1025 -980	-995 -960 -910	-910 -880 -830	mV	0°C 25°C 75°C	V_{IN} = V_{IH} or V_{IL}, Loading 50Ω to -2 V
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV	0°C to 75°C	
V_{IH}	Input Voltage HIGH	-2.45 -2.50 -2.60			V	0°C 25°C 75°C	Guaranteed Input HIGH
V_{IL}	Input Voltage LOW			-3.25 -3.30 -3.40	V	0°C 25°C 75°C	Guaranteed Input LOW
I_{EE}	Power Supply Current	-90	-65		mA	25°C	Input Open
V_{EE}	Supply Voltage Range	-5.25	-5.0	-4.75	V	0°C to 75°C	

MILITARY RANGE DC CHARACTERISTICS: V_{EE} = -5.0 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
V_{OH}	Output Voltage HIGH	-1100 -980 -910	-1030 -910 -820	-950 -820 -720	mV	-55°C 25°C +125°C	V_{IN} = V_{IH} or V_{IL}, Loading 100Ω to -2 V
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV	-55° to 125°C	
V_{IH}	Input Voltage HIGH	-2.35 -2.50 -2.70			V	-55°C 25°C +125°C	Guaranteed Input HIGH
V_{IL}	Input Voltage LOW			-3.15 -3.30 -3.50	V	-55°C 25°C +125°C	Guaranteed Input LOW
I_{EE}	Power Supply Current	-90	-65		mA	25°C	Input Open
V_{EE}	Supply Voltage Range	-5.5	-5.0	-4.75	V	-55°C to 125°C	

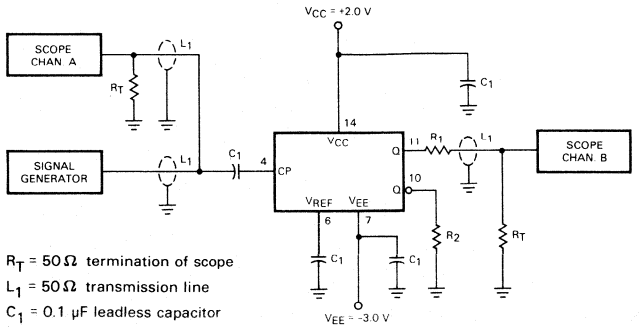
COMMERCIAL AND MILITARY RANGE
AC CHARACTERISTICS: V_{EE} = -5 V, V_{CC} = GND, T_A = -55°C to 125°C unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS	
f_{COUNT}	Maximum Sinusoidal Input Frequency	1000			MHz	0°C to +75°C	AC Coupled, 800 mV pk-pk Input See Note 2
		950				-55°C to +125°C	
f_{COUNT}	Minimum Sinusoidal Input Frequency		25		MHz		
SR_{MIN}	Slew Rate of Squarewave		50		V/μs	See Note 1	

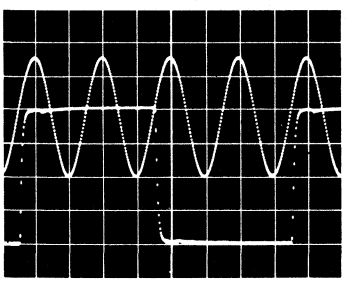
NOTES:

1. Very low frequency operation is possible as long as sufficient slew rate of the input pulse edges is maintained.
2. Input drive shall not exceed 1.5 $V_{pk\text{-}pk}$ max.

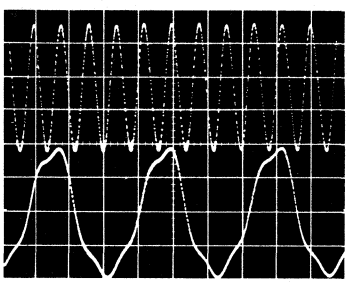
TEST CIRCUIT AND WAVEFORMS



R_T = 50 Ω termination of scope
L_1 = 50 Ω transmission line
C_1 = 0.1 μF leadless capacitor
R_1 = 0 Ω for commercial grade, 50 Ω for military grade
R_2 = 50 Ω for commercial grade, 100 Ω for military grade



25 MHz Operation
Horizontal Scale = 20 ns/div
Vertical Scale = 200 mV/div

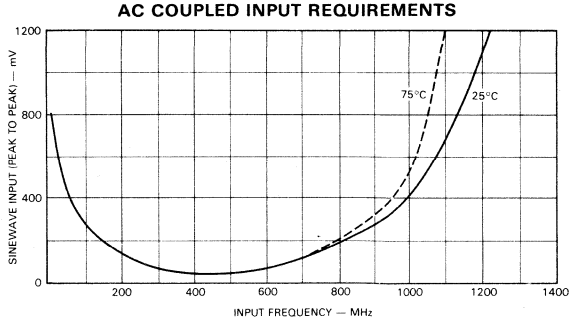


1.2 GHz Operation
Horizontal Scale = 1 ns/div
Vertical Scale = 200 mV/div

TRIGGERING REQUIREMENTS — A dc coupled input should be designed to provide specified V_{IH} and V_{IL} levels. For ac coupling, an external resistor may or may not be necessary depending on the application. If an input signal is always present, only the capacitor is required because an internal 400 Ω resistor connected between CP and V_{REF} centers the ac signal about mid-threshold. For applications in which an input signal is not always present, ac coupling requires that an external 10 k Ω resistor be connected between CP and V_{EE}. This offsets the input sufficiently to avoid extreme sensitivity to noise when no signal is present. Otherwise, noise triggering can lead to oscillation at about 450 MHz. For best operation, both outputs should be equally loaded.

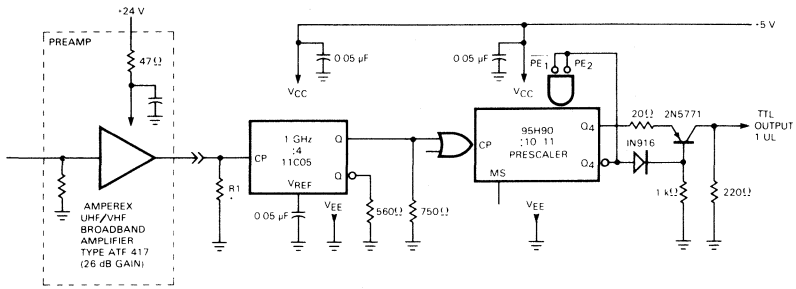
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AC COUPLED INPUT REQUIREMENTS



NOTE: Trigger amplitudes refer to the circuit end of the input cable as opposed to the signal generator end.

APPLICATIONS



* R1 = 10 kΩ only required to desensitize 11C05 input under no-signal conditions.

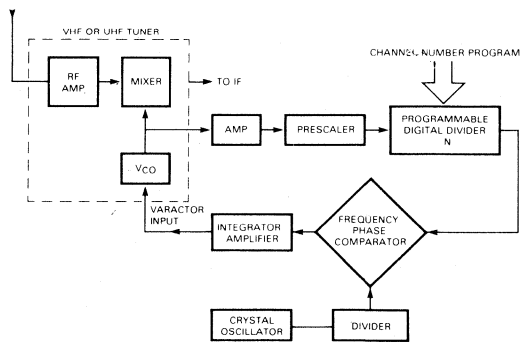
1 Amperex broadband amplifier specified at 26 dB with 75Ω input and output terminations. Note inputs and outputs are internally capacitive coupled therefore no capacitors required between AFF 417 and 11C05.

2 All decoupling capacitors either monolithic ceramic or ceramic leadless capacitors.

1 GHz ÷ 40 Prescaler

The dotted block represents a standard VHF or UHF varactor tuner. An amplifier is connected to the V_{CO} output of the tuner to increase the voltage to acceptable levels for driving a digital ECL prescaler (divider).

The purpose of the prescaler is to divide down the local oscillator high frequencies to a range that can be processed and counted by standard TTL logic. Output of the prescaler is then fed to the programmable divider which is the heart of the system. Its output is passed along to a frequency/phase comparator and is compared to a crystal controlled reference frequency. Then the comparator output is fed to an integrator/amplifier, which in turn provides voltage control to the varactor tuner input. The divide ratio of the programmable counter determines the channel desired.



Frequency Synthesizer for UHF, VHF, TV, Radio Communications.

11C06

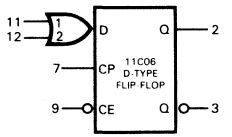
750 MHz D-TYPE FLIP-FLOP

11C00 SERIES

GENERAL DESCRIPTION — The F11C06 is a high speed ECL D-type Master-Slave Flip-Flop capable of toggle rates over 750 MHz. Designed primarily for high speed prescaling, it can also be used in any application which does not require preset inputs. The circuit is voltage compensated, which makes input thresholds and output levels insensitive to V_{EE} variations. Complementary Q and $\overline{Q}$ outputs are provided, as are two Data inputs, Clock and Clock Enable inputs. The 11C06 is pin compatible with the Motorola MC1690L but is a higher frequency replacement.

- **TOGGLE FREQUENCY = 750 MHz TYP AT 25°C**
- **WIRED-OR CAPABILITY**
- **COMPLEMENTARY SIMULTANEOUS OUTPUTS**
- **OPEN EMITTER FOLLOWER OUTPUTS**
- **SEPARATE V_{CC} PINS ELIMINATE NOISE COUPLING**
- **INTERNAL 50 kΩ NOMINAL INPUT PULL-DOWN RESISTORS**
- **VOLTAGE COMPENSATED**

LOGIC SYMBOL



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

PIN NAMES

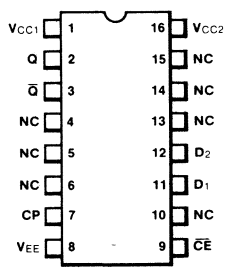
D_n	Data Input
CP	Clock Input
$\overline{CE}$	Clock Enable (Active LOW)
Q	Output
$\overline{Q}$	Complementary Output

TRUTH TABLE

$\overline{CE}$	CP	D	Q_{n+1}
L	L	X	Q_n
L	H	X	Q_n
L	⎍	L	L
L	⎍	H	H
H	X	X	Q_n

X = Don't Care

CONNECTION DIAGRAM
DIP (TOP VIEW)



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FUNCTIONAL DESCRIPTION — While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times.

The CP and $\overline{CE}$ inputs are logically identical, but physical constraints associated with the dual in-line package make the $\overline{CE}$ input slower at the upper end of the toggle range. To prevent new data from entering the master on the next CP LOW cycle, $\overline{CE}$ should go HIGH while CP is still HIGH.

DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table Loading 50Ω to -2 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1635 -1620 -1595	mV	0°C 25°C 75°C	
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	$V_{IN} = V_{IHB}$ or V_{ILA} for D_n Inputs Loading 50Ω to -2 V
V_{OLC}	Output Voltage LOW			-1615 -1600 -1575	mV	0°C 25°C 75°C	
V_{IH}	Input Voltage HIGH	-1135 -1095 -1035		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1500 -1485 -1460	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs
I_{IH}	Input Current HIGH Clock Input Data Input			 250 270	μA	25°C	$V_{IN} = V_{IHA}$
I_{IL}	Input Current LOW	0.5			μA	25°C	$V_{IN} = V_{IHB}$
I_{EE}	Power Supply Current	-59	-40		mA	25°C	All Inputs Open

AC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC} = GND, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay (CP-Q) Propagation Delay (CP-Q)	0.7 0.7	1.0 1.0	1.2 1.2	ns ns	
t_{TLH} t_{THL}	Transition Time 20%-80% Transition Time 80%-20%	0.5 0.5	0.8 0.8	1.0 1.0	ns ns	See Figure 1
$f_{TOG\ (MAX)}$	Toggle Frequency (CP)	650	750		MHz	See Figure 2, Note
t_s t_h	Set-up Time Hold Time		0.2 0.2		ns	

NOTE:
The device is guaranteed for f_{TOG} (CP) ≥ 600 MHz, f_{TOG} ($\overline{CE}$) ≥ 550 MHz over the 0°C to +75°C temperature range.

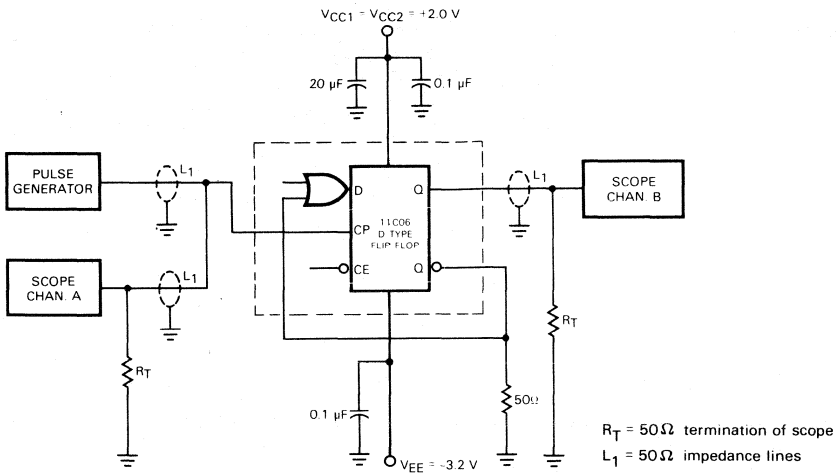


Fig. 1. Propagation Delay (CP-Q)

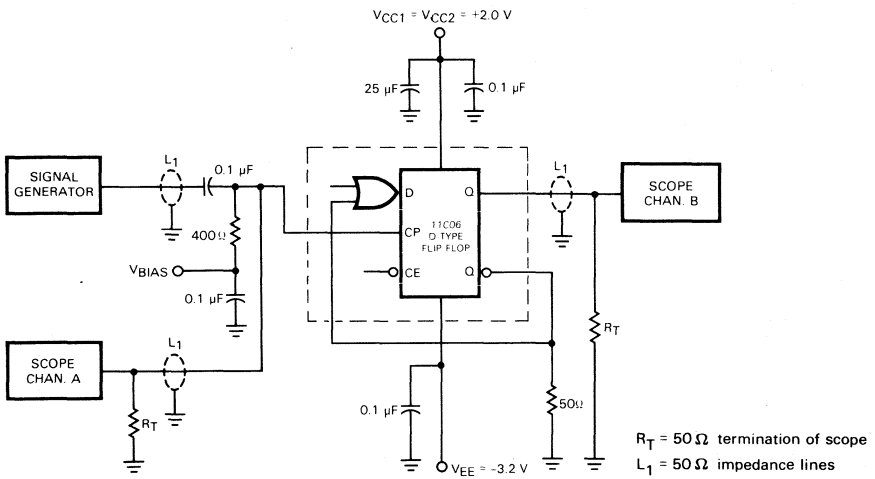
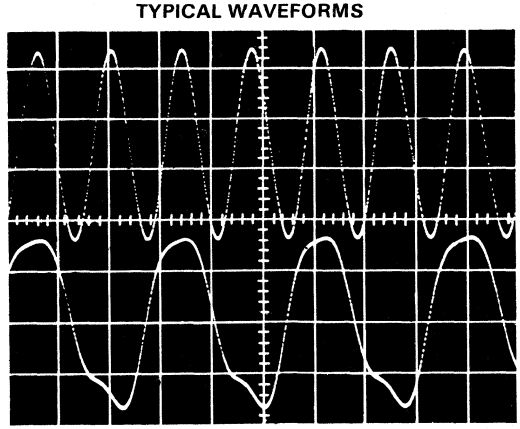


Fig. 2. Toggle Frequency Test Circuit

TYPICAL WAVEFORMS



HORIZONTAL SCALE = 1.0 ns/div
VERTICAL SCALE = 200 mV/div

700 MHz Operation

11C24

DUAL VOLTAGE CONTROLLED MULTIVIBRATOR

11C00 SERIES

GENERAL DESCRIPTION — The 11C24 contains two astable multivibrators with totem pole TTL outputs. Each circuit operates independently, with its frequency determined by an applied voltage V_{IN} in conjunction with an external timing capacitor C_X. Operating frequency ranges from typically 30 MHz with 10 pF C_X to low frequencies determined only by practical limits on capacitor size. Input control voltage variation from 1.0 V to 5.0 V causes a frequency change of typically 4.5 to 1.

Each circuit consists of a current mode multivibrator driving a TTL buffer. Each multivibrator has its own power and ground pins to minimize crosstalk, while the buffers have common power and ground pins. Each output will drive 12 standard TTL loads.

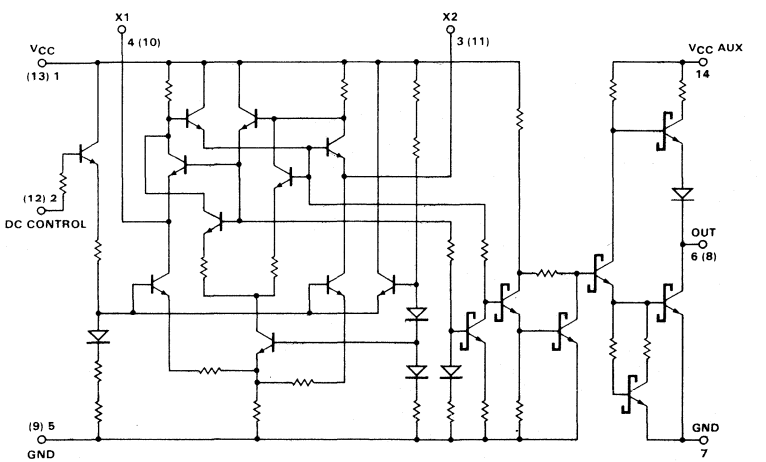
The device is designed primarily for phase locked loop applications, performing the analog-to-frequency conversion. By appropriate choice of timing capacitors, the two circuits in one package can provide a 10 to 1 tuning range. It can also be used for fixed-frequency applications and can be operated with a crystal in place of C_X.

- **BROAD FREQUENCY RANGE — DC TO 30 MHz**
- **BROAD TUNING RATIO — TYPICALLY 4.5 TO 1**
- **TTL TOTEM POLE OUTPUTS**
- **DECADE TUNING RANGE PER PACKAGE**

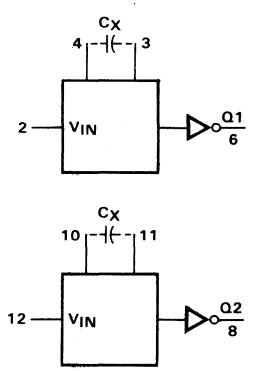
FUNCTIONS

V_{IN}	Applied Control Voltage
C_X	External Timing Capacitor
Q_1, Q_2	Outputs

SCHEMATIC DIAGRAM

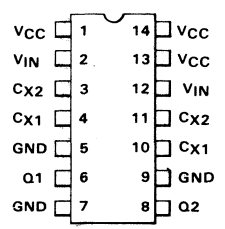


LOGIC SYMBOL



VCC: VCM = Pins 1, 13
Output Buffers = Pin 14
GND: VCM = Pins 5, 9
Output Buffers = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION — Each half of the 11C24 contains a current mode multivibrator, an ECL-to-TTL translator and a TTL output buffer. The external timing capacitor connects between the collectors of a pair of transistors operating as current sources. These two current sources determine the rate at which C_X is alternately charged in opposite directions during a complete cycle. The voltage swing at the C_X terminals is controlled by an ECL latch.

The external control voltage V_{IN} can change the two source currents by a factor of typically 4.5 to 1. When V_{IN} is changed, a third internal current source is automatically changed in a compensating manner to maintain constant total current through the ECL latch. This, in turn, maintains constant voltage swing at the C_X terminals despite the changes in charging current. A detailed description of the dynamic operation is given in the data sheet for the 11C58 VCM, which is the high frequency version with ECL outputs.

The ECL-to-TTL translator circuit receives complementary drive from the ECL latch, converts it to single-ended signal, and provides sufficient gain to drive the TTL buffer. Schottky-clamped transistors are used in the translator and buffer to balance transition times and improve the output waveform at high frequencies.

Each multivibrator has its own power and ground pins to prevent on-chip crosstalk, either between multivibrators or from an output buffer to a multivibrator. Outside the package, the V_{CC} pins are normally connected to the same bus, as are the ground pins. It is advisable to use an rf bypass capacitor between power and ground, as close to the package as possible. Excessive common coupling in the power or ground distribution can cause one circuit to have a pulling effect on the other.

During multivibrator operation, the voltage across C_X alternates from a peak of approximately 0.8 V of one polarity to 0.8 V of the opposite polarity. The capacitor chosen for C_X should thus be capable of withstanding 1V in either direction; for waveform symmetry, its capacitance-versus-voltage characteristic should be linear over this range.

Figure 1 shows the relationship between frequency and timing capacitance for several values of control voltage. At very low values of C_X, stray capacitance has a noticeable effect on the shape of the curves. For C_X of 100 pF or more, however, frequency is inversely proportional to C_X for a given value of V_{IN}. This reciprocal relationship allows the product $f_O \times C_X$ to be plotted as a function of V_{IN}, as shown in *Figure 2*. This curve shows that the most effective range for V_{IN} is 3 to 5 V. For V_{IN} less than about 3 V, an internal clamp circuit comes into play and maintains the minimum voltage to the current source transistors required to insure proper operation. The clamp circuit also acts as the controlling element when the V_{IN} terminal is unused, *i.e.*, left open. As a recommended upper limit, V_{IN} should not exceed the V_{CC} supply by more than about 0.5 V; otherwise, the input resistor will become forward biased and tend to clamp the input, making circuit response less predictable.

Figures 3 and *4* show the typical frequency deviation as a function of supply voltage and ambient temperature. The temperature curves apply for the 11C24 only, excluding effects of temperature on the timing capacitor. Frequency deviations with supply voltage and temperature are effectively nullified either when a crystal is used in place of C_X for fixed frequency applications, or when a phase locked loop is used for variable frequency applications. *Figure 5* shows a phase locked loop in block diagram form. If the VCM frequency starts to drift, the variable frequency into the 11C44 phase/frequency detector also changes. The 11C44 detects the discrepancy between the reference and variable inputs and generates an error signal. After filtering and amplification, the error signal is applied to the VCM control input and changes f_O until the two signals into the 11C44 again agree in phase and frequency.

TYPICAL OUTPUT FREQUENCY VERSUS TIMING CAPACITANCE FOR VARIOUS INPUT VOLTAGES

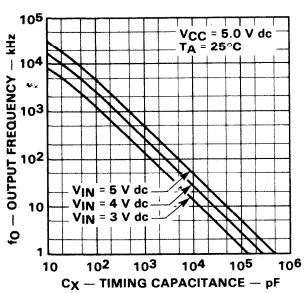


Figure 1

TYPICAL FREQUENCY-CAPACITANCE PRODUCT VERSUS CONTROL VOLTAGE

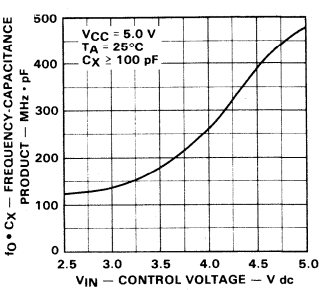


Figure 2

TYPICAL FREQUENCY DEVIATION VERSUS SUPPLY VOLTAGE

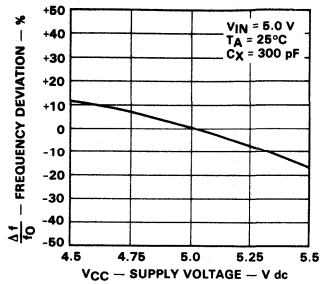


Figure 3

TYPICAL FREQUENCY DEVIATION VERSUS AMBIENT TEMPERATURE FOR VARIOUS INPUT VOLTAGES

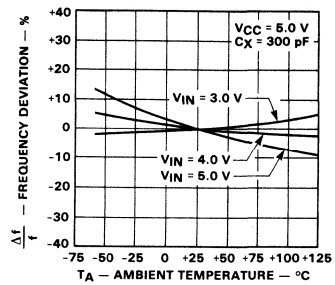


Figure 4

PHASE LOCKED LOOP

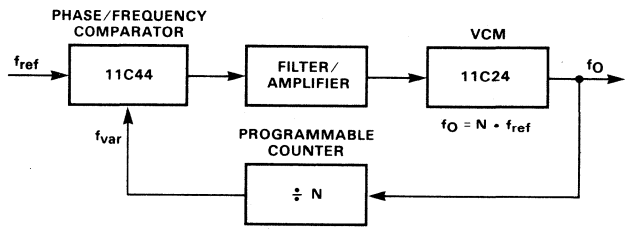


Figure 5

RECOMMENDED OPERATING CONDITIONS

PART TYPE		SUPPLY VOLTAGE V dc		AMBIENT TEMP °C	
		MIN	MAX	MIN	MAX
11C24DC	Commercial	4.75	5.25	0	+75
11C24DM	Military	4.5	5.5	-55	+125

DC CHARACTERISTICS: Over operating temperature range unless otherwise noted.

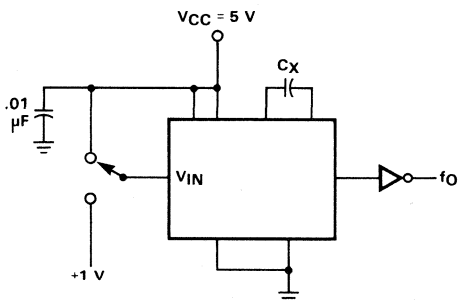
SYMBOL	CHARACTERISTIC	PIN(s)	LIMITS Note 1 B	LIMITS Note 1 A	UNITS	CONDITIONS		V_{CC} Note 2
V_{OH}	Output Voltage HIGH	6	2.4		V	11C24DM	Pins 1, 4, 13, 14 = V_{CC}	Min
		6	2.5		V	11C24DC	I_{OH} = -1.6 mA	
		8	2.4		V	11C24DM	Pins 10,13,14 = V_{CC}	Min
		8	2.5		V	11C24DC	I_{OH} = -1.6 mA	
V_{OL}	Output Voltage LOW	6		0.5	V	Pins 1, 3, 13, 14 = V_{CC} I_{OL} = 9.8 mA		Min
		8		0.5	V	Pins 11, 13, 14 = V_{CC} I_{OL} = 9.8 mA		Min
I_{IN}	Input Current	2,12		40	µA	V_{IN} = 5.0 V; Pins 1,13,14 = V_{CC}		Max
I_{CC}	Power Supply Current	1,13,14		37	mA	T_A = 25°C; Pins 2,4,10,12 = 5 V; Pins 1,3,14 = V_{CC}		5.0 V
I_{SC}	Short-Circuit Output Current	6	-65	-20	mA	Pins 1, 4, 13, 14 = V_{CC}	V_{OUT} = 0 V	5.0 V
		8	-65	-20	mA	Pins 10, 13, 14 = V_{CC}		

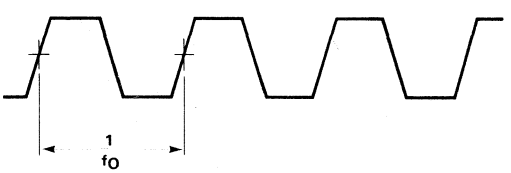
NOTES:
1. B is the most negative limit; A is the most positive limit.
2. Min and Max refer to the recommended V_{CC} values for the particular device type. Pins 5, 7, 9 grounded for all tests.

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS		UNITS	CONDITIONS	
		B	TYP			
f_{MAX}	Maximum Oscillation Frequency	25	30	MHz	C_X = 10 pF, V_{IN} = 5.0 V	
TR	Tuning Ratio Test	3.5	4.5		$\frac{f_O \text{ @ } V_{IN} = +5 \text{ V}}{f_O \text{ @ } V_{IN} = +1 \text{ V}}$	C_X = 100 pF

SWITCHING CIRCUIT AND WAVEFORM





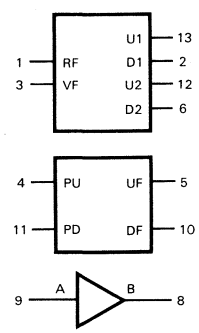
11C44

PHASE/FREQUENCY DETECTOR

11C00 SERIES

GENERAL DESCRIPTION — The 11C44 contains a Phase/Frequency Detector, a Phase Dectector, a Charge Pump, and an Amplifier. The Phase/Frequency Detector accepts TTL signals representing a Reference Frequency (RF) and a Variable Frequency (VF), compares the relative timing of their negative going transitions, and generates either and UP (U1) or a DOWN (D1) signal whose duration is equal to the RF-VF timing difference. When the RF and VF signals have the same frequency, the Phase Detector outputs U2 and D2 provide binary signals whose duty cycles are proportional to the phase angle between RF and VF. The Charge Pump can be driven from U1 and D1 or U2 and D2, and has three possible output states representing CHARGE, DISCHARGE, and HOLD instructions when applied to an integrator. The Amplifier is a Darlington transistor with grounded emitter and uncommitted collector and base. The 11C44 thus contains several of the functional elements used in phase-locked loop applications. It is pin compatible with the Motorola MC4044/4344, but has better discrimination capability for small phase differences.

LOGIC SYMBOL

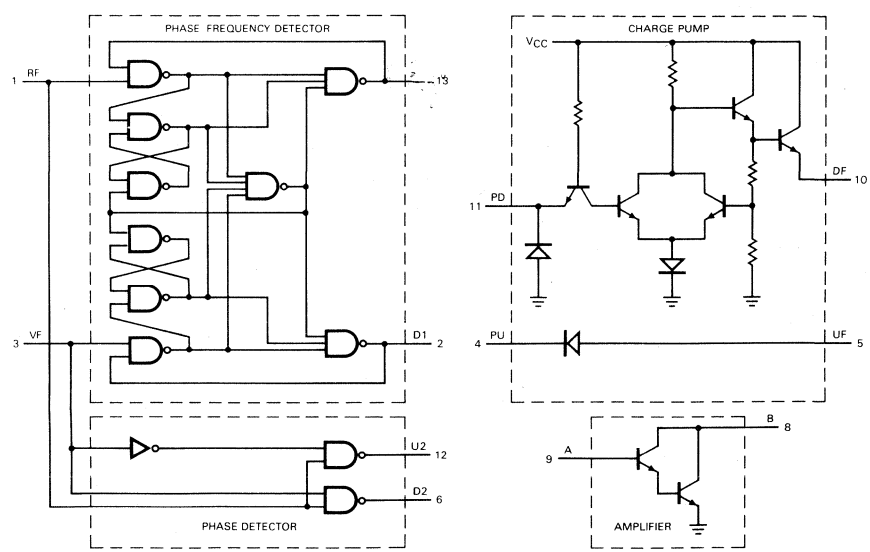


V_{CC} = Pin 14
GND = Pin 7

FUNCTIONS

RF — Reference Frequency Input
VF — Variable Frequency Input
U1, D1 — Phase/Frequency Detector Outputs
U2, D2 — Phase Detector Outputs
PU, PD — Charge Pump Inputs
UF, DF — Charge Pump Outputs
A — Amplifier Input
B — Amplifier Output

LOGIC DIAGRAM AND SCHEMATIC



RECOMMENDED OPERATING CONDITIONS

PART NUMBER	SUPPLY VOLTAGE V_{dc}		AMBIENT TEMPERATURE °C	
	MIN	MAX	MIN	MAX
11C44DC — Commercial	4.75	5.25	0	+75
11C44DM — Military	4.5	5.5	-55	+125

DC CHARACTERISTICS: (over operating temperature range unless otherwise noted)

SYMBOL	CHARACTERISTIC	PIN(s)	LIMITS B	LIMITS A	UNITS	CONDITIONS		V_{CC1}
V_{IH}	Input HIGH Voltage	1, 3, 11	2.0		V	Per Truth Tables		MIN
V_{IL}	Input LOW Voltage	1, 3, 11		0.9	V	Per Truth Tables		MIN
V_{OH2}	Output HIGH Voltage	2, 6, 12, 13	2.4		V	11C44DM	I_{OH} = -1.6 mA	MIN
			2.5		V	11C44DC		
V_{OL2}	Output LOW Voltage	2, 6, 12, 13		0.5	V	I_{OL} = 20 mA		MIN
V_{CD}	Clamp Diode Voltage	1, 3, 11	-1.5		V	I_{IN} = -10 mA; T_A = 25°C only		MIN
I_{IL}	Input LOW Current	1, 3	-4.8		mA	V_{IN} = 0.4 V		MAX
		11	-1.6					
I_{IH}	Input HIGH Current	1, 3		120	µA	V_{IN} = V_{OH} MIN		MAX
		11		40				
		1, 3, 11		1.0	mA	V_{IN} = 5.5 V; T_A = 25°C only		MAX
I_{CEX2}	Output Leakage Current	2, 6, 12, 13		250	µA	V_{OUT} = 5.0 V		5.0 V
I_{SC2}	Short-circuit Output Current	2, 6, 12, 13	-65	-20	mA	V_{OUT} = 0 V		5.0 V
V_{EH}	Output HIGH Voltage	10	1.5		V	I_{OH} = -1 mA; Pin 11 = V_{IL}		MIN
I_{ER}	Output Leakage Current	10		5.0	µA	Pin 10 = 1.5 V; Pin 11 = V_{OH} MIN		MAX
I_C	Amplifier Output Current	8	1.0		mA	T_A = MAX	I_B Pin 9 = 2 µA; V_{CE} Pin 8 = $V_{CC(MAX)}$	MAX
			0.8		mA	T_A = 25°C		
			0.5		mA	T_A = 0°C;11C44DC		
			0.2		mA	T_A = -55°C;11C44DM		
I_{CES}	Amplifier Leakage Current	8		120	µA	Pin 9 = gnd; V_{CE} Pin 8 = $V_{CC(MAX)}$		MAX
V_{FD}	Diode Forward Voltage	5	0.5		V	I_{FD} Pin 5 = 1 mA; Pin 4 = gnd		5.0 V
I_{RD}	Diode Reverse Current	4		5.0	µA	V_R Pin 4 = 5.5 V; Pin 5 = gnd		5.0 V
I_{CC}	Power Supply Current	14		40	mA	Inputs Open		5.0 V

NOTES:
1. Min and Max refer to the recommended V_{CC} values for the particular device type.
2. Apply voltage or current sources to outputs only after outputs are in the appropriate states.
Outputs 2 and 13 require sequential RF-VF exercising to assure proper states.

TESTING — Testing the Phase/Frequency Detector requires some preliminary exercising of RF and VF to get U1 and D1 into predictable states. Any number of sequences can be devised from the flow table in *Figure 5. Figure 1* shows a sequence that contains all possible combinations of input, output, and internal states. This sequence can also be used cyclically, as suggested by the double designations of the last three steps, which makes it useful for the type of functional testing that requires repetitive output waveforms.

For parametric testing, which is normally much more time consuming than functional testing, it may be desirable to use a short sequence to minimize overall test time. In parametric testing, the act of disconnecting a forcing function from U1 or D1 often creates an electrical disturbance in the wiring and cabling, which in turn triggers the Phase/Frequency Detector into another state. It is therefore recommended that the inputs be resequenced between successive tests. *Figure 2* lists short sequences that get the outputs into the three possible combinations.

RF and VF should be sequenced in Grey code to avoid ambiguities due to timing differences in the RF-VF signal sources. Depending on the noise characteristics of the test apparatus, it is advisable to use RF-VF input signal levels considerably above the listed V_{IH} and below the V_{IL} levels. For an I_{SC} test, the RF-VF inputs should be in the O-O state to avoid retriggering through the internal feedback when U1 or D1 is forced to zero volts. Input sequencing is not required for testing U2 and D2. The truth table for the Phase Detector is shown in *Figure 3.*

STEP #	INPUTS		OUTPUTS	
	RF	VF	U1	D1
1	1	0	X	X
2	0	0	X	X
3	1	0	X	X
4	0	0	0	1
5	1	0	0	1
6	1	1	0	1
7	0	1	0	1
8	0	0	1	1
9	0	1	1	1
10	0	0	1	0
11	0	1	1	0
12	1	1	1	0
13	1	0	1	0
14	0	0	1	1
15	1	0	1	1
16	1	1	1	1
17/1	1	0	1	0
18/2	0	0	1	1
19/3	1	0	1	1

X = Undefined

Fig. 1 Cyclical Sequence for Phase/Frequency Detector Testing

STEP #	INPUTS		OUTPUTS	
	RF	VF	U1	D1
1a	1	0	X	X
2a	0	0	X	X
3a	1	0	X	X
4a	0	0	0	1
1b	1	1	X	X
2b	0	1	X	X
3b	0	0	X	X
4b	0	1	X	X
5b	0	0	1	0
1c	1	1	X	X
2c	1	0	X	X
3c	1	1	X	X
4c	1	0	X	X
5c	0	0	1	1

X = Undefined

Fig. 2 Short Sequences for Phase/Frequency Detector Testing

INPUTS		OUTPUTS	
RF	VF	U2	D2
0	0	1	1
0	1	1	1
1	0	0	1
1	1	1	0

Fig. 3 Phase Detector Truth Table

FUNCTIONAL DESCRIPTION — 11C44 operation is best explained by examining its role in a typical application, such as the phase-locked loop shown in the block diagram of *Figure 4*. In this arrangement a relatively low frequency oscillator is made to control a much higher frequency VCO. The ÷ N counter scales down the VCO output frequency (OF) and provides a variable frequency (VF) in the same range as the reference frequency (RF). For example, with RF of 100 kHz and OF of 120 MHz, the counter is set to divide by 1200. External controls such as thumbwheel switches are used to change the counter divide ratio, which in turn leads to a change in OF. Extending the foregoing example, changing the counter modules from 1200 to 1201 effectively reduces VF below 100 kHz. The detector generates an error signal which ultimately increases the VCO frequency until VF again equals RF at 100 kHz. The net result is that OF is increased to N x RF, in this case 120.1 MHz. The loop also corrects for VCO drift, since a change in OF causes VF to be higher or lower than RF, in turn causing the detector to generate a corrective signal and pull the VCO back into lock.

Phase detection can be performed by simple functions such as a latch or an Exclusive-OR, but these are susceptible to locking on harmonics. To avoid this effect, a detector must ignore repetitive state changes on one of its inputs unless and until a state change occurs on the other input. This requires internal memory. The 11C44 Phase/Frequency Detector contains several internal latches, as can be seen in the logic diagram. When power is first applied, the circuit can settle in any one of several states for any combination of RF and VF input states. Subsequent response to RF and VF transitions can be predicted from the sequential flow table of *Figure 5*.

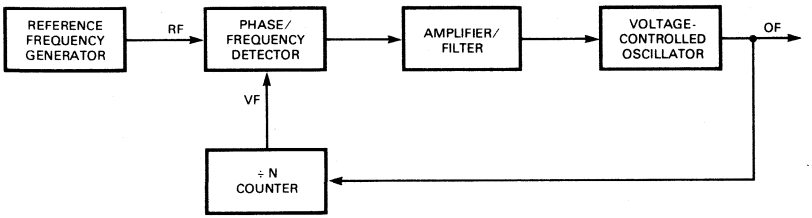


Fig. 4 General Arrangement for Phase-Locked Loop

Each possible combination of RF, VF, U1 and D1 is identified by a number in the flow table. If the number is in parenthesis, it indicates a stable state; without parenthesis it indicates an unstable state. Note that for any given combination of RF-VF inputs, *i.e.*, in each column, there are three possible stable states corresponding to the three possible combinations of U1 and D1. To determine the circuit response to an input change, first move horizontally from the column representing the present input combination to the column representing the new input combination. This will identify the new state number. If this new state number is not in parenthesis, move vertically to the same number in parenthesis. For example, if the RF-VF input combination changes from 1-1, with the circuit in state (7), to 1-0, move right to state 12. Since this is an unstable state, move down to (12). This is the new state of the circuit and is the starting point for determining circuit response to a subsequent input change.

The flow table shows that if the inputs change back and forth between 0-0 and 1-1, the circuit changes state accordingly between (5) and (7), while U1 and D1 remain in the 1-1 condition. Note that when RF-VF changes back and forth repeatedly between 0-0 and 1-1, it means that the two inputs agree both in phase and frequency. Thus the constant 1-1 signals from U1 and D1 indicate the LOCK condition. *Figures 6* and *7* show how U1 and D1 respond when RF and VF differ in frequency or phase. State numbers correspond to stable states in the flow table. In *Figure 6a*, VF is lower in frequency than RF, causing a periodic LOW signal from U1 and a constant HIGH from D1. The U1 signal indicates that the VCO frequency should be increased. In *Figure 6b*, VF is higher than RF, causing a periodic LOW signal from D1 and a constant HIGH from U1. The D1 signal means that the VCO frequency should be decreased.

Figures 7a and *7b* show that the Phase/Frequency Detector can respond in either of two ways to the same set of RF and VF inputs, if they differ in phase but have the same frequency. In *Figure 7a*, the circuit is assumed to start in state (2); the result is a signal at U1 whose duration in the LOW state is 50% of a full cycle time, indicating that VF lags RF by 180°. In *Figure 7b*, the circuit is assumed to start in state (6), leading to a D1 signal whose LOW duration is 50% of a full cycle time. This indicates that VF leads RF by 180°, which is, of course, the same as saying that VF lags RF by 180°. Thus the output indications of *7a* and *7b* are equivalent. Other supplementary lead/lag angle indications can also occur, such as 90° lead/270° lag, 120° lead/240° lag, etc. These situations are not likely to arise in any operating loop but can easily occur in bench tests using a pair of slaved pulse generators for RF and VF signal sources and momentarily interrupting V_{CC} to the detector.

RF-VF INPUT STATES				OUTPUTS	
0-0	0-1	1-1	1-0	U1	D1
(1) 5	2 (2)	3 (3)	(4) 8	0 0	1 1
(5) 9	6 (6)	7 7	8 1 2	1 1	1 1
5 1	2 2	(7) 7	12 (8)	1 1	1 1
(9) 5	(10) 6	11 (11)	12 (12)	1 1	0 0

Fig. 5 Flow Table for Phase/Frequency Detector

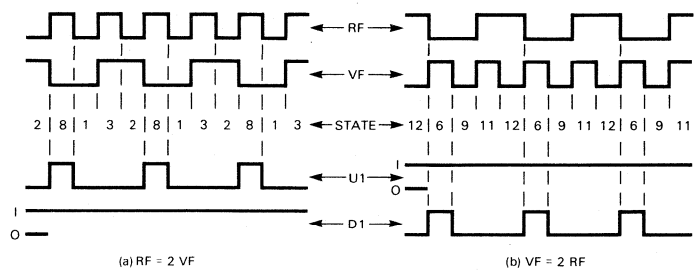


Fig. 6 Phase/Frequency Detector Response for Unequal Input Frequencies

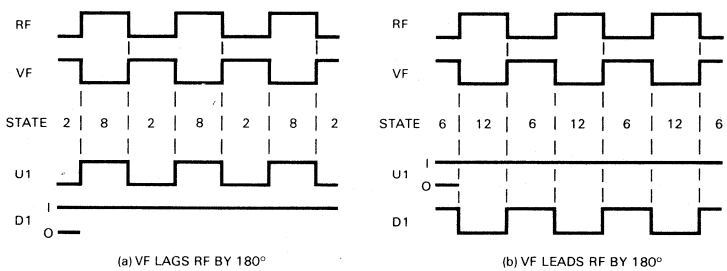


Fig. 7 Alternate Interpretations by the Phase/Frequency Detector

FUNCTIONAL DESCRIPTION (Cont.)
The Charge Pump consists of a diode connected between terminals PU and UF, and a special inverter between terminals PD and DF. The inverter output has only a pull-up transistor. Thus when DF is HIGH, it is a low impedance source with an output voltage of about +2.25 V. When the PD input goes HIGH, the base of the DF pull-up transistor is held near ground potential and thus the DF output is a very high impedance. With the Charge Pump driven from the Phase/Frequency Detector as indicated in *Figure 8*, a LOW signal at the PU input causes the UF output to be a low impedance to ground, with an output voltage of approximately +0.75 V. When the PU input is HIGH, the diode is back biased and is thus a high impedance. For symmetric phase detector gain in the pump-up and pump-down modes, the effective input threshold of the amplifier, symbolized as V_{REF} in *Figure 8*, should be midway between the UF level of +0.75 and the DF level of +2.25 V, or about +1.5 V.

Figure 9 shows an arrangement for evaluating detector output as a function of phase difference between RF and VF. The internal delay controls of the pulse generators provide phase angle variations approaching ±360°, limited somewhat by the tendency of a pulse generator to become erratic when the internal delay approaches the pulse period. With the generator outputs in phase, the Charge Pump produces no output pulses and the measured voltage is +1.5 V. Dealying the output of a generator A with respect to B causes the Charge Pump to produce positive pulses extending to +2.25 V. The pulse duration is equal to the time between the negative edge of B and the negative edge of A. As the delay is increased toward a full cycle (360°), the filtered output approaches +2.25 V. Conversely, delaying the output of generator B with respect to A causes the Charge Pump to produce negative pulses extending down to +0.75 V. The pulse duration equals the delay from the negative edge of A to the negative edge of B; as the delay approaches 360°, the filtered output approaches +0.75 V. Plotting the output voltage as a function of lead or lag angle gives the characteristic shown in *Figure 10*. The slope of the characteristic, and thus the detector gain, is approximately 0.12 V/radian.

The variation of detector gain in the vicinity of zero phase difference is of particular interest to system designers. Finite internal delays limit the ability of the Phase/Frequency Detector to respond to small differences in timing between the negative edges of RF and VF. This causes a dead zone in the middle of the characteristic, which can be seen in the expanded graph of *Figure 11*. Immediately to either side of this dead zone the detector gain is greater than average. This effect is also due to internal detector responses involving some of the unstable states shown in the flow table *(Figure 5)* and the internal race conditions which accompany them. The logic circuitry of the 11C44 Phase/Frequency Detector is designed with careful attention to internal switch points, time constants, and path delays. This results in much less severe gain variations than exhibited by the MC4044, as indicated in *Figure 11*.

The Phase Detector has no internal storage, thus the U2-D2 output signals are strictly a function of the present state of RF-VF. From the truth table of *Figure 3*, it can be seen that if the RF and VF input signals have the same frequency and phase, *i.e.*, switch back and forth between 1-1 and 0-0, the U2 output is always HIGH and the D2 output has a 50% duty cycle. If the RF-VF signals switch between 0-1 and 1-0 (180° out of phase), D2 will remain HIGH and the U2 output will exhibit a 50% duty cycle. For any other phase angle between RF and VF, U2 and D2 will each be active (LOW) during some part of an input cycle. For a 90° phase angle between RF and VF, U2 and D2 will each exhibit a 25% (LOW) duty cycle.

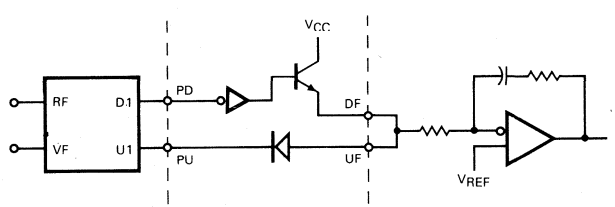
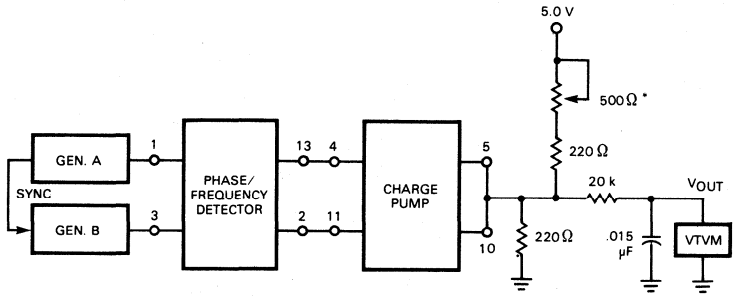


Fig. 8 Charge Pump Connections



*Adjust for V_{OUT} = 1.5 V with D.U.T. unplugged.

Fig. 9 Phase/Frequency Detector Gain Test

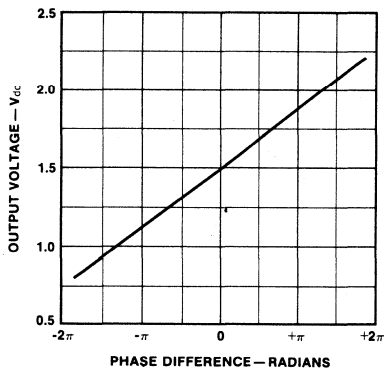


Fig. 10 Output Voltage vs Phase Difference

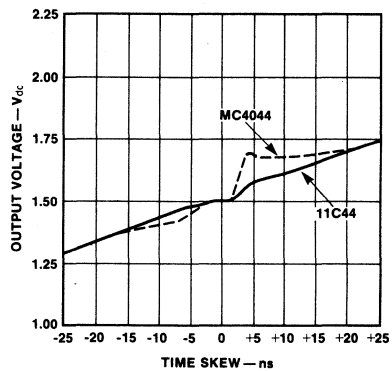
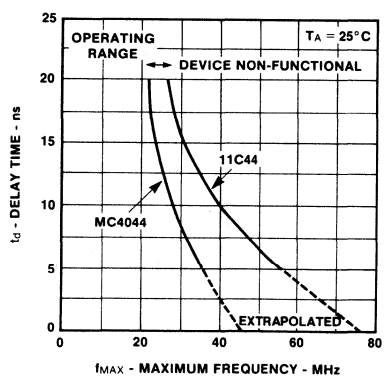
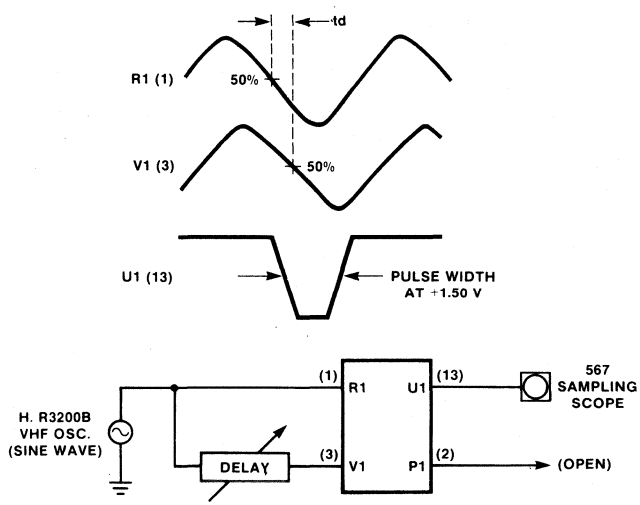


Fig. 11 Detector Output Response Near Lock





DELAY TIME VS MAXIMUM FREQUENCY

11C58

VOLTAGE CONTROLLED MULTIVIBRATOR

11C00 SERIES

GENERAL DESCRIPTION – The 11C58 is an ECL astable multivibrator utilizing current mode circuitry and having emitter follower buffers to provide ECL output levels. Operating frequency is determined by an applied voltage V_{CX} in conjunction with an external timing capacitor C_X.

The circuit is designed to accommodate a V_{CX} dynamic range of 2 V, which causes a frequency change of typically four to one for a given C_X value. Operating frequency ranges from typically 155 MHz with 5 pF C_X to low frequencies determined only by practical limits on capacitor size.

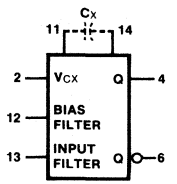
Noise on the analog input signal can be decoupled by connecting a bypass capacitor from the Input Filter terminal to ground. Similarly, a bypass capacitor from the Bias Filter to ground helps eliminate ripple on the output signal at high frequencies.

- **BROAD FREQUENCY RANGE — DC TO 155 MHz**
- **TRUE AND COMPLEMENT OUTPUTS**
- **50 Ω DRIVE CAPABILITY**
- **USES STANDARD TTL OR ECL POWER SUPPLY**
- **ONLY ONE TIMING CAPACITOR REQUIRED**

FUNCTIONS

V_{CX}	Applied Control Voltage
Bias Filter	For Ripple Elimination
Input Filter	For Input Noise Decoupling
C_X	External Timing Capacitor
Q, $\overline{Q}$	Outputs

LOGIC SYMBOL

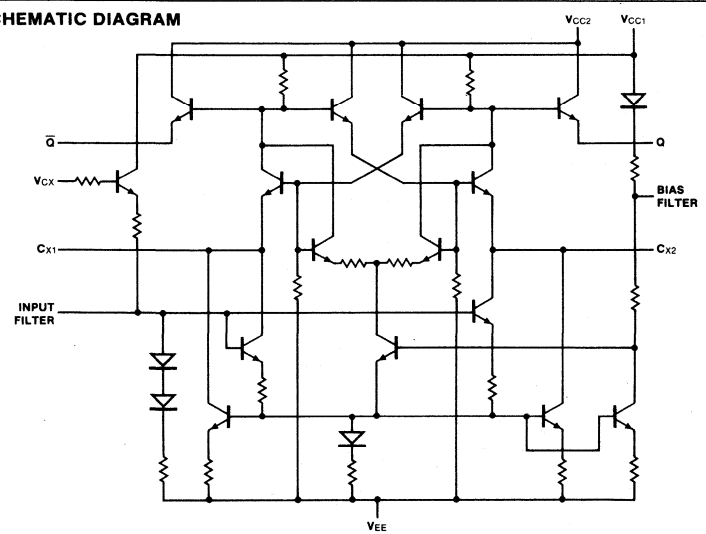


V_{CC1} = Pin 1

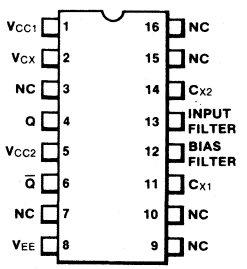
V_{CC2} = Pin 5

V_{EE} = Pin 8

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW0)



9

FUNCTIONAL DESCRIPTION — The simplified schematic and waveforms of *Figure 1* highlight basic operation of the 11C58. Q1 and Q4 turn on and off alternately, while Q2 and Q3 serve as level shifting buffers. C_X is alternately charged in different directions by the voltage controlled current sources I_1 and I_2 acting in conjunction with Q1 and Q4. To follow through a cycle of operation, assume that Q1 has just turned on, causing a positive voltage step at its emitter and a negative step at its collector. Since the voltage across C_X cannot change instantaneously, the positive step also appears at Q4 emitter. Simultaneously the negative step is applied through Q2 to the base of Q4. Thus Q4 is turned off and Q1 supplies the current required to satisfy I_1 and I_2. Since I_2 must flow through C_X, the voltage across C_X starts decreasing linearly. During the time that Q1 is on, the base-emitter voltages of Q3 and Q1 in series hold V_{11} constant at about 2 V_{BE} below V_{CC}. With V_{11} constant and C_X discharging linearly, Q4 emitter voltage is a negative going ramp, as indicated by the V_{14} waveform sketch.

This negative ramp eventually reaches a point where the base-emitter junction of Q4 becomes forward biased. Thus Q4 starts turning on and its collector current I_{C4} causes a negative going voltage drop across R2 which is applied by Q3 to the base of Q1. This reduces I_{C1}, which decreases the voltage drop across R1. The resultant positive going voltage at the base of Q2 is applied to Q4, which accelerates the turn-on of Q4. The circuit reaction is thus regenerative and produces a negative going voltage step at the Q4 collector and a positive step at the Q4 emitter. The negative step is applied by Q3 to Q1 base while the positive step is applied through C_X to the Q1 emitter. Q1 is thus turned off and I_1 starts charging C_X in the opposite direction, producing the negative going ramp shown on the V_{11} waveform. At the end of this ramp Q1 is again turned on and the circuit returns to the conditions assumed for the starting point of this analysis.

The full schematic shows that I_1 and I_2 each consists of a fixed current source in parallel with a variable current source controlled by the applied voltage V_{CX}. The useful range of V_{CX} is from V_{CC} to (V_{CC} - 2 V). From a given operating point within this range, making V_{CX} more positive increases the charging current and thus increases the operating frequency. For a given value of V_{CX}, operating frequency and C_X are inversely proportional, as indicated in the graph of *Figure 2*. Note that stray capacitances tend to predominate when C_X is small. The product of frequency and C_X is plotted in *Figure 3* as a function of V_{CX}. Note that V_{CC} is taken as the ground reference for the V_{CX} scale.

The total current switched through R1 and R2 is maintained constant, in spite of changes in charging current, by a pair of transistors with their bases and collectors connected in common with those of Q1 and Q4. This pair of transistors functions as a simple current switch operating in synchronism with Q1 and Q4. The current supplied to the emitters of this switching pair is automatically adjusted by internal circuitry to offset any changes in the charging current. By thus maintaining a constant total current through R1 or R2, the output voltage swing is made independent of V_{CX}.

SIMPLIFIED SCHEMATIC AND WAVEFORMS

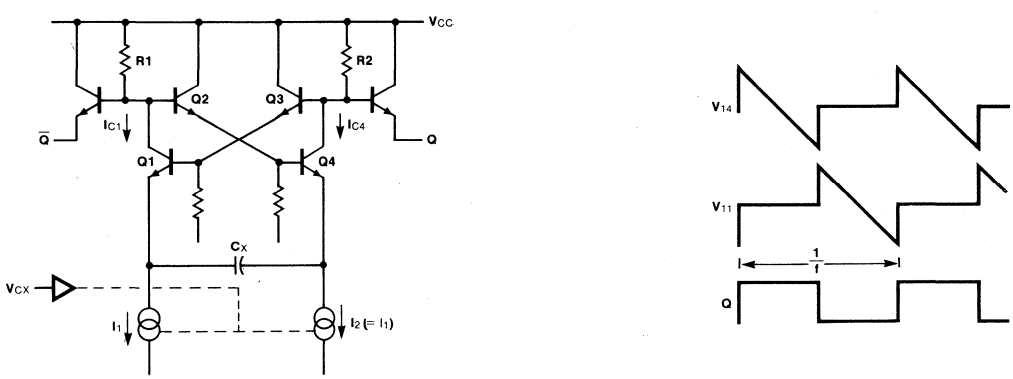


Figure 1

The net voltage across C_X changes from a peak of approximately 0.8 V of one polarity at the beginning of a ramp to 0.8 V in the opposite polarity at the end of the same ramp. The capacitor chosen for C_X should thus be capable of withstanding 1 V in either direction; for waveform symmetry its capacitance-vs-voltage characteristic should be linear over this range.

The power supply for the 11C58 can have its negative side designated as the bround reference, as is commonly done with TTL/DTL circuits, or the positive terminal can be designated as ground as is usually done in an ECL system. This latter configuration is preferable for incoming test purposes and is assumed as a condition for the specifications given in the dc test table. Notice that the ac test arrangement uses split power supplies to offset V_{CC} above scope ground by +2.0 V. This offset allows the 50 Ω terminations built into the sampling scope inputs to act as the specified standard loads for the 11C58 outputs. This in turn allows direct connection of the circuit to the scope using coaxial cables, thereby eliminating high impedance probes and possible problems of improper loading, impedance mismatch, improper compensation, bandwidth limitations and unequal channel delay.

The 11C58 can be operated from the same +5.0 V ±5% supply with TTL circuits, provided that good rf bypassing is used to prevent the effects of TTL current spikes from affecting 11C58 operation. These spikes create noise on both the positive and negative sides of the supply and are most effectively limited by capacitors placed close to the TTL packages.

TYPICAL CHARACTERISTICS

OUTPUT FREQUENCY vs CAPACITANCE FOR VARIOUS VALUES OF INPUT VOLTAGE

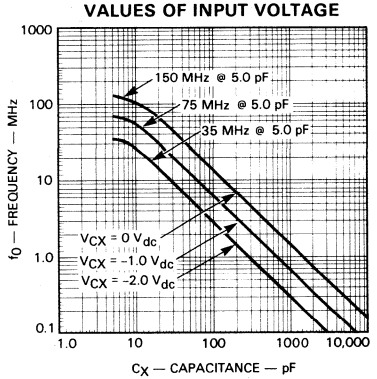


Figure 2

FREQUENCY-CAPACITANCE PRODUCT vs CONTROL VOLTAGE (V_{CX}) FOR C_X > 10 pF

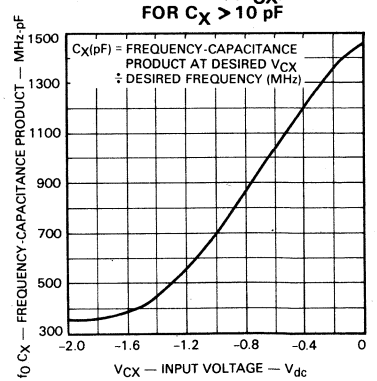


Figure 3

DC CHARACTERISTICS: V_{EE} = -5.2 V, V_{CC1} = V_{CC2} = GND

SYMBOL	CHARACTERISTIC	LIMITS A	LIMITS B	UNITS	T_A	CONDITIONS
V_{OH}	Output Voltage HIGH	-1000 -960 -900	-840 -810 -720	mV	0°C 25°C 75°C	Note 1 for Pin 6; Note 2 for Pin 4 V_{CX} = -1.0 V Loading is 50 Ω to -2 V
V_{OL}	Output Voltage LOW	-1870 -1850 -1850	-1620 -1620 -1595	mV	0°C 25°C 75°C	Note 2 for Pin 6; Note 1 for Pin 4 V_{CX} = -1.0 V Loading is 50 Ω to -2 V
I_{IH}	Input Current HIGH		350	µA	25°C	V_{CX} = Gnd Note 2
I_{IL}	Input Current LOW	-0.5		µA	25°C	V_{CX} = -2.0 V Note 2
I_{EE}	Power Supply Current	-32		mA	25°C	Note 1 or Note 2

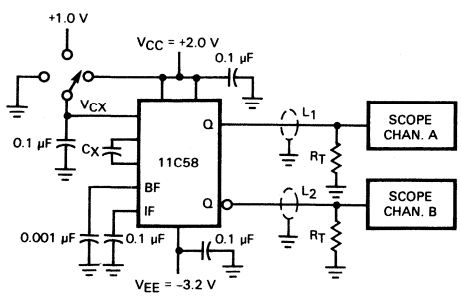
NOTES:

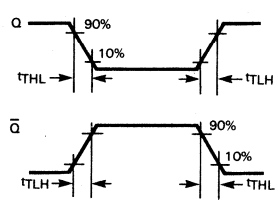
1. Connect germanium or Schottky diode (11)—(14)
2. Connect germanium or Schottky diode (11)—(14)

AC CHARACTERISTICS: V_{EE} = -3.2 V, V_{CC1} = V_{CC2} = +2.0 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS A	LIMITS TYP	LIMITS B	UNITS	CONDITIONS	
t_{TLH}, t_{THL}	Transition Time (10%-90%) or (90%-10%)			3.0	ns	V_{CX} = +2.0 V	C_X = 5 pF
				4.6	ns	V_{CX} = +1.0 V	
				8.5	ns	V_{CX} = Gnd	
f_{OSC1}	Oscillation Frequency	130	155	175	MHz	V_{CX} = +2.0 V, C_X = 5 pF	
f_{OSC2}	Oscillation Frequency	78	90	100	MHz	V_{CX} = +2.0 V, C_X = 10 pF	
TR	Tuning Ratio Test	3.1	4.5			$TR = \frac{f_{OSC} @ V_{CX} = +2.0\ V}{f_{OSC} @ V_{CX} = Gnd}$	C_X = 10 pF

SWITCHING CIRCUIT AND WAVEFORMS





L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope

11C70

MASTER/SLAVE D FLIP-FLOP

11C00 SERIES

GENERAL DESCRIPTION – The 11C70 is a high-speed ECL D Type Master/Slave Flip-Flop capable of toggle rates over 650 MHz. Designed primarily for communications and instrumentation, it can also be used in other digital applications and is fully compatible with 10,000 Series ECL. Asynchronous Direct Set and Direct Clear inputs are provided which override the clock.

The circuit is voltage compensated, which makes output levels and input thresholds insensitive to V_{EE} variations. This also allows operation with ECL supply voltage V_{EE} of −5.2 V or with TTL supply V_{CC} of +5.0 V. Each input has an internal 50 kΩ pull-down resistor, which allows unused inputs to be left open. Open emitter-follower outputs accommodate a variety of loading and terminating schemes. The 11C70 is pin compatible with the Motorola MC1670 but is a higher frequency replacement.

- **TOGGLE FREQUENCY 650 MHz TYP AT 25°C**
- **VOLTAGE COMPENSATED**
- **COMPLEMENTARY SIMULTANEOUS OUTPUTS**
- **INTERNAL 50 kΩ (NOMINAL) PULL-DOWN RESISTORS**
- **OPEN EMITTER FOLLOWER OUTPUTS DRIVE TERMINATED LINES**
- **SEPARATE V_{CC} PINS ELIMINATE NOISE COUPLING**

PIN NAMES

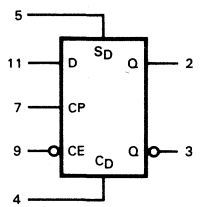
$\overline{CE}$	Clock Enable (Active LOW)
CP	Clock Pulse
D	Data Input
Q, $\overline{Q}$	Complementary Outputs
S_D	Direct Set
C_D	Direct Clear

TRUTH TABLE

INPUTS					Q_{t+1}	OPERATION
S_D	C_D	D	$\overline{CE}$	CP		
H	L	X	X	X	H	Direct Set
L	H	X	X	X	L	Direct Clear
H	H	X	X	X	–	Indeterminate
L	L	X	H	⌐	Q_t	Disable Clock
L	L	H	L	⌐	H	Clocked Set
L	L	L	L	⌐	L	Clocked Clear

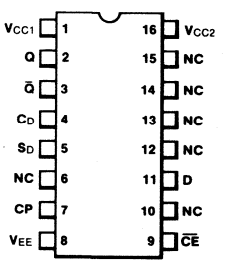
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
t, t+1 = Time before and after Clock positive transition

LOGIC SYMBOL



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION — Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times. While the clock is LOW, the slave is in a HOLD condition and information present on the D input is gated into the master. When the clock goes HIGH, it locks the master into its present state, making it insensitive to the D input, causing the new information to appear on the outputs.

The CP and $\overline{CE}$ inputs are logically identical, but physical constraints associated with the Dual In-Line package make the $\overline{CE}$ input slower at the upper end of the toggle range. To prevent new data from entering the master on the next CP LOW cycle, $\overline{CE}$ should be HIGH while CP is still HIGH.

A HIGH signal on S_D or C_D will override the clocked inputs and force Q or $\overline{Q}$, respectively, to go HIGH. If both C_D and S_D are HIGH, the two output voltages will be somewhere between the HIGH and LOW levels and thus, cannot be usefully defined.

When the input signals for the 11C70 come from other ECL circuits, either 11C00 series or 10,000 series types, these circuits will automatically provide appropriate signal swings. Provided, of course, that these circuits are operated within their ratings and that due consideration is given to terminations appropriate to the particular application, as discussed in the Fairchild ECL Handbook.

For applications wherein the clock signal comes from a circuit type other than ECL (in high frequency prescaling, for example) it is generally necessary to use external components to shift the signal levels and center them about the 11C70 input threshold region. A typical biasing scheme is shown in *Figure 1*. Resistors R1 and R2 are chosen such that the quiescent voltage at the CP input is -1.3 V with respect to the V_{CC} terminal of the 11C70. Also indicated is the coupling from $\overline{Q}$ back to the D input to make a simple toggle. The clock source should be designed to provide a signal swing in the range of 400 mV to 1200 mV, peak-to-peak, over the specified frequency and temperature range. To avoid saturating the input transistor, and thus limiting the frequency capability, the positive peak of the clock should not be more positive than -0.4 V with respect to V_{CC}.

The 11C70 outputs have no internal pull-down resistors. When driving a microstrip line terminated at the far end by a resistor returned to -2 V (w.r.t. V_{CC}), the quiescent I_{OH} current in the line performs the pull-down function when the output starts to go LOW. For series termination or for short unterminated lines, a 270 Ω resistor to V_{EE} will provide adequate pull-down current. The outputs switch slightly faster when both outputs are equally loaded than if only one output is loaded. Equal and opposite changes in Q and $\overline{Q}$ load currents tend to cancel the effects of the small but finite inductance of the V_{CC} pin.

The test arrangements illustrate the use of split power supplies, with a 2 V V_{CC} and -3.2 V V_{EE}. This is done as a matter of instrumentation convenience, since it allows the outputs to be connected via 50 Ω cables directly to the sampling scope inputs, which have 50 Ω internal terminations. By thus avoiding the use of probes, test correlation problems between supplier and user are minimized. In actual applications, only a single power supply is needed, and ground can be assigned to V_{CC}, as in ECL systems, or to the V_{EE} side as in TTL systems. RF bypass capacitors are recommended in either case.

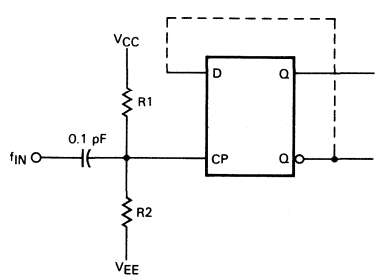


Fig. 1. Input Biasing for AC Coupled Triggering

DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
V_{OH}	Output Voltage HIGH	−1000		−840	mV	0°C	
		−960		−810		25°C	
		−900		−720		75°C	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table
V_{OL}	Output Voltage LOW	−1870		−1665	mV	0°C	Loading 50 Ω to −2 V
		−1850		−1620		25°C	
		−1850		−1595		75°C	
V_{OHC}	Output Voltage HIGH	−1020			mV	0°C	
		−980				25°C	
		−920				75°C	$V_{IN} = V_{IHB}$ or V_{ILA} for D Input
V_{OLC}	Output Voltage LOW			−1615	mV	0°C	Loading 50 Ω to −2 V
				−1600		25°C	
				−1575		75°C	
V_{IH}	Input Voltage HIGH	−1135		−840	mV	0°C	Guaranteed Input Voltage HIGH for
		−1095		−810		25°C	All Inputs
		−1035		−720		75°C	
V_{IL}	Input Voltage LOW	−1870		−1500	mV	0°C	Guaranteed Input Voltage LOW for
		−1850		−1485		25°C	All Inputs
		−1830		−1460		75°C	
I_{IH}	Input Current HIGH				μA	25°C	$V_{IN} = V_{IHA}$
	Clock Input			250			
	Data Input			270			
	S_D and C_D			550			
I_{IL}	Input Current LOW	0.5			μA	25°C	$V_{IN} = V_{IHB}$
I_{EE}	Power Supply Current	−48			mA	25°C	All Inputs Open

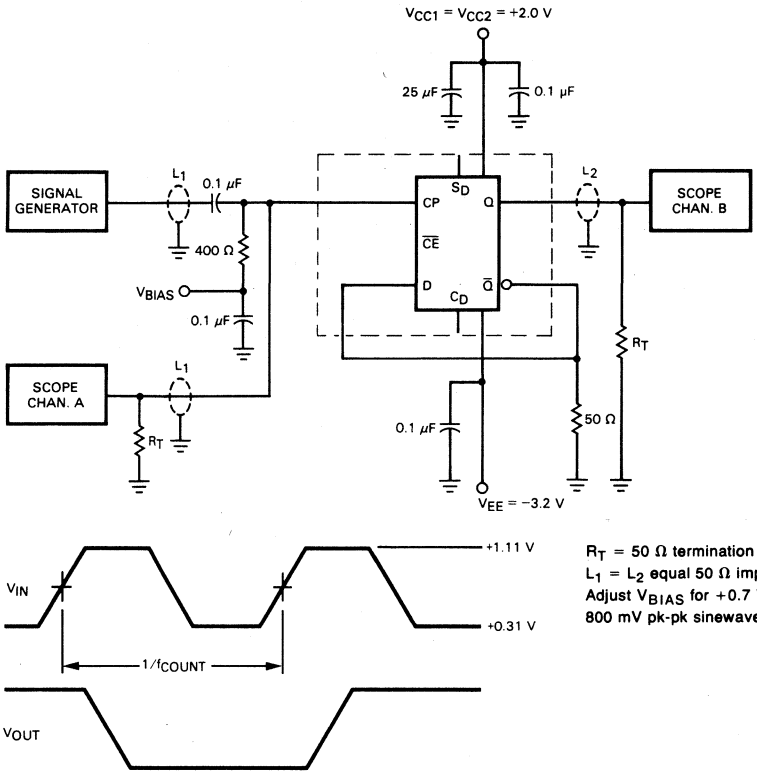
AC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PHL}, t_{PLH}	Propagation Delay (CP−Q)	0.8	1.1	1.4	ns	
t_{PLH}, t_{PHL}	Propagation Delay (S_D−$\overline{Q}$, C_D−Q)		1.3	1.7	ns	See Figures 3 and 4
t_{TLH}	Transition Time 20%−80%		0.9	1.3	ns	
t_{THL}	Transition Time 80%−20%		0.9	1.3	ns	
$f_{TOG(max)}$	Toggle Frequency (CP)	550	650		MHz	See Figure 2

NOTE: This device is guaranteed for $f_{TOG(max)} \geq 500$ MHz over the 0°C to 75°C temperature range.

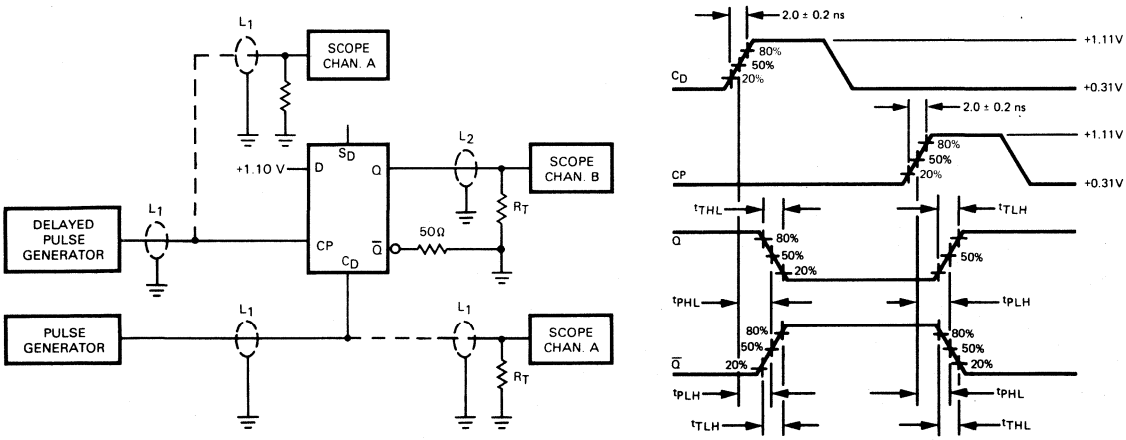
9

AC CIRCUITS AND WAVEFORMS



R_T = 50 Ω termination of scope
$L_1 = L_2$ equal 50 Ω impedance lines
Adjust V_{BIAS} for +0.7 V baseline of 800 mV pk-pk sinewave input

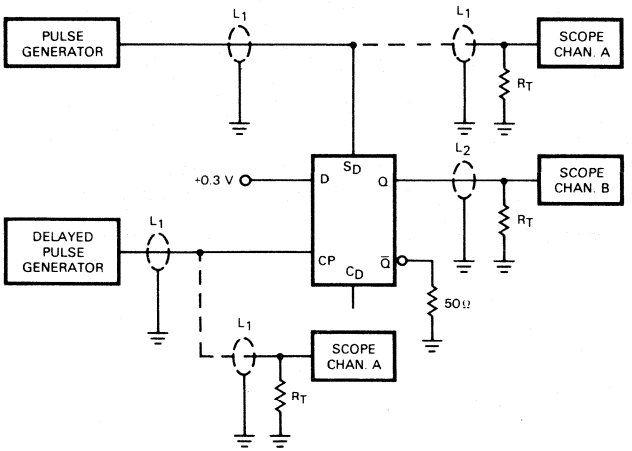
Fig. 2. Toggle Frequency Test Circuit

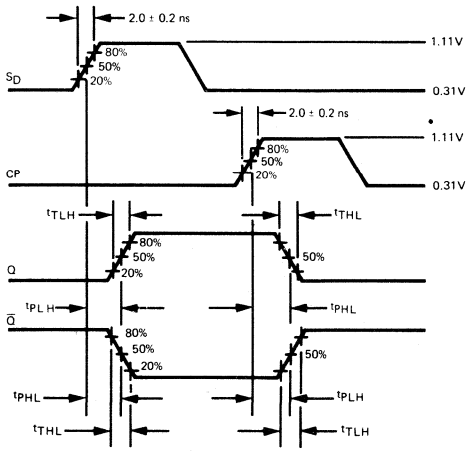


$V_{CC1} = V_{CC2}$ = +2.0 V
V_{EE} = −3.2 V
R_T = 50 Ω termination of scope
$L_1 = L_2$ equal 50 Ω impedance lines
All input transition times are 2 ± 0.2 ns

Fig. 3. Propagation Delay and C_D Test Circuit

AC CIRCUITS AND WAVEFORMS (Cont'd)





$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\ \Omega$ termination of scope
$L_1 = L_2$ equal 50 Ω impedance lines
All input transition times are 2 ± 0.2 ns

Fig. 4. Propagation Delay and S_D Test Circuit

11C83

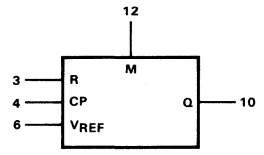
1 GHz DIVIDE-BY-248/256 PRESCALER

11C00 SERIES

GENERAL DESCRIPTION – The 11C83 Prescaler is guaranteed to operate above 950 MHz over the 0°C to +75°C temperature range and with a V_{CC} variation from +4.75 to +5.5 V. The circuit requires only one supply voltage and the clock input signal can be either dc or ac coupled. The prescaler divides by either 248 or 256, as determined by the signal applied to the Mode Control (M) input. This feature makes it possible to use the 11C83 in conjunction with other logic to achieve a broad range of overall divide ratios, either fixed or programmable. For example, a divide ratio of 1000 can be achieved by one 11C83 and one 9LS161 modulo-16 counter.

- **DC TO 950 MHz OPERATION – GUARANTEED OVER 0°C TO +75°C**
- **DC OR AC COUPLED INPUT**
- **USES STANDARD TTL OR CMOS POWER SUPPLY**
- **OUTPUT DRIVES TTL OR CMOS**
- **DIVIDE BY 248/256 MODE CONTROL**

LOGIC SYMBOL



V_{CC} = Pin 1
V_{CCA} = Pin 14
GND = Pin 7

FUNCTIONS

CP = Clock pulse input

M = Mode Control input
LOW = ÷ 248
HIGH = ÷ 256

Q = Output w/2K pull-up

R = 10 kΩ to GND, for optional CP offset

V_{REF} = Internal reference voltage, for ac coupled clocking

FUNCTIONAL BLOCK DIAGRAM

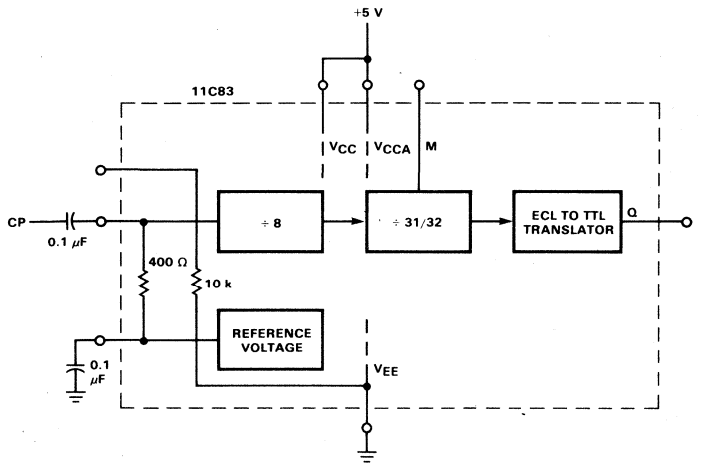
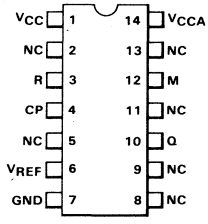


Fig. 1.

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)



FUNCTIONAL DESCRIPTION — The 11C83 contains a 3-stage modulo-8 divider whose output drives a 5-stage modulo-31/32 divider. The 5-stage circuit has a natural divide ratio of 32, but a LOW signal on the Mode Control input causes it to skip one state and thus divide by 31. Referred to the CP input, this changes the overall divide ratio from 256 to 248. Both dividers are designed with ECL circuitry and the divide-by-31/32 drives an ECL-to-TTL translator. The translator has a 2 kΩ pull-up resistor returned to V_{CC} through a diode and thus will pull up high enough to drive CMOS as well as TTL inputs. In the LOW state, the output can sink 10 mA at a V_{OL} level of 0.5 V or less.

The relationship between the output waveform, the divide ratio and the Mode Control input signal are outlined in *Figure 2*. The trigger pulses shown are those which operate the divide-by-31/32 circuit. Although these pulses cannot be monitored, they are convenient to use as timing references in discussing delay time, setup time and, by extension, timing constraints on any external logic used to generate Mode Control signals. As shown, the output is LOW for 16 pulse periods regardless of the state of M. The duration of the output HIGH state, however, can be either 15 or 16 pulse periods. The pulse edge that makes Q go HIGH is identified as t_0. The 15th following pulse edge causes Q to go LOW if M is LOW at least 3 ns before t_{15}. If M is HIGH at this time, Q will go low after the 16th pulse edge following t_0.

The mutual constraints between the maximum operating frequency and the total delay in generating the M input signal can be deduced by considering an example. *Figure 3* shows an 11C83 driving the clock input of a 9LS161 Modulo-16 Counter. The table shows that the 9LS161 counts up from 5 to 8 and then presets back to 5 to repeat the sequence. Its Q_2 and Q_3 outputs drive the Preset Enable of the 9LS161 and the M input of the 11C83. The clock input of the 9LS161 responds to the positive-going edge of the 11C83 output and, thus, it is appropriate to evaluate delays from t_0 of *Figure 2*. The indicated t_{PLH} consists of a worst-case delay of 25 ns, plus the time to rise to the 1.3 V level at the 9LS161 input. For a stray capacitance of 10 pF, this rise will not exceed 10 ns. Thus the t_{PLH} in *Figure 2* will be 35 ns or less.

The worst-case t_{PLH} of the 9LS161, from CP to Q, is 20 ns with a 15 pF load and is measured to the 1.3 V level on the rising output. The Q_3 output must rise further, however, to reach the V_{IH} level of the M input, which is approximately 1.5 V below V_{CC}. This extra rise takes about 8 ns. Note that an external 2 kΩ pull-up resistor is shown in *Figure 3*. This provides additional HIGH state noise margin and also helps the Q_3 rise rate. This resistor also tends to increase the t_{PHL} of the 9LS161, as measured at the 1.3 V level, but this is not a critical timing factor because the falling Q_2 output is effectively in the LOW state as soon as it passes through the V_{IL} level of the 11C83 M input, at about 2.6 V.

For this example, the cumulative delays from t_0 of *Figure 2* are 35 ns t_{PLH} to the 9LS161 CP input plus 28 ns to the 11C83 M input. Adding 3 ns setup time for M preceding t_{15} gives a minimum time of 66 ns for the period of 15 pulses into the divide-by-31/32 circuit. But at a frequency of 1 GHz into the divide-by-8 circuit, the pulse frequency into the divide-by-31/32 is 125 MHz and 15 pulse periods constitute 120 ns. Thus the frequency limit for *Figure 3* is that of the 11C83 input, rather than the delays in the Mode Control feedback loop. A different result is obtained by replacing the 9LS161 with the F40161 CMOS equivalent. CMOS delays are measured between the 50% points, or 2.5 V with a 5 V supply. Thus the 11C83 output rise time is measured to the 2.5 V level rather than 1.3 V, which takes approximately 25 ns rather than 10 ns. The worst-case t_{PLH} of the F40161 is 185 ns to the 2.5 V level and the output rise from 2.5 V to 3.5 V takes another 5 ns. Substituting these numbers in the previous example gives 243 ns minimum for the period of 120 pulses into the divide-by-8. This gives an upper frequency limit of about 495 MHz. The frequency limit can be extended by using a logic inverter between the 11C83 output and the clock input of the F40161. This makes the F40161 trigger when the 11C83 output goes negative, rather than positive, which precedes t_0 by the period of 128 pulses into the divide-by-8. Since the 11C83 output falls to 2.5 V much faster than it rises, a CMOS inverter increases the total delay to only about 260 ns. This is the minimum period for 248 pulses into the divide-by-8, which translates to a maximum frequency of 955 MHz. Note that the 2 kΩ pull-up resistor of *Figure 3* is not required with the CMOS counter, nor is it desirable from the standpoint of loading the Q_2 output in the LOW state.

If an application requires a prescaler output HIGH signal level more positive than +5 V, it will be necessary to use a discrete transistor or some other type of interface circuit. The use of an external pull-up resistor returned to a higher voltage is not recommended, due to the possibility of causing latch-up in the output transistor. This voltage limitation is one of the trade-offs necessary to achieve transistors with the bandwidth required for 1 GHz counting.

The 11C83 clock input is one side of a differential switch whose other side is connected to an internally generated reference voltage. A 400 Ω internal resistor is connected between the clock input and reference voltage, as shown in *Figure 1*. This biases the input in the middle of the threshold region, which maximizes the input sensitivity and eliminates the need for external biasing resistors with capacitively coupled clocking. Also provided is a 10 kΩ resistor returned to V_{EE}. For ac coupled applications in which a clock signal is not always present, this resistor (pin 3) should be connected to the clock pin. This offsets the input sufficiently to avoid extreme sensitivity to noise when no signal is present. Otherwise, noise triggering can lead to oscillation at about 300 MHz. For dc coupled clocking the input signal levels should be designed to provide the specified V_{IH} and V_{IL} levels, which are nominally 2.5 V and 3.3 V below V_{CC}, respectively.

For a sinusoidal input waveform the minimum frequency of operation is about 50 MHz, due to edge rate limitations. Operation down to dc is possible provided that the input pulse edges have a slew rate of 50 V/μs or better. Minimum peak-to-peak trigger amplitude as a function of frequency is shown in *Figure 4*. Maximum recommended trigger amplitude is 1200 mV pk-pk. An rf bypass capacitor should be connected between V_{REF} (pin 6) and ground to maintain input sensitivity and to make the input impedance independent of internal switching. Input impedance is 54 Ω resistive at 1 GHz and has a capacitive component at lower frequencies, as shown in *Figure 5*. The 11C83 uses separate V_{CC} pins for the faster and slower parts of the circuit to prevent any interaction through the medium of lead inductance. The two V_{CC} pins should be connected together as close to the package as possible. Low impedance V_{CC} and V_{EE} (GND) distribution and rf bypass capacitors are recommended to prevent crosstalk with other circuits.

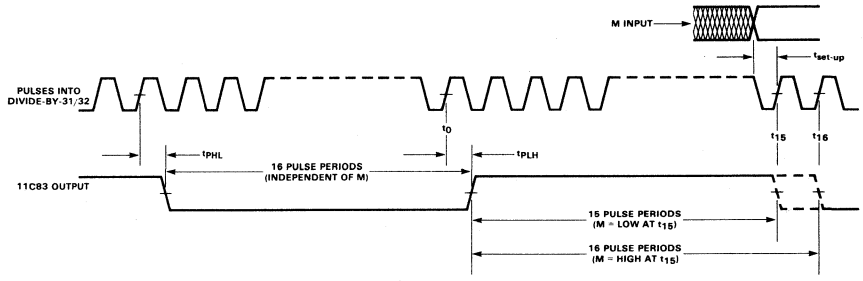
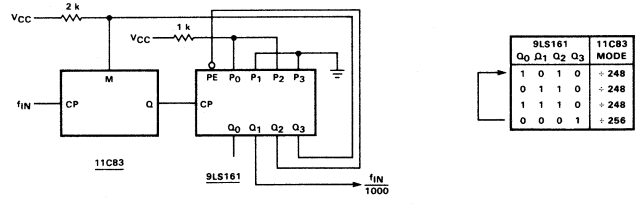


Fig. 2 Effect of M on Output Duty Cycle



9LS161 Q_0 Q_1 Q_2 Q_3	11C83 MODE
1 0 1 0	÷ 248
0 1 1 0	÷ 248
1 1 1 0	÷ 248
0 0 0 1	÷ 256

Fig. 3 Divide-by-1000 Obtained by Pulse-Swallowing

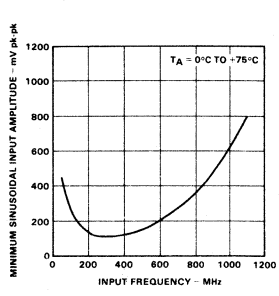


Fig. 4 AC Coupled Triggering Characteristics

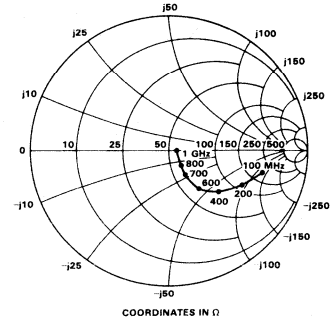


Fig. 5 High Frequency Input Characteristics

DC CHARACTERISTICS: Over operating temperature and voltage range unless otherwise specified: Pins 1 and 14 = V_{CC}, Pin 7 = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.7	3.6		V	V_{CC} = 4.75 V, I_{OH} = 240 μA
		3.5	4.2		V	V_{CC} = 4.75 V, I_{OH} = 10 μA
V_{OL}	Output LOW Voltage		0.4	0.5	V	V_{CC} = 4.75 V, I_{OL} = 10 mA
			0.33	0.4	V	V_{CC} = 4.75 V, I_{OL} = 5.0 mA
V_{IH}	Input HIGH Voltage at CP Input (Note 3)		2.40		V	T_A = 75°C
			2.50		V	T_A = 25°C
			2.55		V	T_A = 0°C
V_{IL}	Input LOW Voltage at CP Input (Note 3)		1.60		V	T_A = 75°C
			1.70		V	T_A = 25°C
			1.75		V	T_A = 0°C
V_{IH}	Input HIGH Voltage at M Input (Note 3)	3.58		V_{CC}	V	V_{CC} = 5.0 V, T_A = 75°C
		3.40		V_{CC}	V	V_{CC} = 5.0 V, T_A = 25°C
		3.34		V_{CC}	V	V_{CC} = 5.0 V, T_A = 0°C
V_{IL}	Input LOW Voltage at M Input (Note 3)	GND		2.78	V	V_{CC} = 5.0 V, T_A = 75°C
		GND		2.60	V	V_{CC} = 5.0 V, T_A = 25°C
		GND		2.54	V	V_{CC} = 5.0 V, T_A = 0°C
I_{IH}	Input HIGH Current at M			250	μA	V_{IN} = 3.4 V, T_A = 25°C
I_{IL}	Input LOW Current at M	0.5			μA	V_{IN} = 2.6 V, T_A = 25°C
I_{OS}	Output Short-Circuit Current	1.6		2.9	mA	V_{CC} = 5.0 V, T_A = 25°C
I_{CC}	Power Supply Current		100	130	mA	V_{CC} = 5.0 V, T_A = 25°C
V_{CC}	Operating Supply Voltage	4.75	5.0	5.5	V	T_A = 0°C to +75°C

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification, a copy of which may be obtained from Fairchild ECL Product Marketing, Mountain View, Ca.
2. Typical values are at V_{CC} = 5.0 V and T_A = 25°C.
3. The M and CP input thresholds are referenced to V_{CC}, and vary directly with V_{CC}. For example, raising V_{CC} by 0.2 V also raises the thresholds by 0.2 V.

AC CHARACTERISTICS: T_A = 0°C to +75°C, Pins 1 and 14 = +5.0 V, Pin 7 = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
f_{COUNT}	Maximum Sinusoidal Input Frequency	950	1100		MHz	ac coupled input, 800 mV pk-pk
f_{COUNT}	Minimum Sinusoidal Input Frequency		50		MHz	Note 1
SR_{MIN}	Minimum Slew Rate, Squarewave Input		50		V/μs	Note 2

NOTES:
1. Input drive shall not exceed 1.2 V pk-pk.
2. Operation at very low frequency is possible, provided that sufficient slew rate of the input pulse edge is maintained.

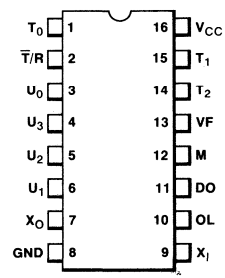
11C84
40-CHANNEL CB RADIO SYNTHESIZER
FAIRCHILD 11C00 SERIES

GENERAL DESCRIPTION – The 11C84 is a 16-pin LSI chip containing all the digital circuitry normally used in a digital Phase Locked Loop (PLL), including a programmable divide-by-N counter, a reference frequency divider chain, a phase/frequency comparator and a 10.24 MHz oscillator circuit. It accepts channel select inputs from BCD coded switches or the electronic equivalent. Also provided are an out-of-lock output signal and a 5 kHz offset control for single-sideband applications.

External circuitry required to complete a PLL are a voltage controlled oscillator (VCO), an active integrator and a 10.24 MHz crystal. The 11C84 is made with low power Schottky technology to achieve high frequency dividers. This eliminates any need for a prescaler or down-converter between the VCO output (16-17 MHz) and the divide-by-N counter input.

The 11C84 is designed for use in dual-conversion (10.695 MHz 1st IF, 455 kHz 2nd IF) receivers. The Transmit frequency is derived by mixing, rather than being generated directly by the VCO, thus avoiding the problem of feedback from the modulated RF power amplifier back into the VCO.

CONNECTION DIAGRAM
16-PIN DIP (TOP VIEW)

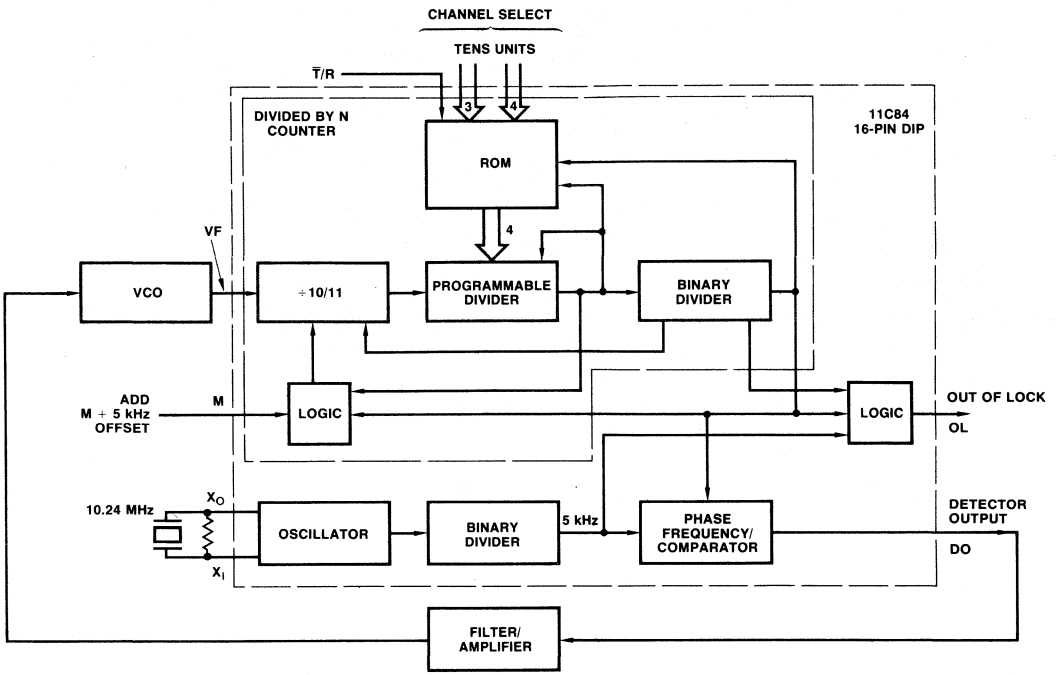


- **BCD CHANNEL SELECTION**
- **PULL-UP RESISTORS ON CHANNEL SELECT INPUTS**
- **WORKS WITH SINGLE OR DUAL CRYSTAL SYSTEMS**
- **PLL OUT-OF-LOCK OUTPUT AVAILABLE, TO INHIBIT TRANSMISSION**
- **DESIGNED FOR DUAL CONVERSION RECEIVERS**
- **LOW POWER SCHOTTKY TECHNOLOGY-OPERATES DIRECTLY AT VCO FREQUENCIES**
- **SELF-BIASED DIVIDER INPUT SIMPLIFIES CAPACITIVE COUPLING FROM VCO**
- **+5 kHz OFFSET CONTROL FOR SSB APPLICATIONS**
- **TRANSMIT FREQUENCY DERIVED BY MIXING – ELIMINATES FEEDBACK-INDUCED DISTORTION**
- **OPERATES FROM +5 V_{dc} SUPPLY**
- **16-PIN DIP PACKAGE**

PIN NAMES

DO	Phase/Frequency Detector Output
M	Mode Control, 5 kHz Offset (Increases VCO by 5 kHz)
OL	Out of Lock Signal, Open Collector (Conducts when PLL is in Out-of-Lock Condition)
T_0, T_1, T_2	Tens Digit BCD Inputs from Channel Select Switch
$\overline{T}/R$	Transmit/Receive Input (Active LOW Transmit)
U_0, U_1, U_2, U_3	Units Digit BCD Inputs from Channel Select Switch
V_F	Variable Frequency Input from VCO (AC Coupled Input)
V_{CC}	+5 V ± 5%
X_O	Crystal Connection (Output)
X_I	Crystal Connection (Input)

FUNCTIONAL BLOCK DIAGRAM



INPUT AND OUTPUT FUNCTIONS

There are seven Channel Select inputs intended for use with a 2-digit BCD switch or the electronic equivalent. The four inputs U_0-U_3 accept the units BCD numbers 0-9, while the three T_0-T_2 inputs accept the tens BCD numbers 0-7. Each of these seven inputs has a 20 kΩ pull-up resistor to V_{CC}, for use with a switch that provides contact closures to ground.

The Mode Control input M is provided for optional use in single sideband (SSB) applications. Grounding the M input increases the VCO frequency by 5 kHz in both Transmit and Receive modes, for SSB operation. For normal (non-SSB) operation, M should be left open; an internal pull-up resistor establishes a HIGH signal level when M is open.

Terminal VF is one input of a differential amplifier whose other input is connected to an internal reference voltage (Figure 1a). The VF input resistance is typically 8 kΩ and is biased in the active region to facilitate capacitive coupling from the VCO. It accepts either sinusoidal or rectangular waveshapes and responds to peak-to-peak amplitudes of 500 mV (Typ).

The Transmit/Receive ($\overline{T}$/R) input changes the divide ratio of the programmable divider, to coordinate with the 455 kHz change in VCO frequency when changing between the two modes. The $\overline{T}$/R input should be grounded for the Transmit mode and open for the Receive mode. The $\overline{T}$/R input contains a 20 kΩ pull-up resistor to establish the logic HIGH level in the open condition.

The 11C84 uses a 5 kHz comparison frequency, obtained by digitally dividing down from a 10.24 MHz reference frequency. The 10.24 MHz signal may be generated externally or internally. If the transceiver uses a separate 10.24 MHz oscillator, its output should be connected to terminal X_I of the 11C84 and can be capacitively coupled. A peak-to-peak amplitude of 500 mV (Typ) is sufficient. Th 10.24 MHz signal can be generated internally by connecting a crystal across terminals X_O and X_I, as shown in Figure 1b.

INPUT AND OUTPUT FUNCTIONS (Cont.)

The Channel Select, M and $\overline{T}$/R inputs, in addition to having pull-up resistors to V_{CC}, are low power Schottky TTL-type inputs, as shown in Figure 1c. The inverters connected to X_O and X_I are also of this type. The quiescent HIGH and LOW logic levels applied to the Channel Select, M and $\overline{T}$/R inputs should meet the same criteria specified for TTL logic; a HIGH signal should be 2.4 V or more, while a LOW signal should be 0.4 V or less. These values guarantee adequate noise margins. An input should not be driven more positive than +10 V.

The Detector Output (DO), as shown in Figure 1d, has three possible conditions: current sourcing, current sinking and high-impedance OFF state. When the loop is locked, DO is in the OFF state and generates no error signals to the integrator. When the variable frequency input to the phase/frequency comparator differs from the 5 kHz reference, the DO output is a series of current pulses with a 5 kHz repetition rate and a duration equal to the phase error. The DO output pulses are negative-going, i.e., current sinking, when the variable frequency lags the reference frequency and are positive-going when the variable frequency leads the reference frequency. These DO output pulse polarities insure the proper direction of varactor-bias change after inversion in the integrator. The phase/frequency comparator cannot give a false indication of lock when one input frequency is a multiple of the other. The comparator also has an anti-backlash feature that prevents it from operating in the "dead zone". For this reason, the charge-pump output will always exhibit a short negative-going pulse followed immediately by a short positive-going pulse. The duration and proximity of these opposing pulses cause no net change to the charge on the integrator.

The Out-of-Lock output is an open collector transistor (Figure 1e) which is turned off in the locked condition. The transistor is turned on whenever the negative going edges of the comparator input signals differ by $>\pm 200$ ns or more. The transistor will then stay on until such time as these negative edges occur within 200 ns of each other for at least two cycles of the 5 kHz reference frequency. The ± 200 ns tolerance allows for leakages associated with the integrator and ensures that the integrator only responds to true out-of-lock conditions. Typically, the OL output is used to suppress transmission and provide an indication of malfunction.

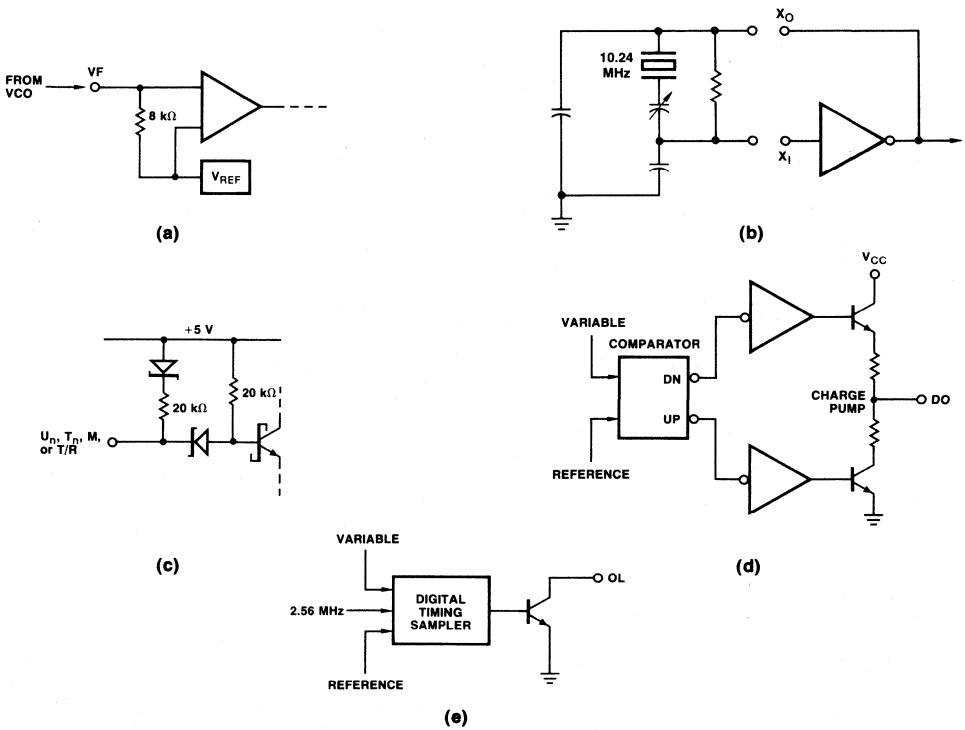


Fig. 1 INPUT AND OUTPUT CONFIGURATIONS

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE: −30 to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.7	V	Guaranteed Input LOW Voltage
V_{CD}	Input Clamp Diode Voltage		−0.88	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage, D_0	1.5	2.3	3.0	V	I_{OH} = −10 μA
V_{OH}	Output HIGH Voltage, X_I	2.4	3.6		V	V_{CC} = MIN, I_{OH} = −400 μA
V_{OL}	Output LOW Voltage, D_0		0.2	0.35	V	I_{OL} = 0, V_{CC} = MIN
V_{OL}	Output LOW Voltage, $\overline{OL}$, X1			0.5	V	I_{OL} = 4.0 mA, V_{CC} = MIN
I_{OH}	Output HIGH Current, $\overline{OL}$			0.2	mA	
I_{OZH}	Output OFF Current, D_0			1.0	μA	V_{CC} = MAX, V_{OUT} = 2.4 V
I_{OZL}	Output OFF Current, D_0			−1.0	μA	V_{CC} = MAX, V_{OUT} = 0.5 V
I_{IH}	Input HIGH Current		0.1	20	μA	V_{CC} = MAX, V_{IN} = 2.4 V
I_{BD}	Input HIGH Current		0.1	100	μA	V_{CC} = MAX, V_{IN} = 5.25 V
I_{IL}	Input LOW Current		0.38	1.0	mA	V_{CC} = MAX, V_{IN} = 0.5 V
R_{SINK}	Output Resistor	1.2	2.0	3.0	kΩ	
R_{SOURCE}	Output Resistor	0.6	0.9	1.5	kΩ	
I_{CC}	Supply Current		86	125	mA	V_{CC} = MAX

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
V_F	Clock Input Sensitivity	1.2	0.7	3.6	V	Peak-to-Peak, ac Coupled
R_{IN}	Clock Input Impedance, ac Coupled					
	a). Input Going HIGH	1.0		20	kΩ	At Input Amplitude of
	b). Input Going LOW	4.0		20	kΩ	1.0 V Peak-to-Peak
f_{IN}	Clock Input Frequency	18.0			MHz	

APPLICATIONS

SINGLE CRYSTAL SYSTEM (Figure 2)

The VCO frequency is injected into first mixer of the receiver and is 10.695 MHz (the first IF frequency) below the selected channel frequency. The 10.24 MHz crystal frequency is injected into the second mixer to obtain the 455 kHz second IF frequency. In the transmit mode, the VCO output is mixed with the 10.24 MHz to obtain the selected channel frequency.

In a single crystal system, the VCO must cover both the Receive and the Transmit tuning ranges, which are offset by 455 kHz. The total required tuning range is approximately 1.5 MHz. To achieve this broad range without incurring penalties in lock-up time when changing between Receive and Transmit modes, an extra varactor diode is effectively switched in or out, respectively. The bias voltage on the extra varactor is designed (or adjusted) so that the VCO control voltage does not change when switching between modes, thus reducing lock-up time.

DUAL CRYSTAL SYSTEM (Figure 3)

In the Receive mode, operation is the same as in the single crystal system. In the Transmit mode, a second crystal oscillator (10.695 MHz) is mixed with the VCO frequency to derive the selected channel frequency. This means that the VCO frequency is the same in either the Receive or the Transmit mode, for a given channel. Thus no band-switching is required; the tuning range need be only about 500 kHz and higher Q tuned circuits can be used to achieve a cleaner VCO design. Also, longer time constants can be used in the loop integrator, thus suppressing the 5 kHz (reference frequency) sideband components in the VCO output.

COST VS PERFORMANCE TRADE-OFF

Although the dual crystal approach requires, of course, a crystal and the associated oscillator components, there is actually very little difference in parts count because the single crystal system requires an extra varactor, potentiometer, switching transistor and auxiliary components. The disadvantages of increased complexity and lower performance of a band-switched VCO tends to dissipate the slight economic advantage of the single crystal system.

40 CHANNEL CB SYNTHESIZER

Figure 4 shows a synthesizer using the single crystal approach and a derived transmit frequency. This circuit was developed while the 11C84 was still in design, using MSI logic functions to simulate the 11C84. In this simulation it was found that digital noise from the programmable divider, feeding back into the VCO, caused spurious noise problems in the receiver. Buffer stage Q9 was incorporated to prevent this problem. Similarly, buffer stage Q6 isolates the 10.24 MHz oscillator from the reference frequency divider input. In using the 11C84, rather than its simulation, these buffer stages may or may not be required.

The primary objective of the design was to provide spectrally clean VCO and 10.24 MHz frequencies. To accomplish this, it was necessary to separate the grounds for the digital and analog portions of the circuit. Therefore, RF transformers are used between the oscillators and the buffers. Transformer coupling also makes it possible to physically separate and shield the 11C84 and buffers to reduce digital noise radiation. The remaining circuitry can, of course, be located on the main pc board of the tranceiver. Decoupling and grounding techniques are of the utmost importance.

TRANSMIT FREQUENCY GENERATION, DIRECT VS DERIVED

As in all system design, trade-offs must be made in the various performance characteristics. Since the 11C84 input circuitry and counters are designed to operate at frequencies up to 30 MHz, a system could be built in which the VCO operates directly at 27 MHz. But, it is very difficult to prevent feedback of the audio-modulated RF-transmitter output into the VCO which, in turn, causes spurious FM modulation of the VCO. For this reason, the 11C84 was programmed for a system using mixing techniques to derive the transmit frequency. That is, the VCO operates at approximately 17 MHz and is mixed with 10.24 MHz to obtain the 27 MHz transmit frequency. This generates a clean VCO signal, free of FM-modulation, but introduces sum and difference mixing products, called spurs, that require filtering.

One advantage of using mixing to derive the transmit frequency is that the VCO need change by only 455 kHz between Transmit and Receive; this can easily be accomplished by switching in an extra varactor diode. In a system where the transmit frequency is derived directly, the VCO must change by 10.24 MHz between Transmit and Receive thereby requiring complex inductive switching.

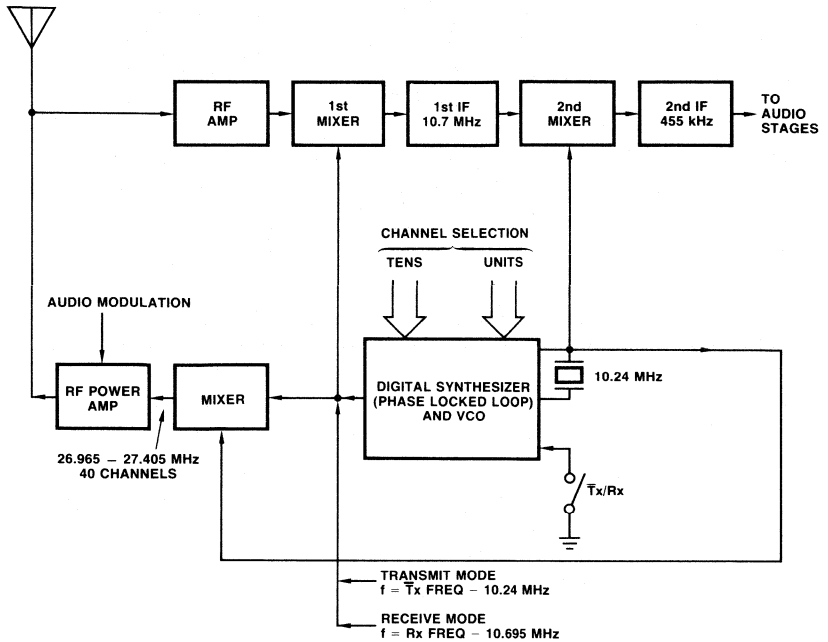


Fig. 2 SINGLE CRYSTAL CONTROL

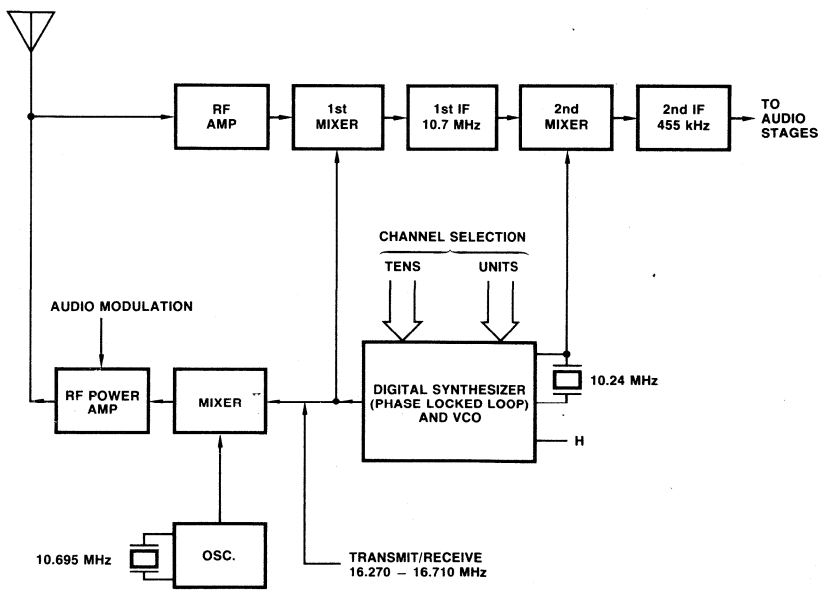


Fig. 3 DUAL CRYSTAL CONTROL

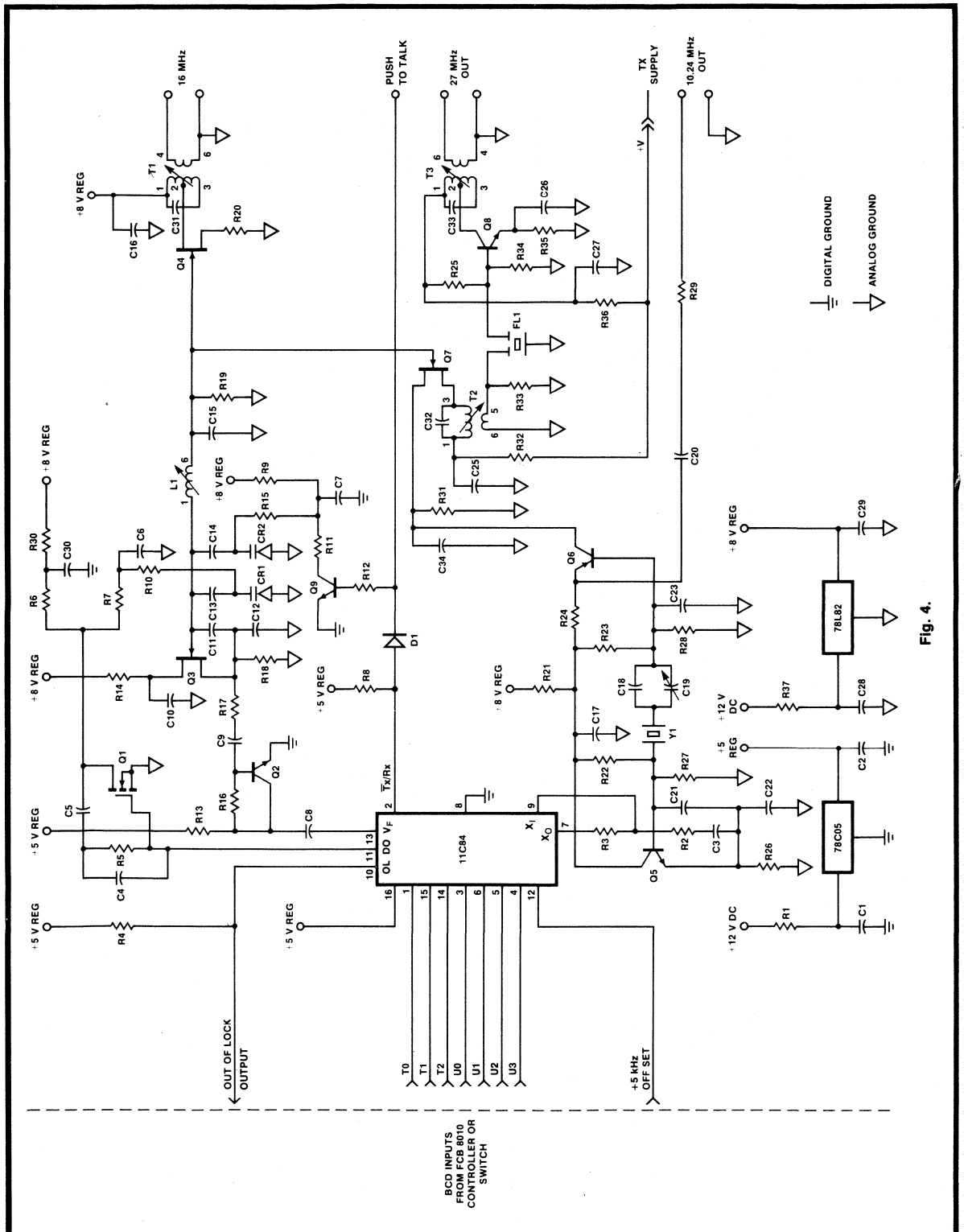

16 MHz
PUSH TO TALK
27 MHz OUT
TX SUPPLY
10.24 MHz OUT
DIGITAL GROUND
ANALOG GROUND
+8 V REG
+5 V REG
+12 V DC
11C84
78L82
78C05
OUT OF LOCK OUTPUT
BCD INPUTS FROM FCB 8010 CONTROLLER OR SWITCH
+5 kHz OFF SET

Fig. 4.

SYNTHESIZER FREQUENCIES – MHz

FCC ASSIGNED CHANNEL	FREQUENCY	VCO OUTPUT TRANSMIT	FREQUENCY RECEIVE	FCC ASSIGNED CHANNEL	FREQUENCY	VCO OUTPUT TRANSMIT	FREQUENCY RECEIVE
1	26.965	16.725	16.270	21	27.215	16.975	16.520
2	26.975	16.735	16.280	22	27.225	16.985	16.530
3	26.985	16.745	16.290	23	27.255	17.015	16.560
4	27.005	16.765	16.310	24	27.235	16.995	16.540
5	27.015	16.775	16.320	25	27.245	17.005	16.550
6	27.025	16.785	16.330	26	27.265	17.025	16.570
7	27.035	16.795	16.340	27	27.275	17.035	16.580
8	27.055	16.815	16.360	28	27.285	17.045	16.590
9	27.065	16.825	16.370	29	27.295	17.055	16.600
10	27.075	16.835	16.380	30	27.305	17.065	16.610
11	27.085	16.845	16.390	31	27.315	17.075	16.620
12	27.105	16.865	16.410	32	27.325	17.085	16.630
13	27.115	16.875	16.420	33	27.335	17.095	16.640
14	27.125	16.885	16.430	34	27.345	17.105	16.650
15	27.135	16.895	16.440	35	27.355	17.115	16.660
16	27.155	16.915	16.460	36	27.365	17.125	16.670
17	27.165	16.925	16.470	37	27.375	17.135	16.680
18	27.175	16.935	16.480	38	27.385	17.145	16.690
19	27.185	16.945	16.490	39	27.395	17.155	16.700
20	27.205	16.965	16.510	40	27405	17.165	16.710

11C84 ADDITIONAL CHANNELS FOR TESTING AND PROVIDING EXPANDED CHANNEL-9 SELECTION CAPABILITY

CHANNEL	FREQUENCY	VCO OUTPUT TRANSMIT	FREQUENCY RECEIVE	
0	26.915	16.675	16.220	VCO LOW RANGE TEST
41	26.995	16.755	16.300	
42	27.045	16.805	16.350	
43	27.095	16.855	16.400	
44	27.145	16.905	16.450	
45	27.195	16.955	16.500	
46	26.065	16.825	16.370	"CHANNEL 9" EMERGENCY
47	26.065	16.825	16.370	
48	26.065	16.825	16.370	
49	26.065	16.825	16.370	
50	27.415	17.175	16.720	VCO HIGH RANGE TEST
51	27.425	17.185	16.730	
52	27.435	17.195	16.740	
53	27.445	17.205	16.750	
54	27.455	17.215	16.760	
55	27.465	17.225	16.770	
56	27.475	17.235	16.780	
57	27.485	17.245	16.790	
58	27.495	17.255	16.800	
59	27.505	17.265	16.810	
60	26.065	16.825	16.370	"CHANNEL 9" EMERGENCY
↓	↓	↓	↓	
79	26.065	16.825	16.370	

9

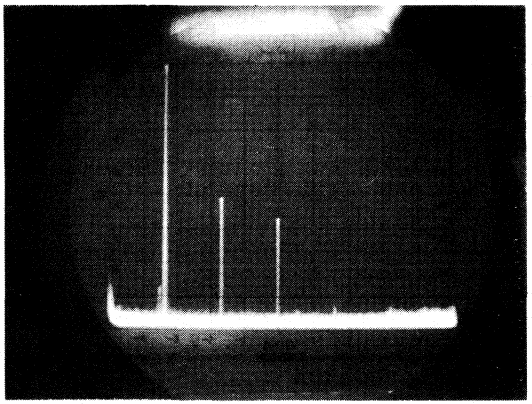
SWITCH ENCODING DATA

SWITCH POSITION	BCD CHANNEL CODES							7-SEGMENT CODES													
	Tens			Units				Display Tens							Display Units						
	T_2	T_1	T_0	U_3	U_2	U_1	U_0	A	B	C	D	E	F	G	A	B	C	D	E	F	G
Chan 1	X	X	X	X	X	X	O	X	X	X	X	X	X	O	O	X	X	O	O	O	O
2				X	X	O	X								X	X	O	X	X	O	X
3				X	X	O	O								X	X	X	X	O	O	X
4				X	O	X	X								O	X	X	O	O	X	X
5				X	O	X	O								X	O	X	X	O	X	X
6				X	O	O	X								X	O	X	X	X	X	X
7				X	O	O	O								X	X	X	O	O	O	O
8				O	X	X	X								X	X	X	X	X	X	X
9	X	X	X	O	X	X	O	X	X	X	X	X	X	O	X	X	X	O	O	X	X
10	X	X	O	X	X	X	X	O	X	X	O	O	O	O	X	X	X	X	X	X	O
11				X	X	X	O								O	X	X	O	O	O	O
12				X	X	O	X								X	X	O	X	X	O	X
13				X	X	O	O								X	X	X	X	O	O	X
14				X	O	X	X								O	X	X	O	O	X	X
15				X	O	X	O								X	O	X	X	O	X	X
16				X	O	O	X								X	O	X	X	X	X	X
17				X	O	O	O								X	X	X	O	O	O	O
18				O	X	X	X								X	X	X	X	X	X	X
19	X	X	O	O	X	X	O	O	X	X	O	O	O	O	X	X	X	O	O	X	X
20	X	O	X	X	X	X	X	X	X	O	X	X	O	X							
21				X	X	X	O														
22				X	X	O	X														
23				X	X	O	O														
24				X	O	X	X								Same						
25				X	O	X	O								as						
26				X	O	O	X								Channels 10-19						
27				X	O	O	O														
28				O	X	X	X														
29	X	O	X	O	X	X	O	X	X	O	X	X	O	X							
30	X	O	O	X	X	X	X	X	X	X	X	O	O	X							
31				X	X	X	O														
32				X	X	O	X														
33				X	X	O	O														
34				X	O	X	X								Same						
35				X	O	X	O								as						
36				X	O	O	X								Channels 10-19						
37				X	O	O	O														
38				O	X	X	X														
39	X	O	O	O	X	X	O	X	X	X	X	O	O	X							
40	O	X	X	X	X	X	X	O	X	X	O	O	X	X	X	X	X	X	X	X	O

X = CLOSURE
O = OPEN

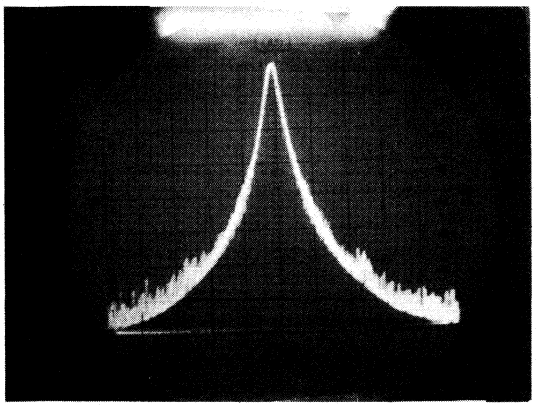
Note: Coding the same for both common-anode and common-cathode LED displays.

TRANSMIT VCO OUTPUT



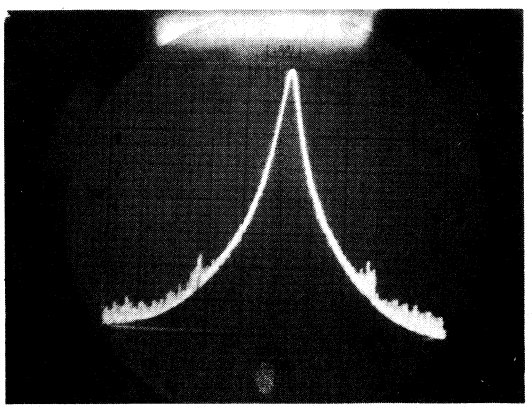
BANDWIDTH 30 kHz – SCAN 10 MHz/DIV

TRANSMIT VCO OUTPUT



BANDWIDTH 50 Hz – SCAN 200 Hz/DIV

TRANSMITTER OUTPUT



BANDWIDTH 50 Hz – SCAN 200 Hz/DIV
FINAL OUTPUT TO ANTENNA

Fig. 5 SPECTRAL OUTPUT

PART LIST
40 CHANNEL CB RADIO SYNTHESIZER USING THE 11C84

PART TYPE		CIRCUIT #
DIGITAL		
11C84	Phase Lock Loop Frequency Synthesizer	ICI
LINEAR IC		
78C05	500 mA Regulator	Q11
78L82	100 mA Regulator	Q10
DISCRETE DEVICES		
PN3643	G.P. NPN Transistors	Q2, Q9, Q5, Q8
PN3644	G.P. PNP Transistors	Q6
2N5485	Field Effect Transistor (Siliconix)	Q3, Q4, Q7
SD212	DMOS N-Channel Enhancement FET Switch	Q1
MV2209	Varactor Diode (Motorola)	CR1
1N4148	Signal Diode	D1
PASSIVE COMPONENTS		
Crystal	10.24 MHz – .001% tolerance Load Capacitance = 32 pF Jan Crystals Div. of Bob Whan & Son Electronics Inc. 2400 Crystal Drive Fort Myers, Florida 33901	Y1
Inductor	Toko-America PRI = 1.6 μH Center, Q = 80, 36 gauge wire	T1 – T3
Inductor	Toko-America .45–1.2 μH, Q = 80, 36 gauge wire	L1
Filter	Murata SFE 27 mA	FL1
PC BOARD		
Fairchild	LSI Synthesizer Board	03177
SWITCHES		
Digitran	37015	S1
OAK	814004-746	
Standard Grigsby Inc.		
CBXP-0075-40		
AMP	76-17323	
FSC	FCB8010	

40 CHANNEL SYNTHESIZER WITH TX MIXER

*R1, R37	15 Ω
R2, R17, R14, R36, R21, R32, R35	220 Ω
R3, R25	3.3 kΩ
R4, R8, R13, R18, R19, R31, R33	1.0 kΩ
R5, R12, R23	10 kΩ
R7, R6	5.6 kΩ
R9	8.2 kΩ
R24	200 Ω
R16, R10, R15	100 kΩ
R11	7.5 kΩ
R26	2.2 kΩ
R22	36 kΩ
R27	27 kΩ
R34, R20, R30, R29	330 Ω
R38, R50	820 Ω
R28	56 kΩ

TOTAL 35

*½ Watt
Others, ¼ Watt

MASTER LIST

*C1, C2, C28, C29	0.33 μF
*C3, C6, C7, C8, C10, C16, C17, C20, C24, C25, C26, C27, C30	0.1 μF
*C5	1.0 μF
*C4	0.047 μF
C9	10 pF
C11 Sub (130 pF)	120 pF
C12	150 pF
C13, C14, C22, C23	330 pF
C15	680 pF
C31	62 pF
C32, C33	22 pF
C18	15 pF
*C19	7-25 pF Trimmer
C21	250 pF
C34	68-75 pF

TOTAL 34

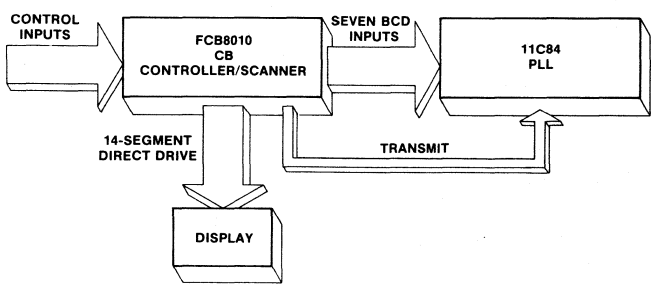
*Ceramic
All others, dipped Mica

CONTROLLER/SCANNER

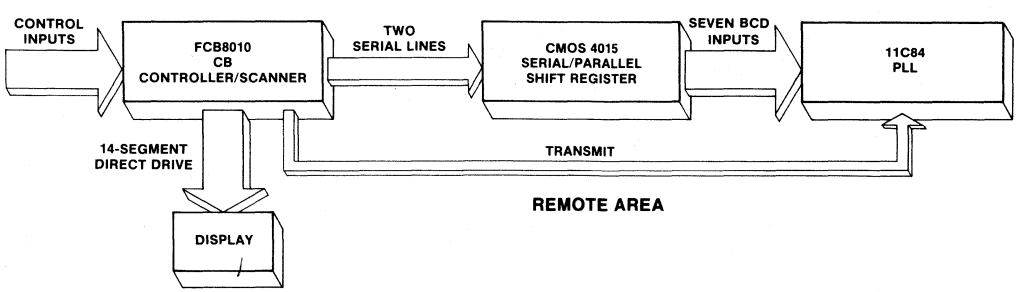
A new controller/scanner IC, the FCB8010, has recently been developed to provide channel information to the PLL circuit, to drive the LED display,and to provide a variety of extra features.

- **Up/down operation at two speeds**
- **Search mode for busy or vacant channels**
- **Scan mode for locating busy channels**
- **Automatic Scan 9 while using priority channel**
- **Emergency 9 for immediate channel-9 access**
- **Stores any five channels**
- **Recalls stored channels**
- **Serial and parallel outputs for synthesizer channel selection**
- **Brightness control for LED display**
- **Single-side-band selection**

Build a remote system with the CB tucked safely in the trunk or other secure spot and only the mike, containing the FCB8010 controller/scanner and the display, attached to the dashboard. The hand-held push button unit is now as convenient to use as a walkie-talkie, and can be removed to prevent theft. Too many wires! Use the controller's serial output to reduce the wires from seven to two! Use parallel operation to build one compact dashboard unit using only the FCB8010 controller/scanner, the 11C84 frequency synthesizer and a display



Parallel Operation



Serial Operation

9

11C90/11C91

650 MHz PRESCALERS

11C00 SERIES

GENERAL DESCRIPTION — The 11C90 and 11C91 are high speed prescalers designed specifically for communication and instrumentation applications. All discussions and examples in this data sheet are applicable to the 11C91 as well as the 11C90.

The 11C90 will divide by 10 or 11 and the 11C91 divides by 5 or 6, both over a frequency range from dc to typically 650 MHz. The division ratio is controlled by the mode control. The divide by 10 or 11 capability allows the use of pulse swallowing techniques to control high speed counting modulos by lower speed circuits. The 11C90 may be used with either ECL or TTL power supplies.

In addition to the ECL outputs Q_4 and $\overline{Q}_4$, the 11C90 contains an ECL-to-TTL converter and a TTL output. The TTL output operates from the same V_{CC} and V_{EE} levels as the counter, but a separate pin is used for the TTL circuit V_{EE}. This minimizes noise coupling when the TTL output switches and also allows power consumption to be reduced by leaving the separate V_{EE} pin open if the TTL output is not used.

To facilitate capacitive coupling of the clock signal, a 400 Ω resistor (V_{REF}) is connected internally to the V_{BB} reference. Connecting this resistor to the Clock Pulse input (CP) automatically centers the input about the switching threshold. Maximum frequency operation is achieved with a 50% duty cycle.

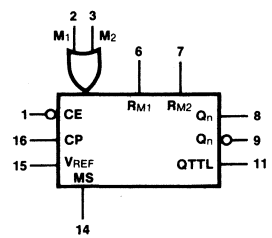
Each of the Mode Control inputs is connected to an internal 2 k resistor with the other end uncommitted (RM_1 and RM_2). An M input can be driven from a TTL circuit operating from the same V_{CC} by connecting the free end of the associated 2 k resistor to V_{CCA}. When an M input is driven from the ECL circuit, the 2 k resistor can be left open or, if required, can be connected to V_{EE} to act as a pull-down resistor.

- **VERY HIGH SPEED – 650 MHz TYPICAL**
- **DIVIDE BY 10/11 OR 5/6 MODE CONTROL**
- **OPERATES FROM TTL OR ECL POWER SUPPLY**
- **HIGH SPEED TOTEM POLE TTL OUTPUT – 20 mA FAN-OUT**
- **COMPLEMENTARY ECL OUTPUTS DRIVE 50 Ω LINES**
- **SEPARATE TTL GND (V_{EE}) PIN MINIMIZES NOISE COUPLING**
- **PULL-UP RESISTORS ON MODE CONTROL INPUTS FOR TTL COMPATIBILITY**
- **INTERNAL BIASING REFERENCE FOR AC COUPLED CLOCKING**
- **INTERNAL 50 kΩ INPUT PULL-DOWNS – UNUSED INPUTS MAY BE LEFT OPEN**
- **COUNT ENABLE CONTROL FOR GATED CLOCKING**
- **ASYNCHRONOUS MASTER SET FOR INITIALIZING**

PIN NAMES

$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input
M_n	Count Modulus Control Input
MS	Asynchronous Master Set Input
Q_n, $\overline{Q}_n$	Complementary ECL Outputs
QTTL	TTL Output
RM_n	2 k Resistor to M_n
V_{REF}	400 Ω Resistor to V_{BB}

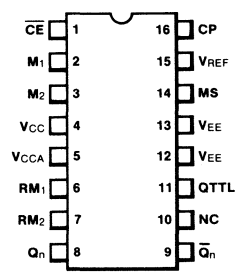
LOGIC SYMBOL



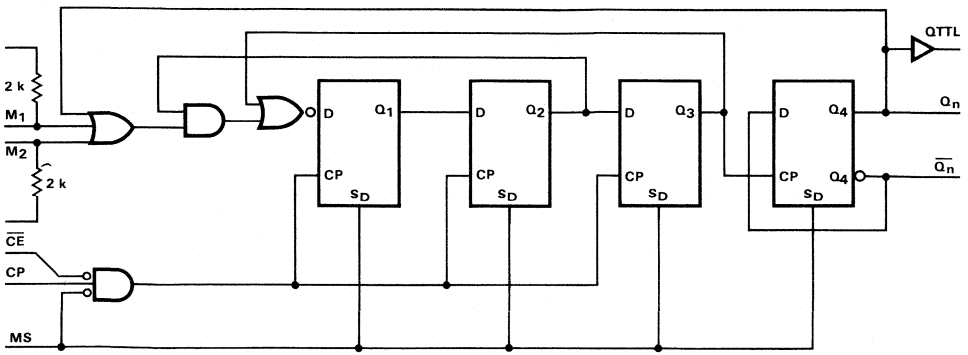
11C90, Q_n = Pin 4
11C91, Q_n = Pin 3

V_{CC} = Pin 4
V_{CCA} = Pin 5
V_{EE} = Pin 12
V_{EE} (TTL) = Pin 13

CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM 11C90



NOTE: This diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than shown.

COUNT SEQUENCE TABLE 11C90

	Q_1	Q_2	Q_3	Q_4(QTTL)	
	H	H	H	H	÷ 11
÷ 10	L	H	H	H	
	L	L	H	H	
	L	L	L	H	
	H	L	L	H	
	H	H	L	H	
	L	H	H	L	
	L	L	H	L	
	L	L	L	L	
	H	L	L	L	
	H	H	L	L	

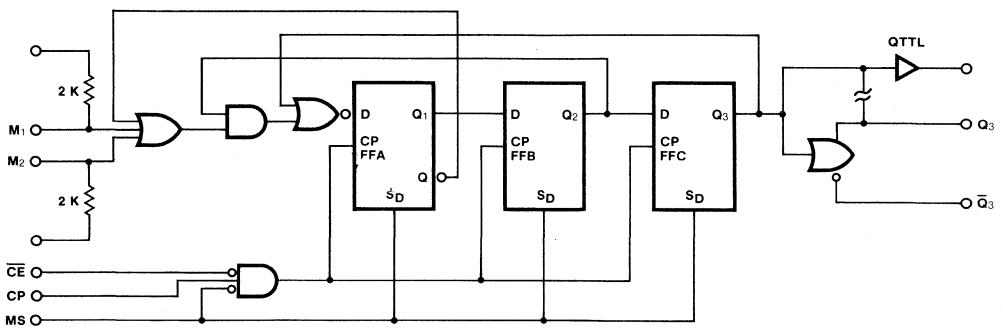
Note: A HIGH on MS forces all Qs HIGH.

OPERATING MODE TABLE 11C90

INPUTS				OUTPUT RESPONSE
MS	$\overline{CE}$	M_1	M_2	
H	X	X	X	Set HIGH
L	H	X	X	Hold
L	L	L	L	÷ 11
L	L	H	X	÷ 10
L	L	X	H	÷ 10

X = Don't Care

LOGIC DIAGRAM 11C91



COUNT SEQUENCE TABLE 11C91

	Q_1	Q_2	Q_3(QTTL)	
	H	H	H	÷ 6
÷ 5	L	H	H	
	L	L	H	
	L	L	L	
	H	L	L	
	H	H	L	

Note: A HIGH on MS forces all Q_s HIGH.

OPERATING MODE TABLE 11C91

INPUTS				OUTPUT RESPONSE
MS	$\overline{CE}$	M_1	M_2	
H	X	X	X	SET HIGH
L	H	X	X	Hold
L	L	L	L	÷6
L	L	X	H	÷5
L	L	H	X	÷5

X = Don't Care

FUNCTIONAL DESCRIPTION — The 11C90 contains four ECL flip-flops, and ECL to TTL converter and a Schottky TTL output buffer with an active pull-up. Three of the flip-flops operate as a synchronous shift counter driving the fourth flip-flop operating as an asynchronous toggle. The internal feedback logic is such that the TTL output and the Q_4 ECL output are HIGH for six clock periods and LOW for five clock periods. The Mode Control (M) inputs can modify the feedback to make the output HIGH for five clock periods and LOW for five clock periods, as indicated in the Count Sequence Table.

The feedback logic is such that the instant the output goes HIGH, the circuit is already committed as to whether the output period will be 10 or 11 clock periods long. This means that subsequent changes in an M input signal, including decoding spikes, will have no effect on the current output period. The only timing restriction for an M input signal is that it be in the desired state at least a set-up time before the clock that follows the HHLL state shown in the table. The allowable propagation delay through external logic to an M input is maximized by designing it to use the positive transition of the 11C90 output as its active edge. This gives an allowable delay of ten clock periods, minus the CP to Q delay of the 11C90 and the M to CP set-up time. If the external logic uses the negative output transition as its active edge, the allowable delay is reduced to five clock periods minus the aforementioned delay and set-up time.

Capacitivley coupled triggering is simplified by the 400 Ω resistor which connects pin 15 to the internal V_{BB} reference. By connecting this to the CP input, as shown in *Figure a*, the clock is automatically centered about the input threshold. A clock duty cycle of 50% provides the fastest operation, since the flip-flops are master/slave types with offset clock thresholds between master and slave. This feature ensures that the circuit will operate with clock waveforms having very slow rise and fall times, and thus, there is no minimum frequency restriction. Recommended minimum and maximum clock amplitude as a function of a frequency and temperature are shown in the graph labeled *Figure e*. When the CP or any other input is driven from another ECL circuit, normal ECL termination methods are recommended. One method is indicated in *Figure b*. Other ECL termination methods are discussed in this Handbook.

When an M input is to be driven from a TTL output operating from the same V_{CC} and ground (V_{EE}), the internal 2 k resistor can be used to pull the TTL output up as shown in *Figure c*. Some types of TTL outputs will only pull up to within two diode drops of V_{CC}, which is not high enough for 11C90 inputs. The resistor will pull the signal up through the threshold region, although this final rise may be somewhat slow, depending on wiring capacitance. A resistor network that gives faster rise and also lower impedance is shown in *Figure d*.

The ECL outputs have no pull-down resistors and can drive series or parallel terminated transmission lines. For short interconnections that do not require impedance matching, a 270 Ω to 510 Ω resistor to V_{EE} can be used to establish the V_{OL} level. Both V_{CC} pins must always be used and should be connected together as close to the package as possible. Pin 12 must always be connected to the V_{EE} side of the supply, while pin 13 is required only if the TTL output is used. Low impedance V_{CC} and V_{EE} distribution and rf bypass capacitors are recommended to prevent crosstalk with other circuits.

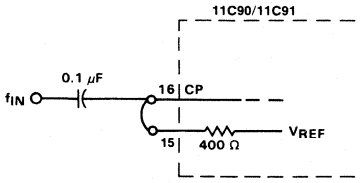
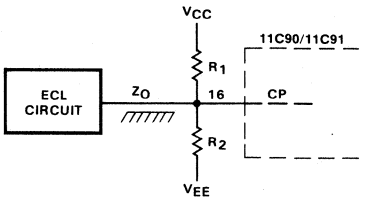


Fig. a Capacitively Coupled Clocking



Z_O Ω	50	75	100
R_1 Ω	81	122	163
R_2 Ω	130	195	260

Fig. b Clocking by ECL Source via Terminated Line

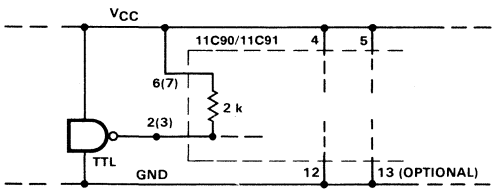


Fig. c Using Internal Pull-up with TTL Source

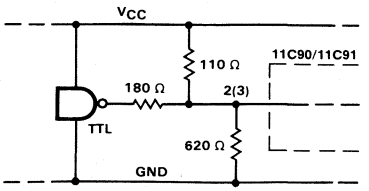


Fig. d Faster Low Impedance TTL to ECL Interface

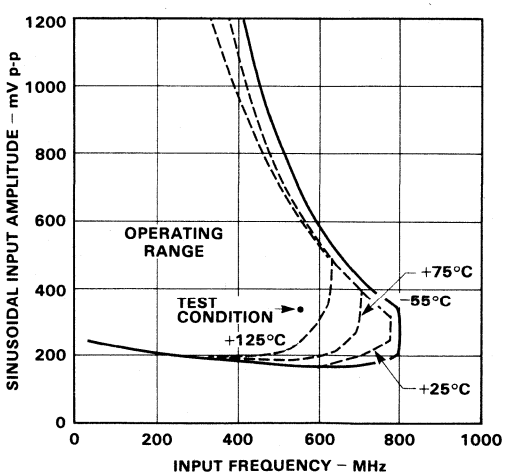


Fig. e AC Coupled Triggering Characteristics

TTL INPUT/OUTPUT OPERATION

DC CHARACTERISTICS: Over Operating Temperature and Voltage Range unless otherwise noted. Pins 12 and 13 = GND.

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP (Note 4)	LIMITS A	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage M_1 and M_2 Inputs		4.1		V	Guaranteed Input HIGH Threshold Voltage (Note 5), $V_{CC} = V_{CCA} = 5.0$ V
V_{IL}	Input LOW Voltage M_1 and M_2 Inputs		3.3		V	Guaranteed Input LOW Threshold Voltage (Note 5), $V_{CC} = V_{CCA} = 5.0$ V
V_{OH}	Output HIGH Voltage QTTL Output	2.3	3.3		V	$V_{CC} = V_{CCA} =$ MIN, $I_{OH} = -640\ \mu A$
V_{OL}	Output LOW Voltage QTTL Output		0.2	0.5	V	$V_{CC} = V_{CCA} =$ MIN, $I_{OL} = 20.0$ mA
I_{IL}	Input LOW Current M_1 and M_2 Inputs		−2.3	−5.0	mA	$V_{CC} = V_{CCA} =$ MAX, $V_{IN} = 0.4$ V Pins 6, 7 = V_{CC}
I_{SC}	Output Short Circuit Current	−20	−35	−80	mA	$V_{CC} = V_{CCA} =$ MAX, $V_{OUT} = 0.0$ V Pin 14 = V_{CC}

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, CA.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at $V_{CC} = 5.0$ V and $T_A = 25°C$.
5. The M_1 and M_2 threshold specifications are normally referenced to the V_{CC} potential, as shown in the ECL operation tables. Using V_{EE} (gnd) as the reference, as in normal TTL practice, effectively makes the threshold vary directly with V_{CC}. Threshold is typically 1.3 V below V_{CC} (*e.g.*, +3.7 V at $V_{CC} = +5$ V). A signal swing about threshold of ±0.4 V is adequate, which gives the stated V_{IH} and V_{IL} values. The internal 2 k resistors are intended to pull TTL outputs up to the required V_{IH} range, as discussed in the FUNCTIONAL DESCRIPTION and shown in *Figure c*.

TTL OPERATION

AC CHARACTERISTICS: $V_{CC} = V_{CCA} = 5.0$ V Nominal, $V_{EE} =$ GND, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, (50% − 50%) CP to QTTL	6	10	14	ns	See Figure f
t_{PLH}	Propagation Delay, (50% − 50%) MS to QTTL		12	17	ns	
t_s	Mode Control Set-up Time	4	2		ns	
t_h	Mode Control Hold Time	0	−2		ns	
t_{TLH}	Output Rise Time (20% to 80%)		10		ns	
t_{THL}	Output Fall Time (20% to 80%)		2		ns	
f_{MAX}	Count Frequency	550 600	650 650		MHz	−55°C to +125°C 0°C to +75°C Clock Input ac Coupled 350 mV peak-to-peak sine wave, Note 6

NOTE 6: TTL Output Signal swing is guaranteed at f_{MAX} over temperature range.

ECL OPERATION – INDUSTRIAL RANGE

DC CHARACTERISTICS: $V_{CC} = V_{CCA} = GND$, $V_{EE} = -5.2$ V

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
V_{OH}	Output HIGH Voltage Q_4 and $\overline{Q}_4$	−1060 −1025 −980	−995 −960 −910	−905 −880 −805	mV	0°C 25°C 75°C	Load = 50 Ω to −2 V
V_{OL}	Output LOW Voltage Q_4 and $\overline{Q}_4$	−1820	−1705	−1620	mV	0°C to 75°C	
V_{IH}	Input HIGH Voltage	−1135 −1095 −1035		−840 −810 −720	mV	0°C 25°C 75°C	Guaranteed Input HIGH Signal See Note 7
V_{IL}	Input LOW Voltage	−1870 −1850 −1830		−1500 −1485 −1460	mV	0°C 25°C 75°C	Guaranteed Input LOW Signal
I_{IH}	Input HIGH Current CP Input MS Input M_1 and M_2 Input			 400 400 250	 μA	 25°C 25°C 25°C	$V_{IN} = V_{IHA}$
I_{IL}	Input LOW Current	0.5			μA	25°C	$V_{IN} = V_{ILB}$
I_{EE}	Power Supply Current	−110 −119	−75		mA	0°C to 75°C	Pins 6,7,13 not connected
V_{EE}	Operating Supply Voltage Range	−5.7	−5.2	−4.7	V	0°C to 75°C	

ECL OPERATION – INDUSTRIAL RANGE

AC CHARACTERISTICS: $T_A = 0°C$ to +75°C, $V_{CC} = V_{CCA} = GND$, $V_{EE} = -5.2$ V

SYMBOL	CHARACTERISTIC	LIMITS 0°C TYP	LIMITS +25°C MIN	LIMITS +25°C TYP	LIMITS +25°C MAX	LIMITS +75°C TYP	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, (50%-50%) CP to Q4	1.8	1.3	2.0	3.0	2.5	ns	
t_{PLH}	Propagation Delay, (50%-50%) MS to Q4	3.7		4.0	6.0	4.5	ns	Output:
t_s	Set-up Time, M to CP	2.0	4.0	2.0		2.0	ns	R_L = 50 Ω to −2.0 V
t_h	Hold Time, M to CP	−2.0	0.0	−2.0		−2.0	ns	Input:
t_{TLH}	Output Rise Time (20%-80%)	1.0		1.0	2.0	1.0	ns	$t_{ri} = t_{fi} = 2.0 \pm 0.1$ ns (20%-80%)
t_{THL}	Output Fall Time (80%-20%)	1.0		1.0	2.0	1.0	ns	See Figure f.
f_{MAX}	Maximum Clock Frequency	650	600	650		625	MHz	AC coupled input 350 mV peak-to-peak. f_{MAX} is guaranteed to be 575 MHz min at 0°C to 75°C.

ECL OPERATION – MILITARY RANGE

DC CHARACTERISTICS: $V_{CC} = V_{CCA} = GND$, $V_{EE} = -5.2$ V

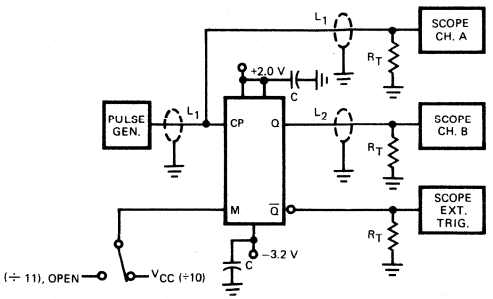
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
V_{OH}	Output HIGH Voltage Q_4 and $\overline{Q}_4$	−1100 −980 −910	−1030 −910 −820	−900 −820 −670	mV	−55°C +25°C +125°C	Load = 100 Ω to −2 V
V_{OL}	Output LOW Voltage Q_4 and $\overline{Q}_4$	−1820	−1705	−1620	mV	−55°C to +125°C	
V_{IH}	Input HIGH Voltage	−1190 −1095 −975		−905 −810 −690	mV	−55°C +25°C +125°C	Guaranteed Input HIGH Signal. See Note 7
V_{IL}	Input LOW Voltage	−1890 −1850 −1800		−1525 −1485 −1435	mV	−55°C +25°C +125°C	Guaranteed Input LOW Signal.
I_{IH}	Input HIGH Current CP Input MS Input M_1 and M_2 Input			 400 400 250	 μA	 +25°C +25°C +25°C	$V_{IN} = V_{IHA}$
I_{IL}	Input LOW Current	0.5			μA	+25°C	$V_{IN} = V_{ILB}$
I_{EE}	Power Supply Current	−110 	−75 −119		mA	+25°C −55°C to +125°C	Pins 6,7,13 not connected
V_{EE}	Operating Supply Voltage Range	−5.7	−5.2	−4.7	V	−55°C to +125°C	

NOTE 7: M_1 or M_2 can be tied to V_{CC} for fixed divide-by-ten operation.

ECL OPERATION – MILITARY RANGE

AC CHARACTERISTICS: $T_A = -55°C$ to $+125°C$, $V_{CC} = V_{CCA} = GND$, $V_{EE} = -5.2$ V

SYMBOL	CHARACTERISTIC	LIMITS −55°C TYP	LIMITS +25°C MIN	LIMITS +25°C TYP	LIMITS +25°C MAX	LIMITS +125°C TYP	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, (50%-50%) CP to Q4	1.5	1.3	2.0	3.0	3.0	ns	Output:
t_{PLH}	Propagation Delay, (50%-50%) MS to Q4	3.5		4.0	6.0	5.0	ns	R_L = 100 Ω to −2.0 V
t_s	Set-up Time M to CP	2.0	4.0	2.0		2.0	ns	Input:
t_h	Hold Time, M to CP	−2.0	0.0	−2.0		−2.0	ns	$t_{ri} = t_{fi} = 2.0 \pm 0.1$ ns (20%-80%)
t_{TLH}	Output Rise Time (20%-80%)	1.0		1.0	2.0	1.0	ns	
t_{THL}	Output Fall Time (80%-20%)	1.0		1.0	2.0	1.0	ns	See Figure f.
f_{MAX}	Maximum Count Frequency	700	600	650		600	MHz	AC coupled input 350 mV peak-to-peak. f_{MAX} is guaranteed to be 550 MHz min at −55°C to 125°C.



CONDITIONS

V_{CC} = +2.0 V

V_{EE} = −3.2 V

R_T = 50 Ω (Scope input impedance)

C_L = Jig and stray capacitance < 5.0 pF

L_1 = L_2 equal 50 Ω impedance lines

C = 0.1 pF

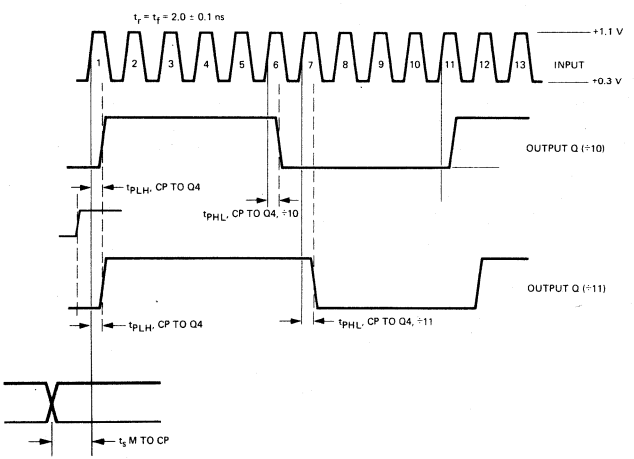


Fig. f

NOTES:

1. Use high impedance probes to test QTTL.
   Connect pin 13 to V_{EE}.
2. For high frequency test use ac coupled input as in *Figure a*.
   Adjust input amplitude to 350 mV p-p.

MAKING PROGRAMMABLE UHF COUNTERS WHEN NONE ARE AVAILABLE OR . . . PULSE SWALLOWING REVISITED

(Reprinted from *Fairchild Journal of Semiconductor Progress*, Vol 3, No. 4)

Recent developments have aroused greater interest in VHF and UHF counters for applications such as mobile communications and digitally tuned FM and TV receivers. Along with such new applications, of course, comes the need for suitable test instruments and signal generators. Although these applications differ in many ways, they have one thing in common —the need for high speed programmable counters. However, it seems inevitable that for some applications the available programmable counters are not fast enough; or, the counters that are fast enough lack the programming capability. One way of getting around this dilemma is to combine the talents of a high speed counter with those of a programmable counter. *Figure 1* shows such a combination, with a UHF prescaler and a programmable counter (the "units" decade) cooperating in a pulse swallowing* scheme to simulate a programmable UHF decade.

Pulse swallowing has been described as a way of combining a counter that is very fast, but rather dumb, with a counter that is very smart, but rather slow, to make the rest of the logic think that there is a very fast, very smart counter up front. For purposes of discussion, a smart counter is defined as one that is fully programmable and directly or indirectly satisfies a few other requirements. Examples are the 10010/16 and 95010/16 ECL circuits and the 93S10/16 TTL elements illustrated in *Figure 2*. Each circuit has a Terminal Count (TC) output which is normally in the inactive state and goes to the active state (LOW for ECL, HIGH for TTL) when the circuit reaches its maximum count, and stays active as long as the circuit retains the maximum count. Each circuit has an active-LOW Parallel Enable ($\overline{PE}$) input and individual Preset data (P_n) inputs for the four flip-flops. A LOW signal on $\overline{PE}$ inhibits counting and enables synchronous presetting. A Count Enable ($\overline{CE}$) input can prevent counting but cannot prevent presetting. Thus the synchronous operating modes of these circuits are Count Up, Hold and Preset, all of which are utilized in either a straightforward programmable counter or in a pulse swallowing counter. The built-in flexibility of these circuits is at the expense of speed, due to the auxiliary gating, the full synchronism, and the time required to do the housekeeping.

Figure 3 illustrates a conventional divider using the fully programmable circuits. The TC output of the first decade is designated f_2 and gates the f_1 pulses into the second stage. The TC of the second stage is the final output f_3 and also the $\overline{PE}$ signal for both stages. Following a Preset, the first stage produces an f_2 pulse (one f_1 period wide) after the first K pulses of f_1 and thereafter produces one f_2 pulse for every 10 f_1 pulses. The second stage, which could as easily be two or more decades, produces an output pulse for every 10 pulses of f_2. Treated as a system building block, the overall divide ratio N can be expressed as follows.

$$N = K + 10(M) \quad (1)$$

For changing the overall divide ratio, K can be considered a fine adjustment and M a course adjustment; therefore, the change in N due to changes in K and M is

$$\Delta N = \Delta K + 10(\Delta M) \quad (2)$$

The fixed ratio counter or prescaler is at the high end of the speed scale, but at the low end of the intelligence scale. *Figure 4* illustrates a fixed prescaler driving a programmable counter. The fixed prescaler takes away some of the flexibility in choosing the overall divide ratio N and in the fine adjustment of N, as shown in *Equations 3* and *4*.

$$N = P \cdot M \quad (3)$$

$$\Delta P = 0$$

$$\therefore \Delta N = P(\Delta M) \quad (4)$$

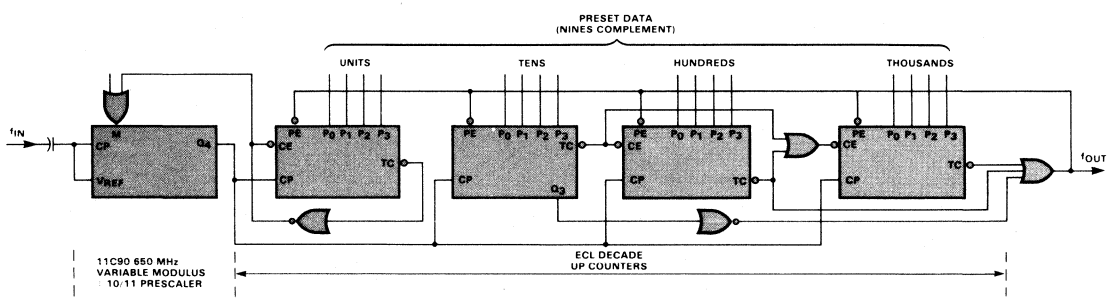


Fig. 1 650 MHz Programmable Pulse Swallowing Counter

*Nichols, J. and Shinn, C., "Pulse Swallowing", EDN, October 1, 1970.

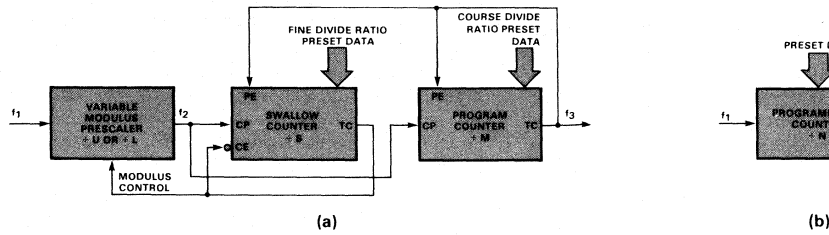


Fig. 7 Pulse Swallowing Counter and Equivalent System Building Block

The divide ratios are summarized as follows:

U = upper (larger) divide ratio of the prescaler
L = lower divide ratio of the prescaler
S = divide ratio of the swallow counter
= number of times the prescaler divides by U in a complete program cycle
M = divide ratio of the program counter
= total number of prescaler cycles in a complete program cycle

From these definitions, the number of times the prescaler divides by its lower ratio in one program cycle can be determined.

M-S = number of times the prescaler divides by L in a complete program cycle

The number of f_1 pulses that occur in each of the prescaler modes during a complete program cycle can be stated as follows:

U•S = number of f_1 pulses into the prescaler during its upper mode

L(M-S) = number of f_1 pulses into the prescaler during its lower mode

U•S + L(M-S) = total number of f_1 pulses into the prescaler during a complete program cycle

Figure 7b shows the pulse swallowing programmable counter as a single functional block, and the overall divide ratio N can be stated from the above definitions.

$$N = f_1 / f_3 = U \cdot S + L(M-S) \quad (5)$$

Alternatively:

$$N = (U-L)S + LM \quad (6)$$

In *Figure 7a*, the preset data inputs suggest that S and M are fine and course program controls respectively. The effect of changing S can be determined by letting S increase by one and the subtracting *Equation 6*.

$$N' = (U-L)(S+1) + LM$$
$$= (U-L)S + LM + (U-L)$$
$$\Delta N = N' - N = U-L$$

And in the general case:

$$\Delta N = (U-L)(\Delta S) \quad (7)$$

Equation 7 offers some insight into why the most popular variable modulus prescalers have divide ratios such as 10/11 and 5/6. U and L differ only by one and changing S by a certain amount changes N by the same amount. Thus the combination of the prescaler and the swallow counter acts like a single, very fast, fully programmable divider. A similar analysis with M as the variable shows that the smallest adjustment afforded by the program counter is L.

$$N' = (U-L)S + L(M+1)$$
$$= (U-L)S + LM + L$$
$$\Delta N = N' - N = L$$

And in the general case:

$$\Delta N = L(\Delta M) \quad (8)$$

Combining *Equations 7* and *8* gives an expression for the effects of changing either or both S and M.

$$\Delta N = (U-L)(\Delta S) + L(\Delta M) \quad (9)$$

Notice that if U is 11 and L is 10, *Equation 9* is the same as *Equation 2* and *Equation 6* is the same as *Equation 1*, since the swallow counter of *Figure 7* and the first stage of *Figure 3* are the same type of circuit; thus S and K have the same meaning. Using 10 for L also means that the program counter can be made up of cascaded decade counters, with each decade corresponding to a decimal digit of the total divide ratio N. This is best shown by a numerical example.

To get N = 4367
with U = 11
and L = 10,
make S = 7
and M = 436

As a check, substitute these values into *Equation 5*.

$$N = U \cdot S + L(M-S)$$
$$= (11)\,7 + 10\,(436-7) = 77 + 4290$$
$$= 4367.$$

Thus, the pulse swallowing counter is programmed in the same way as the divider of *Figure 3*. A practical limitation on the pulse swallowing technique is that M cannot be less than S; otherwise the program counter would reach maximum count before the swallow counter, and the latter would not have a chance to change the divide ratio of the prescaler before being preset. The prescaler would then operate the same as the fixed prescaler of *Figure 4*. Thus with decade programming, the practical minimum divide ratio for a pulse swallowing counter is 90.

While fully programmable counters offer a choice of 9 or 15 different divide ratios, the fixed prescaler offers only one choice. In between these two extremes is the variable modulus prescaler, in which a little bit of speed is sacrificed in favor of a little freedom in choosing divide ratios. A prescaler of this type plays a leading role in a pulse swallowing counter. An example is the 650 MHz 11C90 ÷ 10/11 prescaler shown symbolically in *Figure 5*.

The 11C90 contains three ECL flip-flops operating as a synchronous shift counter, driving a fourth ECL flip-flop operating as an asynchronous toggle. A shift counter is used because it is the fastest configuration in the synchronous menagerie. As a concession to speed, there are no preset inputs and only the outputs of the fourth flip-flop are brought out of the package. A third output repeats the Q waveform via an internal converter and a high speed totem-pole TTL buffer. The internal feedback logic is such that the output is HIGH for six cycles and LOW for five cycles of the input clock. An auxiliary input can modify the feedback so that the output is HIGH for five cycles and LOW for five cycles. In either case, at the instant the output goes HIGH, the circuit is already committed as to whether the output period will be 10 or 11 clock cycles long. Further, the decision as to the length of the next output period need not be made until just before the final (10th or 11th) clock of the current period. This feature means that any external logic operating with the 11C90 has almost 10 (or 11) clock periods in which to decide what the divide ratio of the next output period will be and apply the appropriate signal to the auxiliary control input.

A highly simplified block diagram of a pulse swallowing counter is shown in *Figure 6*. The variable modulus prescaler is shown as two fixed prescalers with a switch to select the output of either one. A swallow counter controls the position of the switch, while a program counter provides the net output f_3, which also serves as a Preset control. At the beginning of a cycle, the switch selects the upper prescaler. After S pulses of f_2, the swallow counter throws the switch to the lower prescaler output. Still later, the program counter reaches maximum and causes a Preset. This in turn causes the swallow counter to throw the switch back to the upper prescaler output and start a new cycle.

A slightly more sophisticated block diagram of a pulse swallowing counter is shown in *Figure 7*. The prescaler and the swallow counter are each one stage, while the program counter is normally two or more stages. As a starting point, assume that a parallel enable signal has just occurred and the preset data has been synchronously entered into all the counter flip-flops. This action returns the two TC outputs to the inactive state, ending the Preset mode. The TC signal of the swallow counter enables its CE input and changes the prescaler to the upper (numerically larger) divide ratio. Both counters start counting up, and after S pulses of f_2 the swallow counter reaches maximum. Its TC output becomes active, locking it into the maximum state and simultaneously changing the prescaler to the lower divide ratio. The program counter continues counting up to its maximum, whereupon its TC output goes to the active state to enable the Preset mode and start a new operation cycle.

It is important to note that the divide ratio M of the program counter determines how many f_2 pulses there are in a complete program cycle; the swallow counter isn't involved. The role of the swallow counter is to modify, within limits, the number of f_1 pulses into the prescaler that are required to produce the M pulses of f_2.

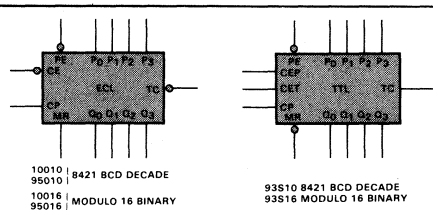


Fig. 2 Examples of Programmable Counters

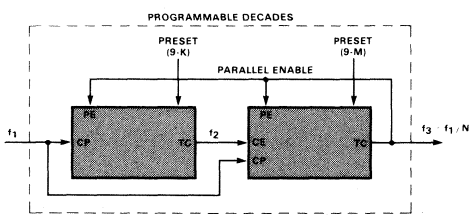


Fig. 3 Conventional Programmable Divider

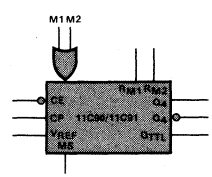


Fig. 5 Variable Modulus ÷ 10/11 650 MHz Prescaler

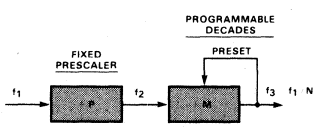


Fig. 4 Fixed Prescaler Used to Reduce Frequency

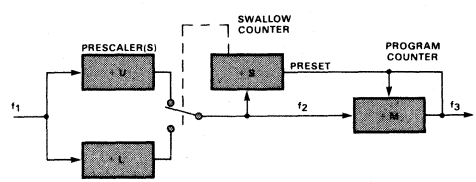


Fig. 6 Simulated Function of a Swallow Counter

INTRODUCTION

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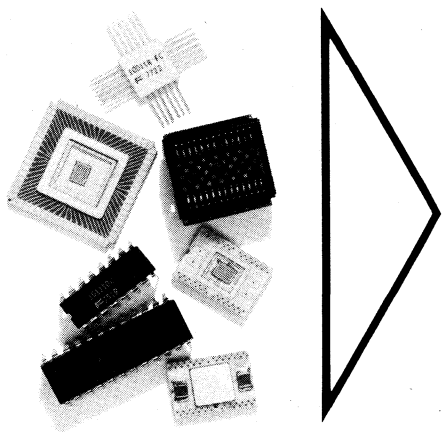
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F100K
INTRODUCTION

Competitive pressure in the data processing industry, with ever-increasing data volumes and new architectures, has stimulated the need for faster processing rates, higher machine densities, and greater system reliability. These requirements can only be met by the use of higher speed integrated circuits with more on-chip integration and multipurpose logic functions. Advanced packaging techniques and optimum system interconnects must be applied to take full advantage of this increased circuit performance. To facilitate system architecture, these high performance integrated circuits also must be less sensitive to environmental influence, i.e., easier to use and have a tighter ac window.

The new F100K standard subnanosecond ECL family has been designed to meet all these requirements. It was planned to provide next-generation system performance and density without total use of LSI while still being compatible with LSI approaches. Fully compensated ECL is used to eliminate most of the traditional ECL limitations while retaining all the advantages.

SELECTION OF CIRCUIT APPROACH

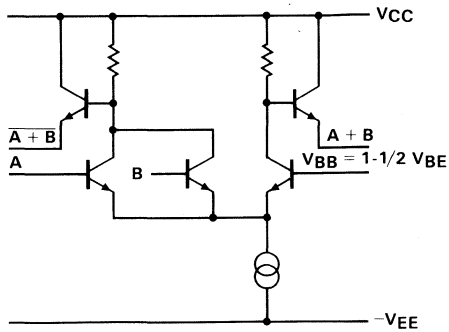
Many circuit implementations were carefully considered prior to selecting the optimum gate configuration for the F100K family. Some of the circuits studied are shown in *Figure 10-1.* The emitter-follower current-switch (E^2CL) and current-mode logic (CML) gates were eliminated mainly because of poor capacitive drive and lack of output wired-OR capability. The CML gate also has low noise margins. The 2-1/2D, EFL, DCTTL and hysteresis gates were eliminated due to the lack of simultaneous complementary outputs along with difficult temperature and voltage compensation characteristics that lead to the loss of system noise immunity.

The choice narrowed down to the current-switch emitter-follower ECL gate which offers the following characteristics:

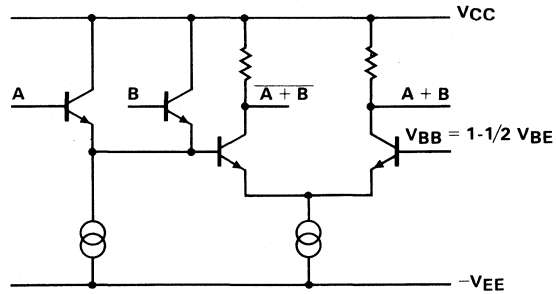
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- High fan-out capability
- Simultaneous complementary outputs
- Excellent ac characteristics
- Compatibility with existing ECL logic and memories
- Series gating capability
- Good noise immunity
- Amenable full compensation and extended temperature characteristics
- External wired-OR capability

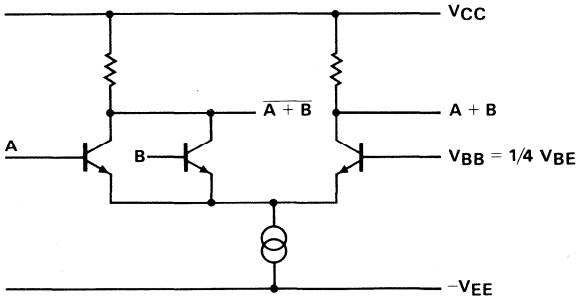
F100K circuits operate with a V_{EE} power supply of −4.5 V ±7% to reduce power dissipation. However, a −5.2 ±10% power supply can be used if desired since these circuits are fully voltage and temperature compensated. Therefore F100K directly interfaces with the widely available 2-ns ECL circuits. It should be emphasized that F100K is a *standard ECL family* with subnanosecond switching speed. Major segments of the computer industry were involved in its definition to ensure its acceptance as a standard product family.



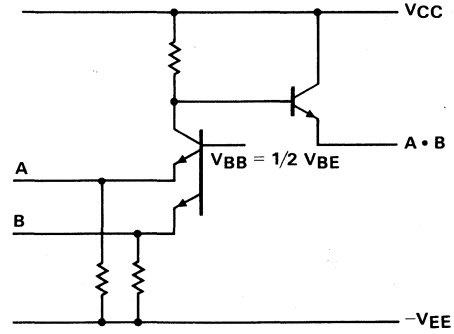
a. ECL Current-Switch Emitter-Follower



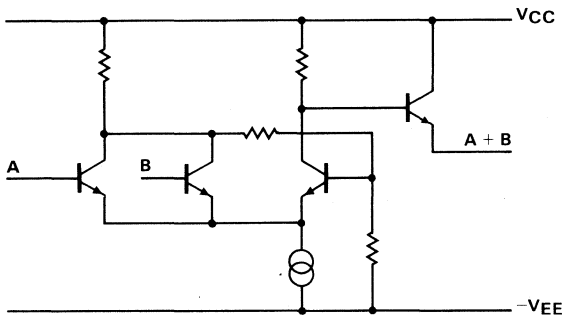
b. E²CL Emitter-Follower Current Switch



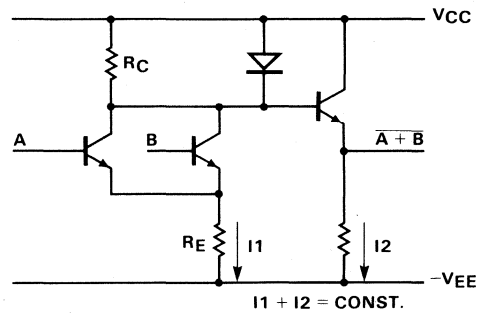
c. CML Current Mode Logic



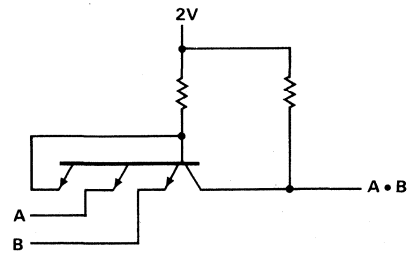
d. EFL Emitter-Follower Logic



e. FBG Feedback Gate, Hysteresis Gate



f. 2-1/2 Diode Logic



g. DCT²L AND Gate

Fig. 10-1 Gate Configuration Options

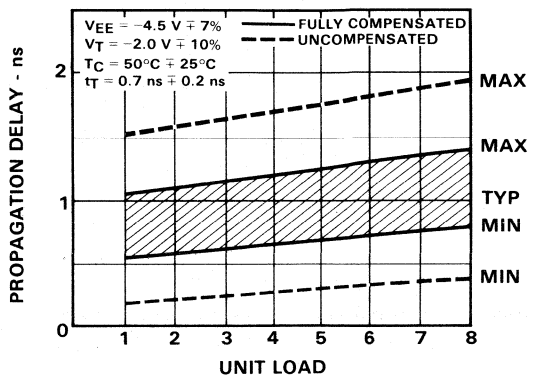


Fig. 10-2 Comparison of Propagation Delays

F100K PHILOSOPHY

The four key features of F100K are high speed at reduced power, high level of on-chip integration, most flexible logic functions available to date, and optimum I/O pin assignment.

The high speed is obtained by the use of ECL design techniques and the advanced Isoplanar II process. All circuit inputs have similar loading characteristics to ease drive requirements, i.e., buffers are incorporated where an input pin would normally drive more than one on-chip gate. The on-chip delay incurred by buffering is less than the system delay caused by an output which drives a capacitance of higher than 3 unit loads. Full compensation was selected for the F100K family to provide improved switching characteristics. Full compensation results in constant signal levels, constant thresholds and improved noise margins over temperature and voltage variations from chip to chip, and thus a tighter ac window in the system environment. A comparison of fully compensated ECL to conventional ECL shows a 2:1 improvement in system ac performance due solely to full compensation *(Figure 10-2).* And, the improved speed has been achieved at reduced power. This power reduction is accomplished by the use of advanced process technology that reduces parasitic capacitances and improves tolerances, by optimum circuit designs using series gating and collector and emitter dotting, and by designing for the use of a −4.5 V V_{EE} power supply.

Higher on-chip integration is made possible by using the 24-pin package to increase the number of pins available for logic by 62% over the conventional 16-pin package. The emphasis in F100K is to minimize the number of SSI functions and maximize the use of MSI and LSI to reduce wiring delays and thus make more efficient use of the fast on-chip switching technology. Only 10 SSI functions are needed to serve all the system needs presently requiring 25 functions in the ECL 10K family.

The logical extension of the F100K family is LSI and already a function providing the equivalent of up to 285 gates, *i.e.,* a 16 × 4 read/write register file, is being developed.

F100K was planned to minimize the total number of logic functions by increasing the flexibility of each function and by making use of more I/O pins. Since next-generation system performance and ease of system designs are major F100K goals, pin assignment is important and was planned to minimize crosstalk, noise coupling and feedthrough, to facilitate OR-ties and ease power-bus routing. Some of the key considerations in selecting the F100K pin assignments were:

- Locate power pins in the center on opposite sides of the package to ease system design and chip layout and to provide low inductance connections.
- Provide two V_{CC} pins, one for the circuit reference and one for the outputs to minimize noise coupling and maximize logic flexibility.
- Locate in-phase outputs adjacent to input pins, where possible, to prevent slowdown due to feedback.
- Locate inverting outputs of logically independent gates adjacent to each other for the shortest possible wired-emitter OR-ties. This provides an AOI function.
- Locate common pins such as common reset and common clock at pin number 22 and address or control inputs at pins 19 and 20. This is to maximize use of CAD for board layouts.
- When feasible, to create multipurpose functions, mode control pins are used to change the character of the functions. These pins can either be controlled by standard logic levels or hard wired, *i.e.*, tied to V_{CC} or left open.

REALIZATION

The fabrication technology of the F100K family is the advanced Isoplanar II process which provides transistors with very high, well controlled switching speeds, extremely small parasitic capacitances and f_T in excess of 5 GHz.

The technology can best be described by comparing the integrated circuit transistor structures of the conventional Planar* process and that of the Isoplanar II process *(Figure 10-3)*. The top view shows the area needed for each structure; the dashed area is the center of the isolation area.

*Planar is a patented Fairchild process.

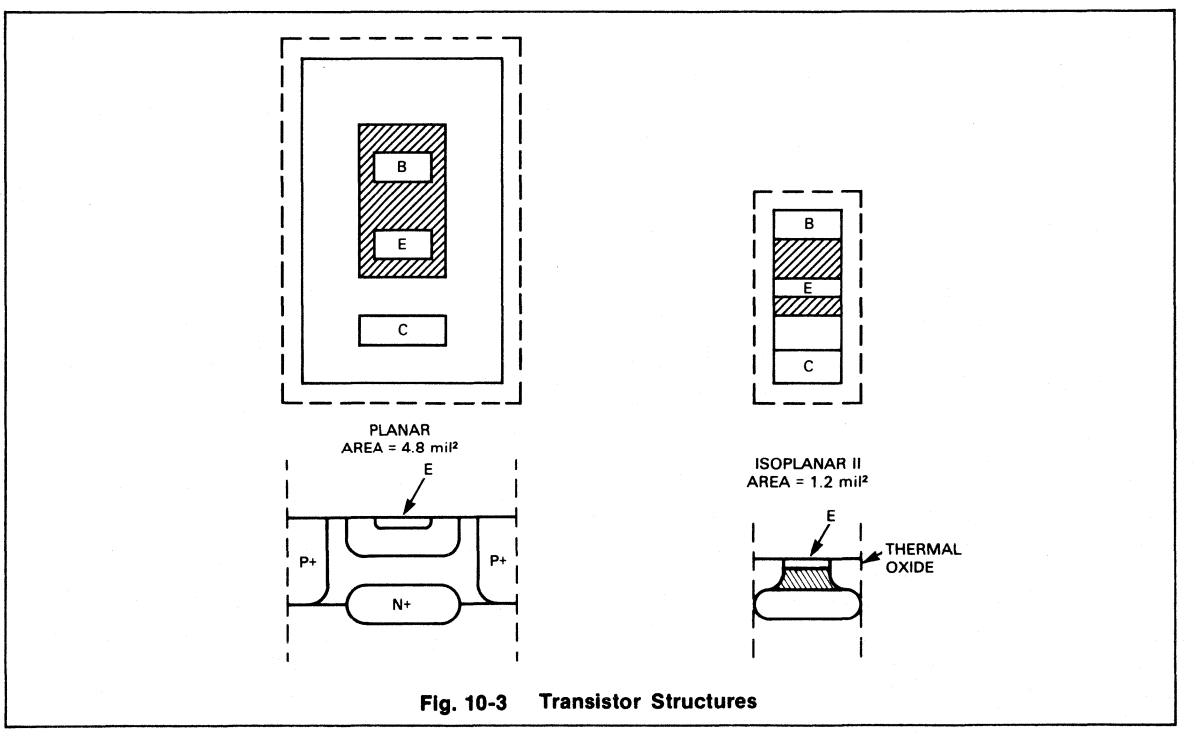


Fig. 10-3 Transistor Structures

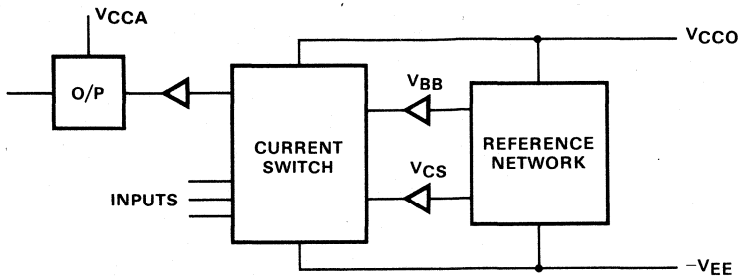


Fig. 10-4 ECL Gate

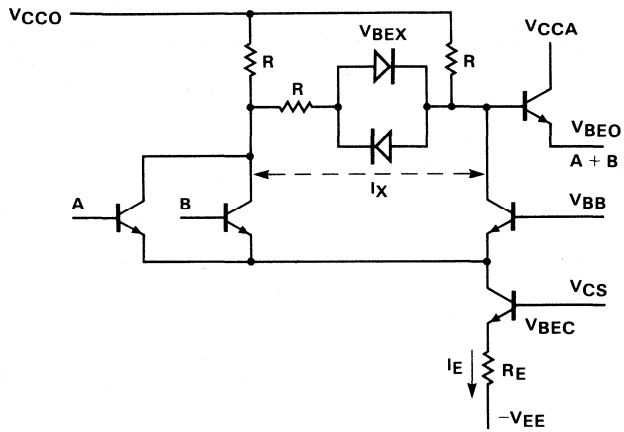


Fig. 10-5 Temperature Compensation

In the Isoplanar process, a thick oxide is selectively grown between devices instead of the P+ region which is present in the Planar process. Since this oxide needs no separation from the base-collector regions, a substantial reduction in device and chip size can be realized. The base and emitter ends terminate in the oxide wall therefore the masks can overlap the device area into the isolation oxide. This overlap feature means that base and emitter masking does not have to meet the extremely close tolerances that might otherwise be necessary, and standard photolithographic processes can be used.

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The "walled emitter" structure allows over a 70% reduction of the transistor silicon area compared to that of a conventional Planar transistor. For a given emitter size, the collector-base area is also reduced by more than 60%. The reduced junction areas result in corresponding reductions in collector-base and collector-substrate capacitances.

Since the active transistor area is only under the emitter, all capacitance and resistance values outside this area are reduced. Parasitic values are further reduced by taking advantage of the masking alignment latitude resulting from the self-aligning nature of the structure.

The heart of F100K is fully compensated ECL[2]. The basic gate consists of three blocks—the current switch, the output emitter followers, and the reference or bias network *(Figure 10-4)*.The current switch allows both conjunctive and disjunctive logic. The output emitter followers provide high drive capability through impedance transformation and allows for increased logic swing. The bias network sets dc thresholds and current-source bias voltages. Temperature compensation at the gate output is achieved by incorporating a cross-connect branch between the complementary collector nodes of the current switch and driving the current source with a temperature insensitive bias network[3] *(Figure 10-5)*.

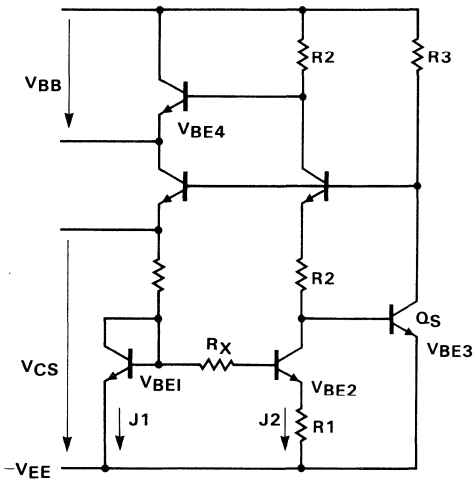


Fig. 10-6 Reference Network

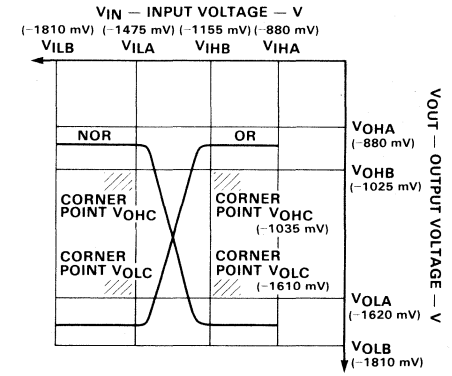


Fig. 10-7 Transfer Characteristics

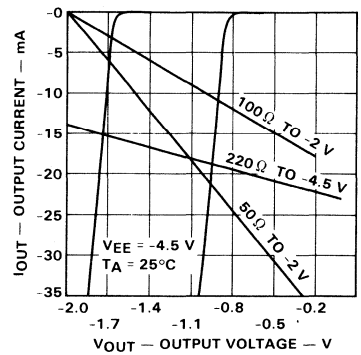


Fig. 10-8 Output Characteristic vs Output Terminations

As junction temperature increases and the forward base-emitter voltage of the output emitter-follower decreases, the collector node of the current switch must become more negative. Since the current-source bias voltage, V_{CS}, is independent of temperature, the switch current increases with temperature due to the temperature dependence of V_{BEC}. The combination of temperature controlled current, I_e, and the cross-connect branch current, I_x, forces the proper temperature coefficient at the collector node of the current switch to null out the V_{BEO} tracking coefficient.[1]

The schematic for the reference network displays a V_{BE} amplifier in the bottom left corner *(Figure 10-6)*. Two base-emitter junctions are operated at different current densities, J1 and J2. The resulting voltage difference, V_{BE1} minus V_{BE2}, appears across R1 and is amplified by the ratio R2/R1. Note that R2 is used twice, once to generate V_{CS} and once to generate V_{BB}. The different current densities, J1 and J2, result in a positive temperature tracking coefficient across R2, which cancels the negative diode-tracking coefficient of V_{BE3} and V_{BE4}. The V_{CS} and V_{BB} thus generated are temperature insensitive at the extrapolated bandgap voltage of silicon[2,3] (approximately 1300 mV).[4] RX in the V_{BE} amplifier compensates for process variations of β and ΔV_{BE}[5]. Voltage regulation is achieved through a shunt regulator shown at the right side of the schematic.

REGULATING PERFORMANCE

F100K compatibility with existing ECL logic families and memories permits direct interface with slower logic families and ensures immediate memory availability. The typical logic swing is 800 mV *(Figure 10-7)* and all voltage levels are specified with a 50 Ω load to –2 V at all outputs to provide transmission line drive capability. However, the inherently low output impedance *(Figure 10-8)* and maximum specified output current, 50 mA, make 25 Ω drive possible at any or all outputs. Alternately, of course, higher termination impedances or other termination schemes are also useful.

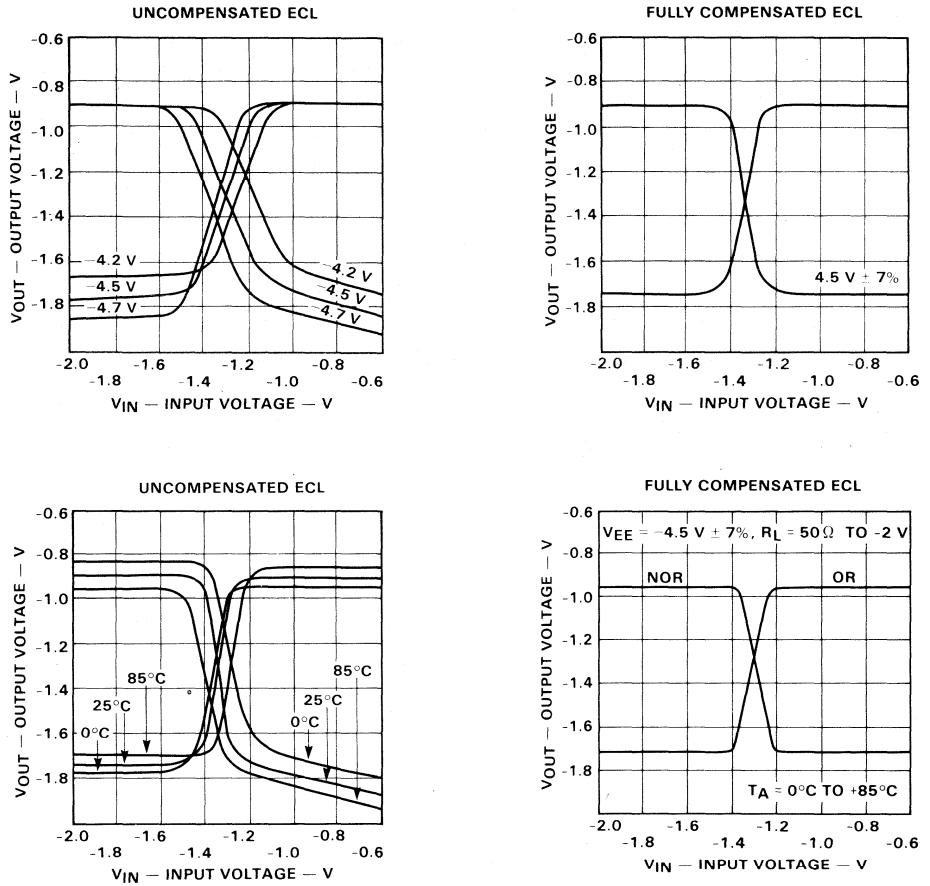


Fig. 10-9 Transfer Characteristics

F100K exhibits constant output levels and thresholds over the 0° C to 85° C specified temperature range and -4.2 V to -5.7 V specified voltage range*(Figure 10-9)*. V_{EE} power supply current is also constant over the specified voltage range*(Figure 10-10);* therefore:

- Propagation delay is constant versus power supply voltage variations thus tightening the ac window.
- Power dissipation is a linear function of the supply voltage, reducing worst-case power consumption.

The typical propagation delay of an SSI gate function driving a 50 Ω transmission line is 0.75 ns, including package, with a power dissipation of 40 mW resulting in a speed-power product of 30 pJ. For optimized MSI functions, the internal gates can dissipate < 10 mW with average propagation delay of < 0.5 ns, giving a power-speed product of < 5 pJ.

F100K has a tighter ac window over the wide range of environmental conditions; thus, the system timing requirements are eased and maximum system clock rates are increased. At the sacrifice of ac performance, the small signal input impedance was conservatively designed to be positive-real over the frequency range encountered by any circuit input. This provides adequate damping to insure ac stability within the system.

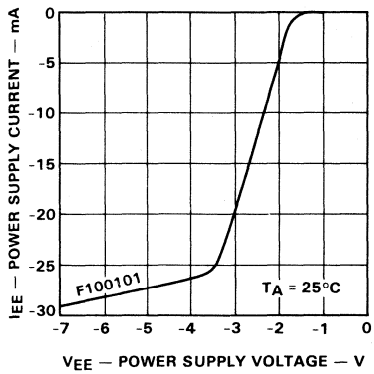


Fig. 10-10 Change In I_{EE} vs Change In V_{EE}

SYSTEM ASPECTS

F100K provides high density digital functions that outperform all other families on the market today. How does this increased circuit performance and higher on-chip density improve system performance?

Propagation delay and transition times vary (ac windows) when functions are operated at the extremes of the specified environmental ranges. With F100K, these variations are reduced and more predictable system timing is achieved. For synchronous machines and very high speed asynchronous systems, timing and its predictability are of utmost importance. Due to F100K constant supply current versus power supply voltage and because of constant levels and thresholds with respect to temperature, voltage variations and gradients, speed skews are minimized.

Not only timing but also maximum system clock rate is affected by the tighter ac window. Thus, with F100K the system designer can use a higher speed value in his worst-case calculations. This can be translated into higher possible system clock rates. Therefore, a machine can perform at up to twice the frequency, solely due to the F100K compensation features. Noise immunity will be of utmost importance in next-generation computers, since much of the noise generated within the system is inversely proportional to the switching transition time of the circuits. The F100K transition time is typically 0.7 ns as compared to 2.0 ns in other ECL families and should therefore increase system crosstalk by the same ratio.

F100K combats the increased system noise by maintaining a virtually invariant noise immunity with variations and gradients in power supply voltage, ambient and junction temperatures. The variation in junction temperatures is much larger than in earlier computer systems because of the mixture of LSI and SSI functions on the same boards.

The initial package selected for the F100K is a 24-pin Flatpak, 0.375 inches square, with leads on 50-mil centers, 6 leads per side. This package was chosen because it offers minimum performance degradations of circuit and system and uses a somewhat conventional packaging technology. More common packaging such as the dual in-line packages do not provide optimum performance due to the loss in speed entering and leaving the package as well as a decrease in system density. With the F100K packaging technique and higher chip complexities within the family, the system density is two to three times higher than that possible with other available ECL families. The various circuits in the F100K family, are listed in the table.

REFERENCES

1 V.A. Dhaka, J.E. Muschinske, and W.K. Owens, "Subnanosecond Emitter-Coupled Logic Gate Circuit Using Isoplanar II", IEEE Journal of Solid-State Circuits, October 1973, pp 368-372.

2 H.H. Muller, W.K. Owens, and P.W.J. Verhofstadt, "Fully Compensated Emitter Coupled Logic: Eliminating the Drawbacks of Conventional ECL", IEEE Journal of Solid-State Circuits, October 1973, pp 362-367.

3 R.R. Marley, "On-chip Temperature Compensation for ECL", Electron Products, March 1, 1971.

4 R.J. Widlar, "New Developments in IC Voltage Regulators", ISSSCC Digital Technical Papers, February 1970, pp 157-159.

5 W.K. Owens, "Temperature Compensated Voltage Regulator Having Beta Compensating Means", United States Patent, No. 3,731,648, December 25, 1973.

DC FAMILY SPECIFICATION

DC Characteristics for the F100K Series Family-Parametric Limits listed below are guaranteed for the entire Fairchild F100K ECL Family unless otherwise specified on the individual data sheets.

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0° C to +85° C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	-1025	-955	-880	mV	V_{IN} = V_{IHA} or V_{ILB}	Loading is 50 Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	V_{IN} = V_{IHB} or V_{ILA}	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed HIGH Signal for all inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed LOW Signal for all inputs	
I_{IL}	Input Current LOW	0.5			µA	V_{IN} = V_{ILB}	

F100K Family

DEVICE	FUNCTION
100101	TRIPLE 5-INPUT GATE
100102	QUINT 2-INPUT GATE
100107	QUINT EX-OR/NOR
100112	QUAD DRIVER
100114	LINE RECEIVER
100117	TRIPLE AOI
100118	5-WIDE AOI
100122	9-BIT BUFFER GATE
100123	HEX BUS DRIVER
100130	TRIPLE D LATCH
100131	TRIPLE D FLIP-FLOP
100136	MULTIPURPOSE COUNTING REGISTER
100141	8-BIT UNIVERSAL SHIFT REGISTER
100142	4 x 4 CONTENT ADDRESSABLE MEMORY
100145	16 x 4 REGISTER FILE
100150	HEX D LATCH
100151	HEX D FLIP-FLOP

DEVICE	FUNCTION
100155	QUAD MULTIPLEXER/LATCH
100156	MASK-MERGE
100158	SHIFT MATRIX
100160	DUAL 9-BIT PARITY
100163	DUAL 8-INPUT MULTIPLEXER
100164	16-INPUT MULTIPLEXER
100165	UNIVERSAL PRIORITY ENCODER
100166	9-BIT COMPARATOR
100170	UNIVERSAL DECODER
100171	TRIPLE 4-INPUT MULTIPLEXER
100179	CARRY LOOKAHEAD
100180	FAST 6-BIT ADDER
100181	4-BIT ALU BINARY/DECIMAL
100194	QUINT TRANSCEIVER
100414	256 x 1 RAM
100415	1024 x 1 RAM
100416	256 x 4 PROM

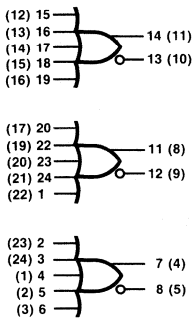
In addition to the above listed devices, a 168 Gate Array is available and is fully compatible with F100K logic and memories.

SSI LOGIC DIAGRAMS

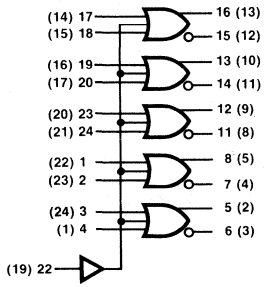
Dual-In-Line Pinouts Listed In ( )
Flatpak Pinouts Listed Without Parenthesis

V_{CC} = Pin 9 (6) V_{CCA} = Pin 10 (7) V_{EE} = Pin 21 (18)

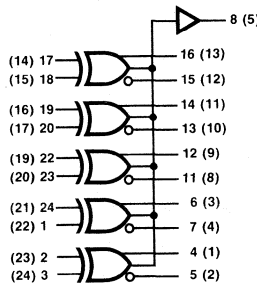
F100101
TRIPLE 5 OR/NOR



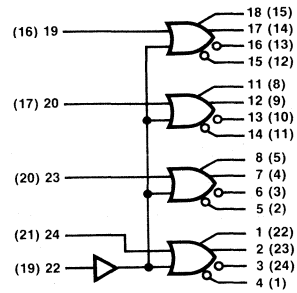
F100102
QUINT 2 OR/NOR



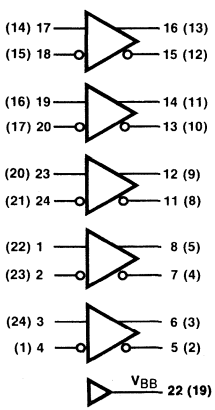
F100107
QUINT EXCLUSIVE OR/NOR



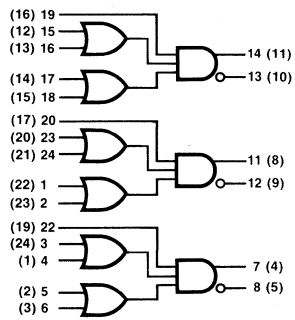
F100112
QUAD DRIVER



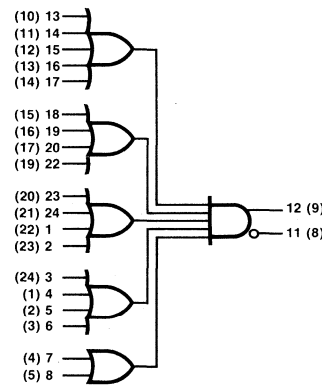
F100114
QUINT DIFFERENTIAL LINE RCVR



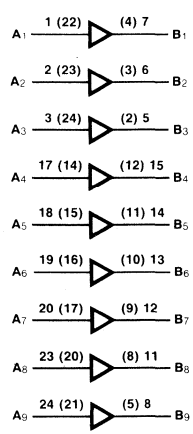
F100117
TRIPLE 2-WIDE OA/OAI



F100118
5-WIDE 5,4,4,4,2 OA/OAI

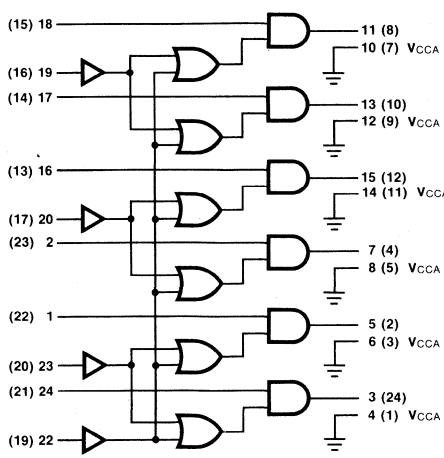


F100122
9-BIT BUFFER GATE



V_{EE} = 21 (18)
V_{CC} = 9 (6)
V_{CCA} = 4, 10, 16, 22
(1, 7, 13, 19)
( ) = DIP

F100123
HEX BUS DRIVER



V_{CC} = Pin 9 (6)
V_{EE} = Pin 21 (18)
V_{CCA} = Pins 10,12,14,8,6,4
(7),(9),(11),(5),(3),(1)

10

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

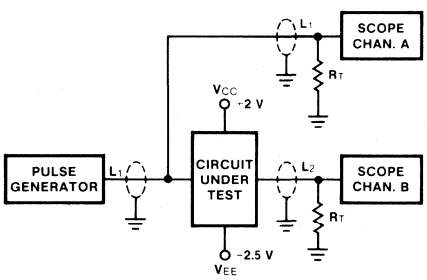
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
I_{IH}	Input Current HIGH				μA	$V_{IN} = V_{IHA}$
	F100101			350		
	F100102			350		
	F100102 Pin 22 (19)			300		
I_{EE}	Supply Current				mA	Inputs open
	F100101	-38	-26	-18		
	F100102	-80	-55	-38		

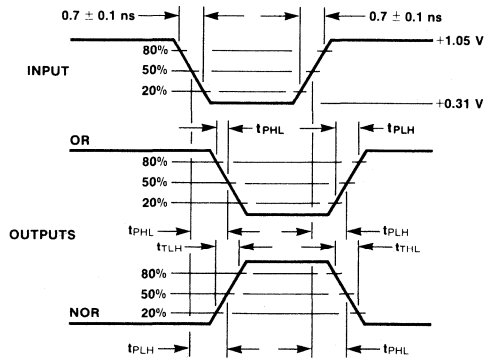
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay, LOW to HIGH, HIGH to LOW	0.45	0.75	0.95	ns	See Test Circuit and Waveforms
t_{PLH}, t_{PHL}	Propagation Delay, LOW to HIGH, HIGH to LOW F100102 Pin 22	1.0	1.5	1.95	ns	
t_{TLH} t_{THL}	Transition Time: F100102 Pin 22 20% to 80%; 80% to 20%	0.55	0.85	1.25	ns	
t_{TLH} t_{THL}	Transition Time: Others 20% to 80%; 80% to 20%	0.50	0.70	1.10	ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING TEST CIRCUIT AND WAVEFORMS





L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig and stray capacitance ≤ 3pF

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH Pins 3,18,20,23,24 (24),(15),(17),(20),(21)			250	μA	$V_{IN} = V_{IHA}$
	Pins 1,2,17,19,22 (22),(21),(14),(16),(19)			350		
I_{EE}	Supply Current	-96	-66	-46	mA	Inputs open

AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH} t_{PHL}	Propagation Delay, Pins 3,18,20,23,24 (24),(15),(17),(20),(21)	0.55	1.10	1.55	ns	See Test Circuit and Waveforms of F100101/100102
t_{PLH} t_{PHL}	Propagation Delay Pins 1,2,17,19,22 (22),(21),(14),(16),(19)	0.55	0.90	1.20	ns	
t_{PLH} t_{PHL}	Propagation Delay Pin 8 (5)	1.25	2.00	2.75	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	0.70	1.20	ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

DESCRIPTION—The F100112 contains four gates, each having two OR and two NOR outputs. Each gate has one individual input and one input that is common to the other three gates. The common input is buffered to minimize input loading, and is useful as either an enable function or as the input of a high fan-out driver of up to sixteen (16) 50 Ω lines (this minimizies speed skew between lines).

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

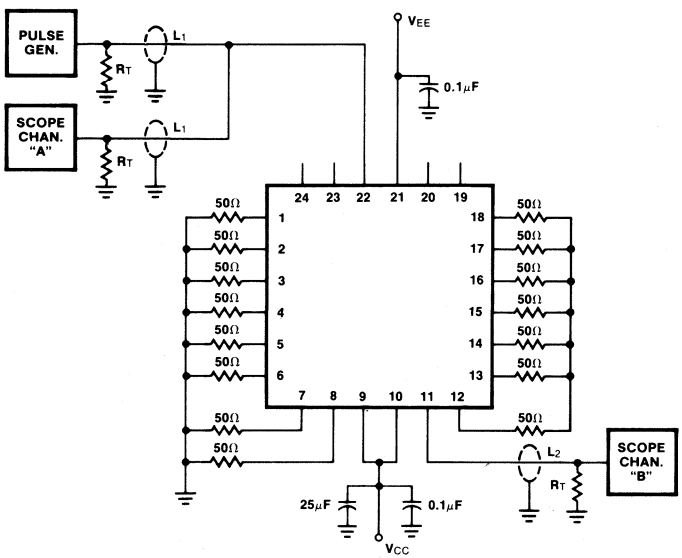
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
I_{IH}	Input Current HIGH Enable (Common Input) Others			 550 450	μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	-106	-73	-51	mA	Inputs open

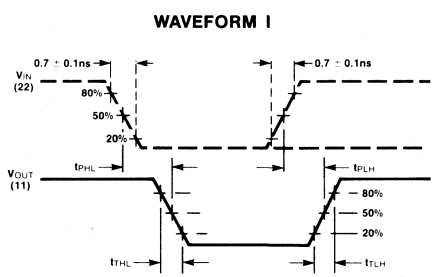
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

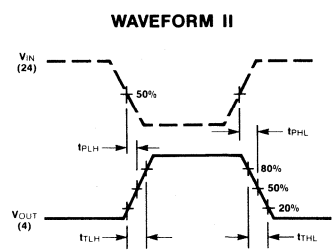
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PHL} t_{PLH}	Propagation Delay, Enable (Common Input)	0.85	1.30	1.70	ns	
t_{PHL} t_{PLH}	Propagation Delay, Data	0.55	0.90	1.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	0.90	1.40	ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING TEST CIRCUIT AND WAVEFORMS







V_{CC} = +2 V, V_{EE} = -2.5 V
L_1 and L_2 = equal length 50Ω impedance lines
R_T equal 50Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50Ω to GND
C_L = Jig & Stray Capacitance ≤ 3pF

DESCRIPTION—The F100114 is a Quint Differential Amplifier with emitter-follower outputs. An internal reference supply (V_{BB}) is available for single ended reception. Active current sources provide common mode rejection of 1.5 V in either the positive or negative direction. A defined output state exists if both inputs are at the same potential between and including $-V_{EE}$ and V_{CC}. The defined state is logic HIGH on outputs 5, 7, 11, 13, 15, (2), (4); (8), (10) and (12).

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
V_{IH}	Input Voltage HIGH	-1165			mV	Guaranteed HIGH Signal for All Inputs*
V_{IL}	Input Voltage LOW			-1475	mV	Guaranteed LOW Signal for All Inputs*
V_{CM}	Common Mode Voltage			1.5	V	Permissible V_{CM} with Respect to V_{BB}
V_{DIFF}	Input Voltage Differential		150		mV	Required for Full Output Swing
I_{IH}	Input Current HIGH		20	50	μA	$V_{IN} = V_{IHA}$ True Inputs = V_{BB} Complement Inputs = V_{ILB}
I_{CBO}	Leakage Current			1.0	μA	$V_{IN} = V_{EE}$ True Inputs = V_{BB} Complement Inputs = V_{ILB}
I_{EE}	Supply Current	-106	-73	-51	mA	True Inputs = V_{BB} Complement Inputs = V_{ILB}
V_{BB}	Reference Voltage	-1380	-1320	-1260	mV	Tie Pins 1,3,17,19,23, to Pin 22 (22), (24), (14), (16), (20) to pin (19)

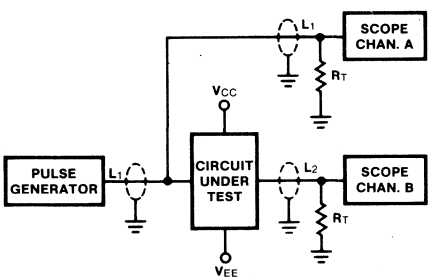
*Single ended operation, one of the inputs tied to V_{BB}.

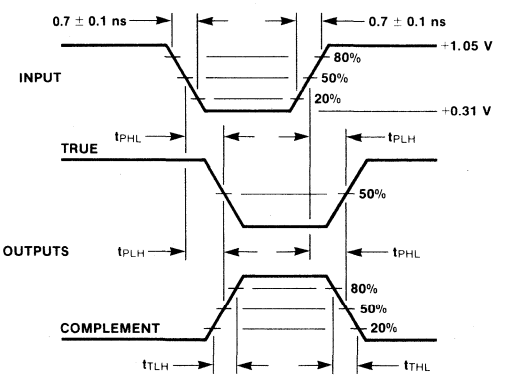
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5V; V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL} t_{PLH}	Propagation Delay,	0.65	1.40	2.20	ns	
t_{THL} t_{TLH}	Transition Time 80% to 20%; 20% to 80%	0.45	0.70	1.50	ns	See Test Circuit and Waveforms Complement Inputs = V_{BB}

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING TEST CIRCUIT AND WAVEFORMS





V_{CC} = +2 V, V_{EE} = -2.5 V
L_1 and L_2 = equal length 50Ω impedance lines
R_T equal 50Ω termination of scope
Decoupling 0.1 μF from V_{CC} and V_{EE} to GND
All outputs are loaded with 50Ω to GND
CL = Jig & Stray Capacitance ≤ 3pF

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
I_{IH}	Input Current HIGH F100117			220	μA	$V_{IN} = V_{IHA}$
	F100118			240		
	F100117 Pins 19,20,22 (16),(17),(19)			350		
	F100118 Pins 13,14,15,16,17 (10),(11),(12),(13),(14)			350		
I_{EE}	Power Supply Current F100117	-79	-54	-37	mA	Inputs open
	F100118	-57	-39	-27		

AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay LOW to HIGH, HIGH to LOW F100117	1.00	1.70	2.30	ns	See Test Circuit and Waveforms of F100101/100102
	F100117 Pins 19,20,22 (16),(17),(19)	0.45	0.75	0.95		
t_{PLH}, t_{PHL}	Propagation Delay, F100118 Pins 13,14,15,16,17, 1,2,23,24,7,8 (10),(11),(12),(13),(14) (22),(23),(20),(21),(4), (5)	1.15	1.90	2.50	ns	
t_{PHL}, t_{PLH}	Propagation Delay, F100118 Pins 18,19,20,22,3,4,5,6 (15),(16),(17),(19),(24), (1),(2),(3)	1.45	2.4	3.15	ns	
t_{TLH} t_{THL}	Transition Time: F100117 20% to 80%; 80% to 20%	0.50	0.75	1.10	ns	
t_{TLH} t_{THL}	Transition Time: F100118 20% to 80%; 80% to 20%	0.55	0.85	1.45	ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

F100122
9-BIT BUFFER
F100K SERIES ECL

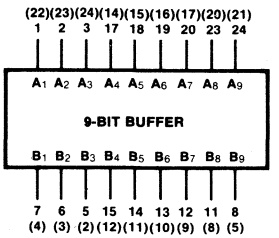
DESCRIPTION — The F100122 contains nine independent, high-speed, buffer gates each with a single input and a single output. The gates are non-inverting. These buffers are useful in bus oriented systems where minimal output loading or bus isolation is desired.

PRELIMINARY

PIN NAMES

A_n	Inputs
B_n	Outputs

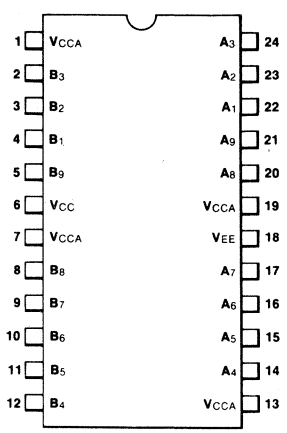
LOGIC SYMBOL



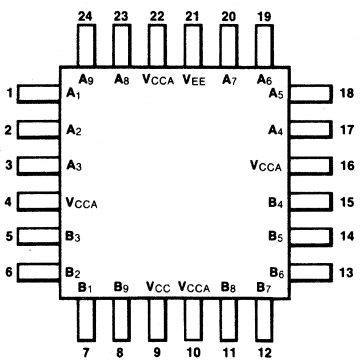
V_{EE} = 21 (18)
V_{CC} = 9 (6)
V_{CCA} = 4, 10, 16, 22 (1, 7, 13, 19)
( ) = DIP

CONNECTION DIAGRAMS

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

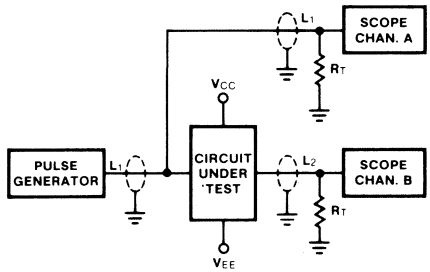
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH			350	μA	V_{IN} = V_{IHA}
I_{EE}	Supply Current		-70		mA	Inputs open

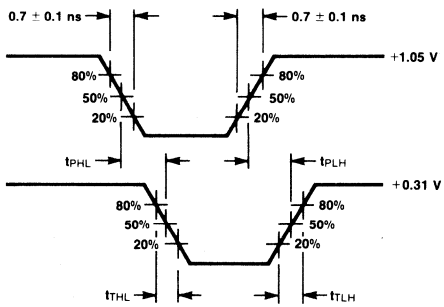
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL}, t_{PLH}	Propagation Delay		0.75		ns	
t_{TLH}, t_{THL}	Transition Time 20% to 80%, 80% to 20%		0.7		ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING TEST CIRCUIT AND WAVEFORMS





V_{CC} = +2 V, V_{EE} = -2.5 V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from V_{CC} and V_{EE} to GND
All outputs are loaded with 50 Ω to GND

F100123

HEX BUS DRIVER

F100K SERIES ECL

DESCRIPTION — The F100123 contains six bus drivers capable of driving terminated lines with terminations as low as 25 Ω. To reduce crosstalk, each output has its respective ground connection and transition times were designed to be longer than on other F100K devices. The driver itself performs the positive logic AND of a data input (pins 1, 2, 16, 17, 18 or 24) and the OR of two select inputs (pin 22 and either pins 19, 20 or 23). Enabling of data is possible in multiples of two, *i.e.*, 2, 4, or all 6 paths.

The output voltage LOW level is designed to be more negative than normal ECL outputs. This allows an emitter-follower output transistor to turn off when the termination supply is -2.0 V ± 10%, and thus present a high impedance to the data bus.

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

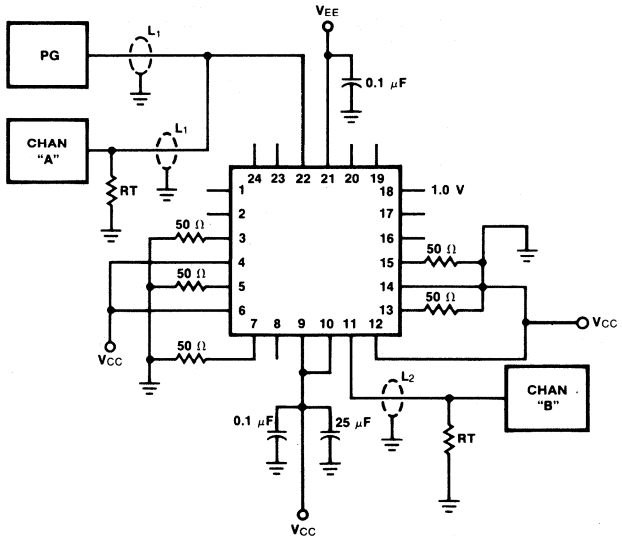
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_H	Input Current HIGH Hex Enable Data & Dual Enable			 330 230	μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	-235	-162	-113	mA	Inputs open

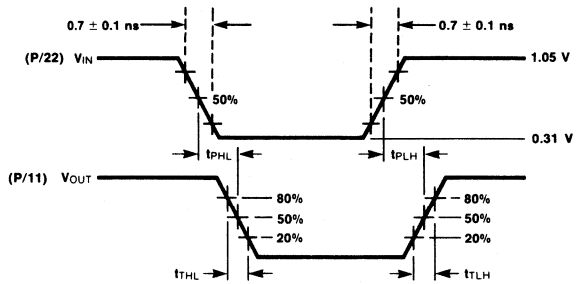
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL}	Propagation Delay, Data to Output	1.00	1.45	1.90	ns	See Switching Circuits & Waveforms
t_{PLH}	Propagation Delay, Data to Output	1.95	3.00	4.15	ns	
t_{PHL}	Propagation Delay Dual Enable to Output	1.20	1.80	2.35	ns	
t_{PLH}	Propagation Delay, Dual Enable to Output	2.30	3.40	4.50	ns	
t_{PHL}	Propagation Delay, Hex Enable to Output	1.20	1.80	2.35	ns	
t_{PLH}	Propagation Delay, Hex Enable to Output	2.60	3.75	4.90	ns	
t_{TLH}	Transition Time 20% to 80%	0.45	0.80	1.20	ns	
t_{THL}	Transition Time 80% to 20%	0.80	1.30	1.90	ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

F100123 SWITCHING CIRCUITS AND WAVEFORMS





V_{CC} = +2 V, V_{EE} = -2.5 V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig & Stray Capacitance ≤ 3 pF

F100130

TRIPLE D LATCH

F100K SERIES ECL

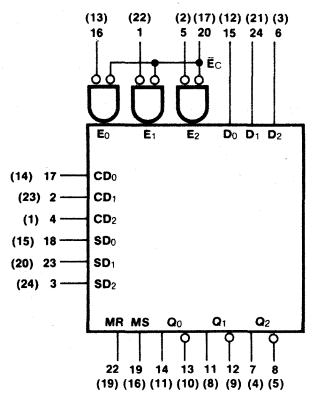
DESCRIPTION — The F100130 contains three D type latches with true and complement outputs and with Common Enable ($\overline{E}_C$), Master Set (MS) and Master Reset (MR) inputs. Each latch has its own Enable ($\overline{E}_n$), Direct Set (SD_n) and Direct Clear (CD_n) inputs. The Q output follows its Data (D) input when both $\overline{E}_n$ and $\overline{E}_C$ are LOW. When either $\overline{E}_n$ or $\overline{E}_C$ or both are HIGH, a latch stores the last valid data present on its D_n input before $\overline{E}_n$ or $\overline{E}_C$ went HIGH.

Both Master Reset (MR) and Master Set (MS) inputs override the Enable inputs. The individual CD_n and SD_n also override the Enable inputs.

PIN NAMES

CD_n	Individual Clear
SD_n	Individual Sets
$\overline{E}_n$	Individual Enables
$\overline{E}_C$	Common Enable
D_n	Data Inputs
MR	Master Clear
MS	Master Set
Q_n	Data Outputs

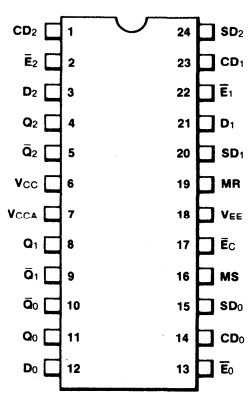
LOGIC SYMBOL



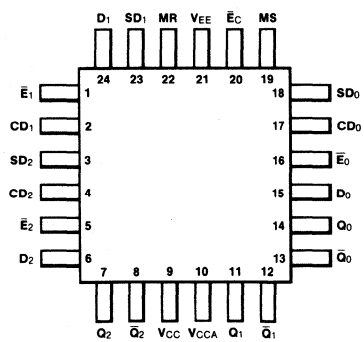
V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)
( ) = DIP

CONNECTION DIAGRAMS

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



TRUTH TABLE

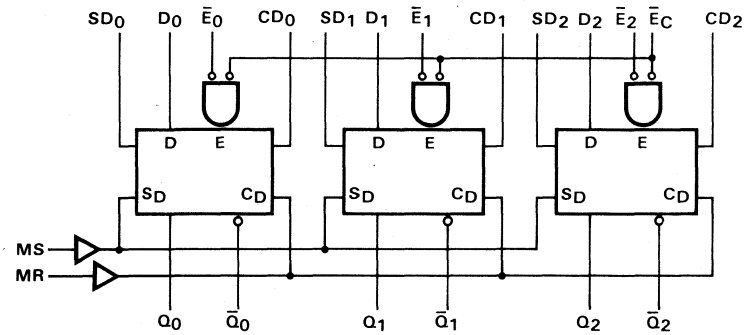
Each Latch

D_n	$\overline{E}_n$	$\overline{E}_C$	MS SD_n	MR CD_n	$\overline{Q}_n$
L	L	L	L	L	L
H	L	L	L	L	H
X	H	X	L	L	*
X	X	H	L	L	*
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

H = HIGH voltage level
L = LOW voltage level
X = Immaterial
* = Retains data present before $\overline{E}$ positive transition
U = Undefined

10

LOGIC DIAGRAM



DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
I_{IH}	Input Current HIGH				μA	$V_{IN} = V_{IHA}$
	D_n			350		
	CD_n, SD_n			530		
	$\overline{E}_n$			240		
	$\overline{E}_c$, MR, MS			450		
I_{EE}	Supply Current	-149	-106	-74	mA	Inputs open

AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC}, = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PHL} t_{PLH}	Propagation Delay, Data to Output	0.50	0.85	1.10	ns	See Circuit and Waveforms for F100131
t_{PHL} t_{PLH}	Propagation Delay, CD_n, SD_n, $\overline{E}_n$ to Output	0.65	1.10	1.45	ns	
t_{PHL} t_{PLH}	Propagation Delay, $\overline{E}_c$ to Output	0.75	1.20	1.55	ns	
t_{PHL} t_{PLH}	Propagation Delay, CD_n, SD_n	1.10	1.85	2.40	ns	
t_s	Set-Up Time				ns	
	Data	0.60				
	CD_n, SD_n	0.80				
	MR, MS	1.70				
t_h	Hold Time				ns	
	Data	0.30				
	CD_n, SD_n	0.0				
	MR, MS	-0.5				
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	0.90	1.30	ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

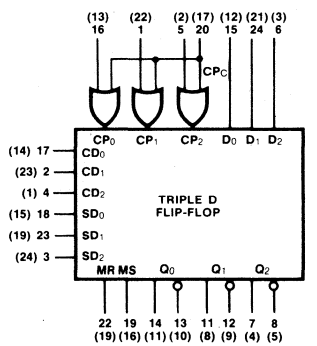
F100131

TRIPLE D FLIP-FLOP

F100K SERIES ECL

DESCRIPTION—The F100131 contains three D type master/slave flip-flops with true and complement outputs, a Common Clock (CP_C), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clocks (CP_n), Direct Set (SD_n) and Direct Clear (CD_n) inputs. Data enters a master when both CP_n and CP_C are LOW and transfers to a slave when CP_n or CP_C (or both) go HIGH. The Master Set, Master Reset and individual CD_n and SD_n inputs override the Clock inputs.

LOGIC SYMBOL



V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)

PIN NAMES

CP_n	Individual Clocks
CP_C	Common Clock
D_n	Data Input
CD_n	Individual Clear
SD_n	Individual Set
MR	Master Reset
MS	Master Set
Q_n	Data Outputs

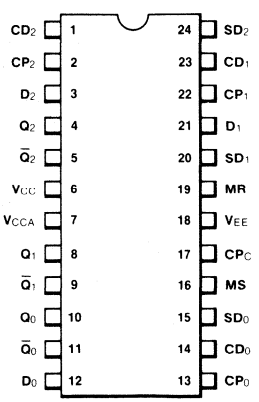
TRUTH TABLE (Each Flip-Flop)

D_n	CP_n	CP_C	MS SD_n	MR CD_n	Q_n (t+1)
L	⎍	L	L	L	L
H	⎍	L	L	L	H
L	L	⎍	L	L	L
H	L	⎍	L	L	H
X	H	X	L	L	Q_n(t)
X	X	H	L	L	Q_n(t)
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

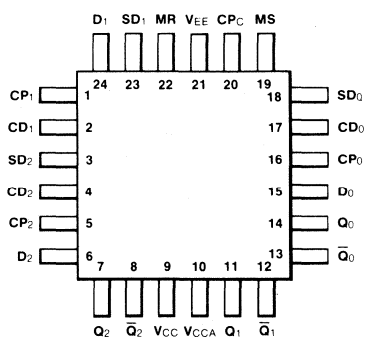
H = HIGH voltage level
L = LOW voltage level
X = Immaterial
U = Undefined
t,t+1 = Time before and after CP positive transition

CONNECTION DIAGRAMS

DIP (TOP VIEW)

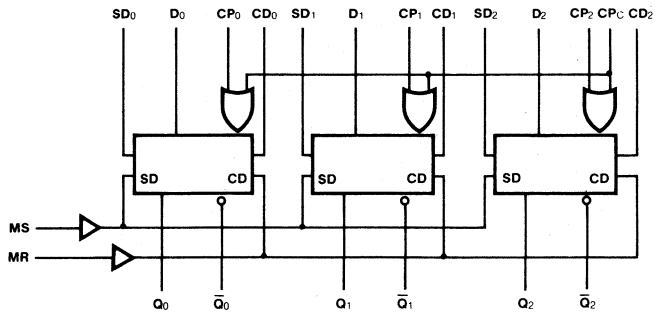


FLATPAK (TOP VIEW)



10

LOGIC DIAGRAM



DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

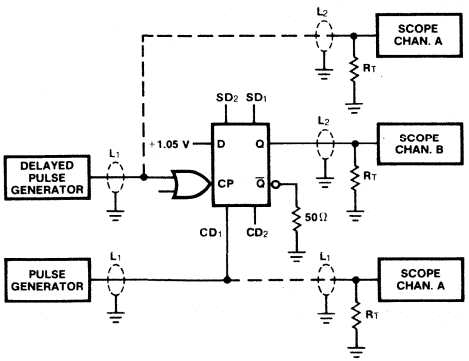
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
I_{IH}	Input Current HIGH				μA	$V_{IN} = V_{IHA}$
	CP_n, D_n			240		
	MS, MR, $\overline{CP}_C$			450		
	CD_n, SD_n			530		
I_{EE}	Supply Current	-149	-106	-74	mA	Inputs open

AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PHL} t_{PLH}	Propagation Delay, CP_C to Output	0.75	1.25	1.65	ns	See Figure 1
t_{PHL} t_{PLH}	Propagation Delay, CD_n, SD_n to Output	0.70	1.15	1.50	ns	
t_{PHL} t_{PLH}	Propagation Delay, CP_n to Output	0.70	1.15	1.50	ns	
t_{PHL} t_{PLH}	Propagation Delay, MS, MR (Clock HIGH)	1.05	1.90	2.75	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	0.90	1.30	ns	
f_{max}	Toggle Frequency	400	550		MHz	See Figure 2
t_s	Set-Up Time				ns	See Figure 3
	D_n	0.60				
	CD_n, SD_n	1.70				
	MS, MR	2.00				
t_h	Hold Time				ns	
	D_n	0.30				
	CD_n, SD_n	0.50				
	MS, MR	0.60				

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING CIRCUITS AND WAVEFORMS



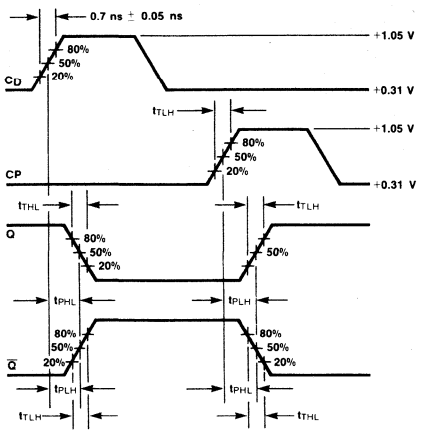
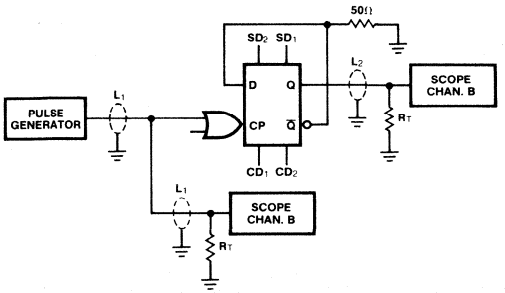


Fig. 1



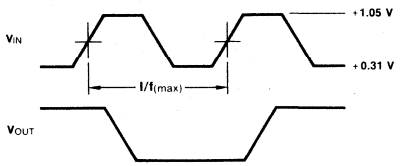


Fig. 2

V_{CC} = +2 V, V_{EE} = −2.5 V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig & Stray Capacitance ≤ 3 pF

10

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

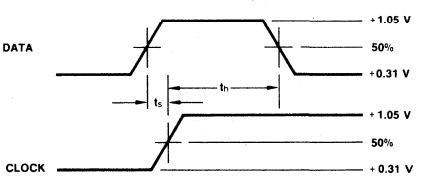


Fig. 3 Set-Up and Hold Times

F100136

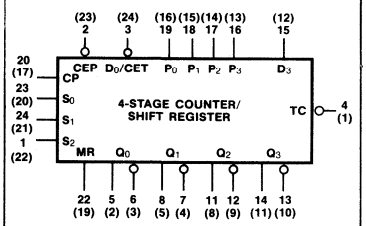
4-STAGE COUNTER/SHIFT REGISTER

F100K SERIES ECL

DESCRIPTION—The F100136 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (S_n) inputs determine the mode of operation, as shown in the mode select table. Two Count Enable ($\overline{CEP}$, $\overline{CET}$) inputs are provided for ease of cascading in multi-stage counters. One Count Enable ($\overline{CET}$) input also doubles as a Serial Data (D_0) input for shift-up operation. For shift-down operation D_3 is the Serial Data input. In counting operations the Terminal Count ($\overline{TC}$) output goes LOW when the counter reaches 15 in the count/up mode or 0 (zero) in the count/down mode. In the shift modes, the $\overline{TC}$ output repeats the Q_3 output. The dual nature of this $\overline{TC}/Q_3$ output and the $D_0/\overline{CET}$ input means that one interconnection from one stage to the next higher stage serves as the link for multi-stage counting or shift-up operation. The individual Preset (P_n) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A HIGH signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, a synchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops.

PRELIMINARY

LOGIC SYMBOL



V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)
( ) = DIP

PIN NAMES

$\overline{CEP}$	Count Enable
$D_0/\overline{CET}$	Do - Serial Data Input Shift Up CET - Count Enable
S_n	Select Inputs
MR	Master Reset
P_n	Preset Inputs
TC	Terminal Count
D_3	Serial Data Input Shift Down
Q_n	Data Outputs

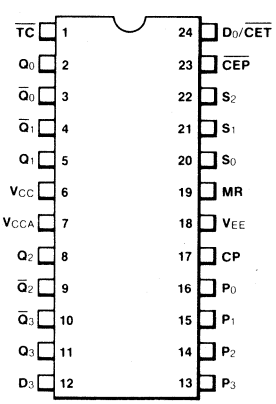
FUNCTION SELECT TABLE

S_0	S_1	S_2	FUNCTION
L	L	L	Load
L	H	L	Shift down
H	H	L	Shift up
L	L	H	Count down
L	H	H	Count up
H	H	H	Hold
H	L	L	Complement
H	L	H	Clear

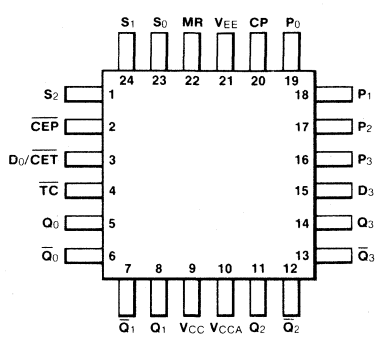
H = HIGH voltage level
L = LOW voltage level

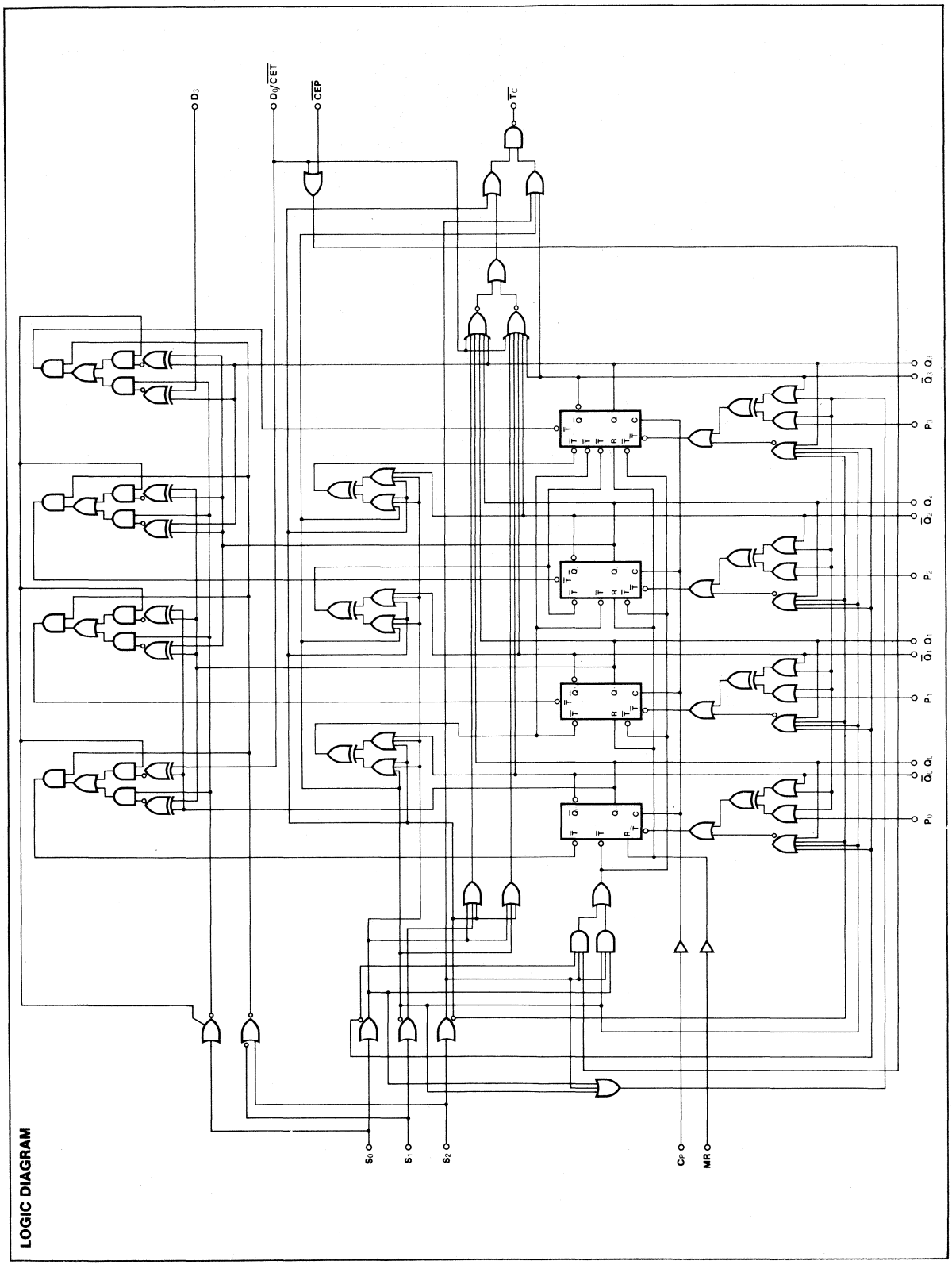
CONNECTION DIAGRAMS

DIP (Top View)



Flatpak (Top View)





LOGIC DIAGRAM

10

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

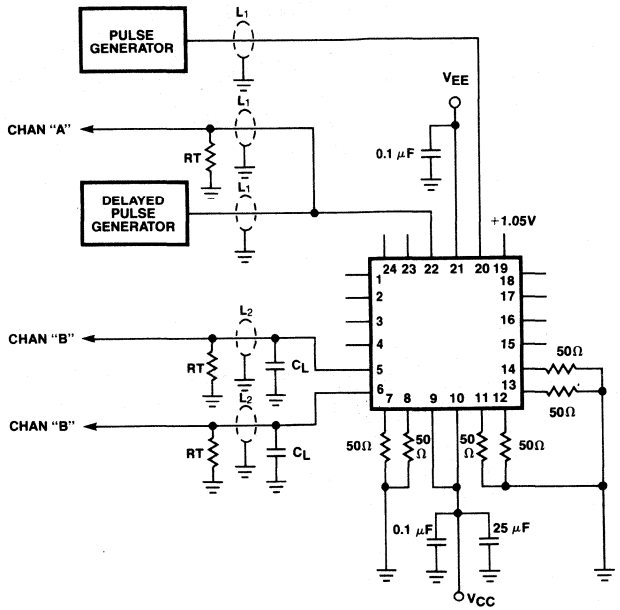
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH				μA	$V_{IN} = V_{IHA}$
	Pn, Sn			180		
	$\overline{CEP}$			200		
	MR			240		
	D_3			280		
	CP			390		
	$D_0/\overline{CET}$			530		
I_{EE}	Supply Current	-283	-195	-136	mA	Inputs open

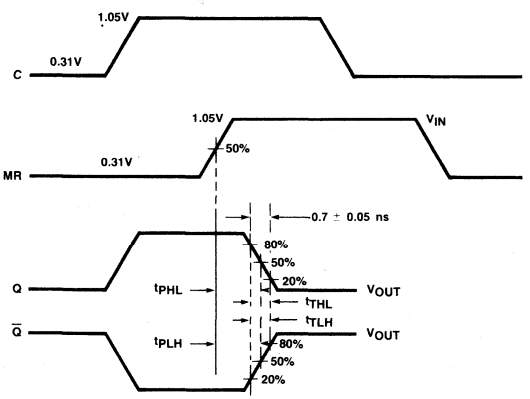
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5V, V_{CC} = GND

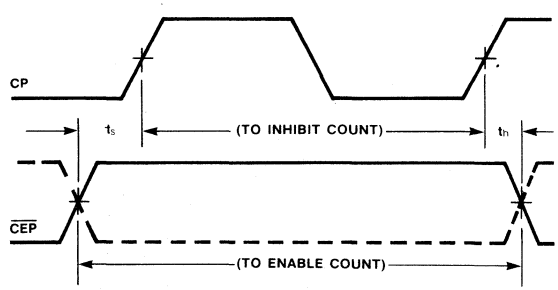
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL} t_{PLH}	Propagation Delay, CP to Q	0.85	1.45	1.90	ns	
t_{PHL} t_{PLH}	Propagation Delay, CP to $\overline{TC}$	2.30	3.40	4.40	ns	See Figure 1
t_{PHL} t_{PLH}	Propagation Delay, MR to Q	2.10	3.00	3.90	ns	
t_{PHL} t_{PLH}	Propagation Delay, MR to $\overline{TC}$	2.50	5.00	6.50	ns	
t_{PHL} t_{PLH}	Propagation Delay, $D_0/\overline{CET}$ to $\overline{TC}$	1.40	2.00	2.60	ns	
$f_{(MAX)}$	Toggle Frequency	300	450		MHz	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	1.00	1.70	ns	
t_s	Set-Up Time D_3, P_n S_n	3.20 3.20			ns	See Figure 2
t_h	Hold Time D_3, P_n S_n	−1.10 −0.3			ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

AC TEST CIRCUIT AND WAVEFORMS







V_{CC} = +2 V, V_{EE} = -2.5 V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig & Stray Capacitance ≤ 3 pF

Fig. 1

t_s is the minimum time before the transition of the enable or clock that information must be present at the data input.

t_h is the minimum time after the transition of the enable or clock that information must remain unchanged at the data input.

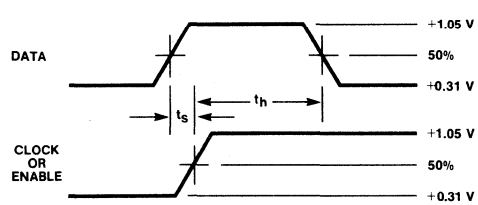


Fig. 2. Set-Up and Hold Times

F100141

8-BIT SHIFT REGISTER

F100K SERIES ECL

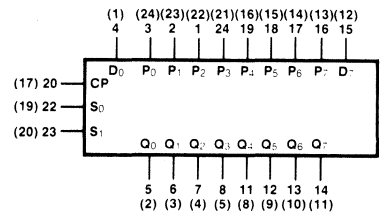
DESCRIPTION — The F100141 contains eight clocked D-type flip-flops with individual inputs (P_n) and outputs (Q_n) for parallel operation, and with serial inputs (D_n) and steering logic for bidirectional shifting. The flip-flops accept input data a set-up time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.

The circuit operating mode is determined by the Select inputs S_0 and S_1, which are internally decoded to select either "parallel entry", "hold", "shift left" or "shift right" as described in the Function Sheet Table.

PIN NAMES

CP	Clock
S_n	Select Inputs
D_n	Serial Inputs
P_n	Individual Inputs
Q_n	Data Outputs

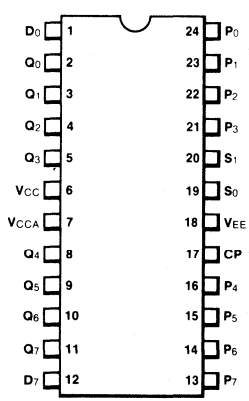
LOGIC SYMBOL



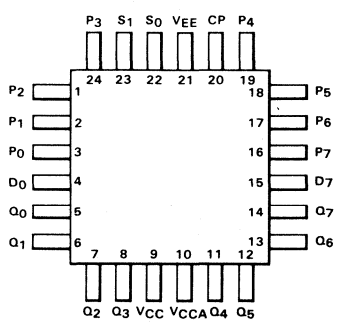
VCC Pin 9 (6)
VCCA Pin 10 (7)
VEE Pin 21 (18)
DIP

CONNECTION DIAGRAMS

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTION	INPUTS					OUTPUTS							
	D_7	D_0	S_1	S_0	CP	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Load Register	X	X	L	L	↑	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Shift Left	X	L	L	H	↑	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	L
Shift Left	X	H	L	H	↑	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	H
Shift Right	L	X	H	L	↑	L	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Shift Right	H	X	H	L	↑	H	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Hold	X	X	H	H	X	No Change							
Hold	X	X	X	X	H	No Change							
Hold	X	X	X	X	L	No Change							

H = High Level (Most Positive)
L = Low Level (Most Negative)
X = Don't Care (May be either High or Low)
↑ = Low to High transition

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

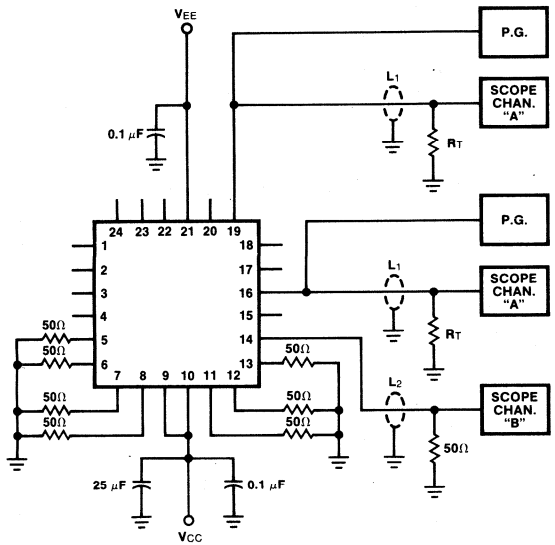
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH				μA	$V_{IN} = V_{IHA}$
	D_n, P_n, S_n			220		
	CP			640		
I_{EE}	Supply Current	-238	-170	-119	mA	Inputs open

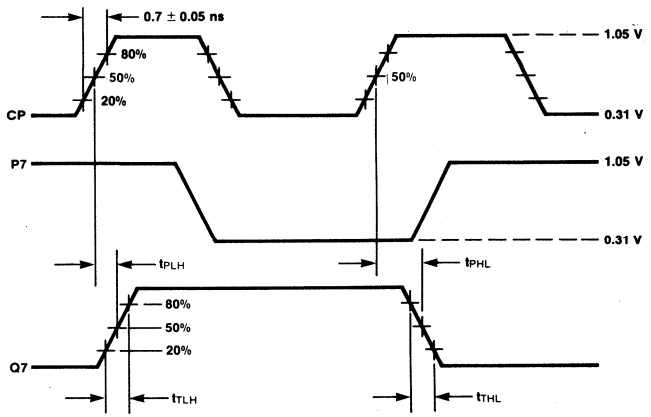
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL} t_{PLH}	Propagation Delay, CP to Output	1.10	1.70	2.20	ns	
f shift	Shift Frequency	380	500		MHz	See Figure 1
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.55	0.95	1.65	ns	
t_s	Set-Up Time				ns	
	D_n, P_n	1.0				
	S_n	2.7				See Figure 2
t_h	Hold Time				ns	
	D_n, P_n	0.0				
	S_n	-0.9				

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

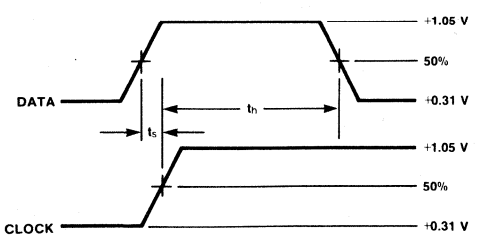
SWITCHING TEST CIRCUIT AND WAVEFORMS





V_{CC} = +2 V, V_{EE} = -2.5 V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig & Stray Capacitance ≤ 3pF

Fig. 1



t_s is the minimum time before the transition of the clock that information must be present at the data input

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

Fig. 2 Set-Up and Hold Times

F100150

HEX D LATCH

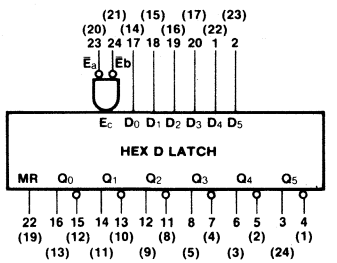
F100K SERIES ECL

DESCRIPTION — The F100150 contains six D type latches with the True and Complement Outputs, a pair of Common Enables ($\overline{E}_a$ and $\overline{E}_b$), and a common Master Reset (MR). A Q output follows its D input when both $\overline{E}_a$ and $\overline{E}_b$ are LOW. When either $\overline{E}_a$ or $\overline{E}_b$ (or both) are HIGH, a latch stores the last valid data present on its D input before $\overline{E}_a$ or $\overline{E}_b$ went HIGH. The MR input overrides all other inputs and makes the Q outputs LOW.

PIN NAMES

D_n	Inputs
MR	Asynchronous Master Reset
Q_n	True Outputs
$\overline{Q}_n$	Complement Outputs
$\overline{E}_a$ and $\overline{E}_b$	Common Enable Inputs (active LOW)

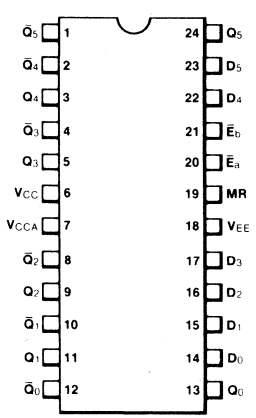
LOGIC DIAGRAM



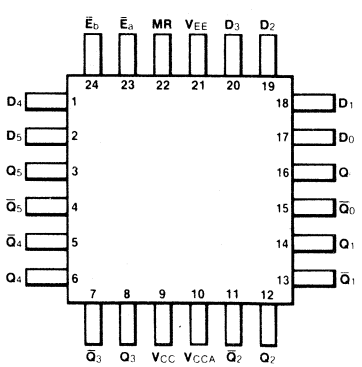
V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)
( ) = DIP

CONNECTION DIAGRAM

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



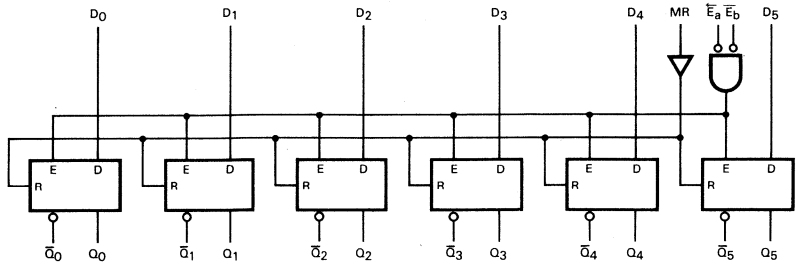
TRUTH TABLE
EACH LATCH

D_n	$\overline{E}_a$	$\overline{E}_b$	MR	Q_n
L	L	L	L	L
H	L	L	L	H
X	H	X	L	*
X	X	H	L	*
X	X	X	H	L

H = HIGH Level
L = LOW Level
X = Immaterial
* = Retains data present before $\overline{E}$ positive transition

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LOGIC DIAGRAM



DC CHARACTERISTICS: V_{EE} =-4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

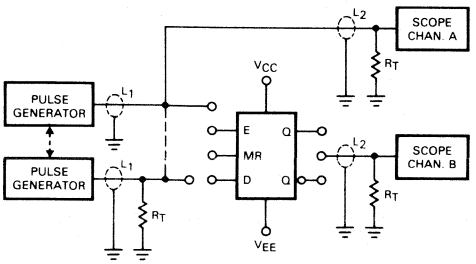
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH MR Inputs Data Inputs $\overline{\text{Enable}}$ Inputs			 450 340 520	μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	-159	-113	-79	mA	Inputs open

AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

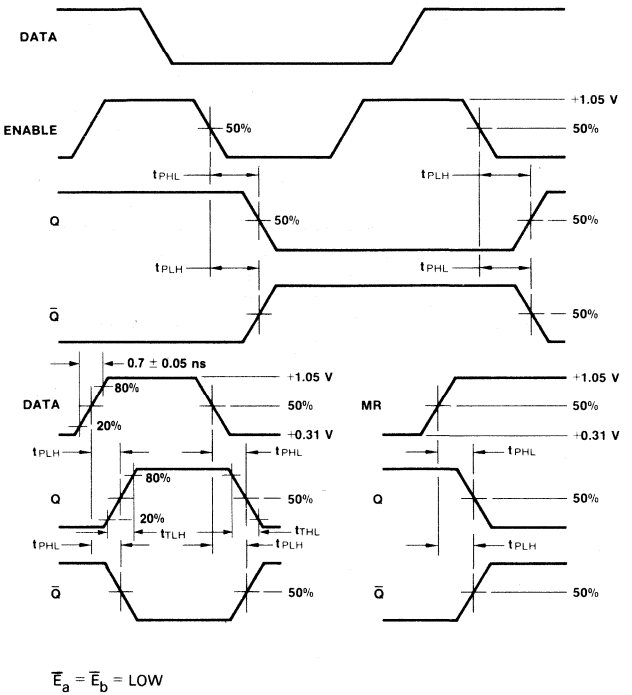
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL} t_{PLH}	Propagation Delay $\overline{\text{Enable}}$ to Output	0.75	1.15	1.50	ns	See Figure 1
t_{PLH}	Propagation Delay, MR to Output	1.15	1.85	2.50	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.55	0.90	1.50	ns	
t_s	Set-Up Time Data to $\overline{\text{Enable}}$ MR to $\overline{\text{Enable}}$	 0.60 3.30	 0.20 2.20		ns	See Figure 2
t_h	Hold Time Data to $\overline{\text{Enable}}$ MR to $\overline{\text{Enable}}$	 0.30 -1.10	 -0.20 -2.20		ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING CIRCUITS AND WAVEFORMS



V_{CC} = +2 V, V_{EE} = -2.5 V
L_1 and L_2 = equal length 50Ω impedance lines
R_T equal 50Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50Ω to GND
C_L = Jig & Stray Capacitance ≤ 3 pF



$\overline{E}_a = \overline{E}_b$ = LOW

Fig. 1.

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t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

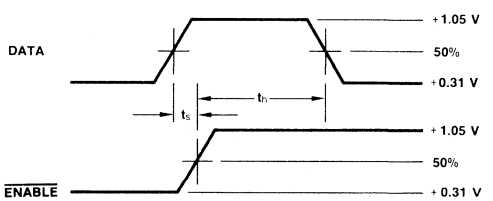


Fig. 2. Set-Up and Hold Times

F100151

HEX D FLIP-FLOP

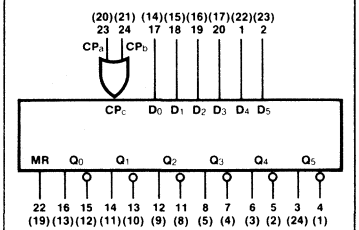
F100K SERIES ECL

DESCRIPTION — The F100151 contains six master/slave flip-flops with True and Complement outputs. A pair of Common Clock inputs (CP_a and CP_b) and common Master Reset (MR) input. Data enters a master when both CP_a and CP_b are LOW and transfers to the slave when CP_a or CP_b (or both) go HIGH. The MR inputs overrides all other inputs and makes the Q outputs LOW.

PIN NAMES

D_n	Inputs
MR	Asynchronous Master Reset
Q_n	True Outputs
$\overline{Q}_n$	Complement Outputs
CP_a and CP_b	Common Clock Inputs

LOGIC SYMBOL

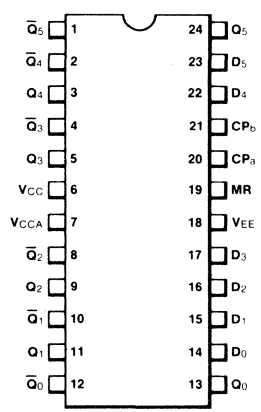


V_{CC} = Pin 9
V_{CCA} = Pin 10
V_{EE} = Pin 21

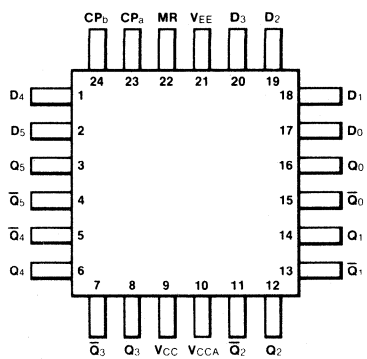
( ) = DIP

CONNECTION DIAGRAMS

DIP (TOP VIEW)



FLATPAK (TOP VIEW)

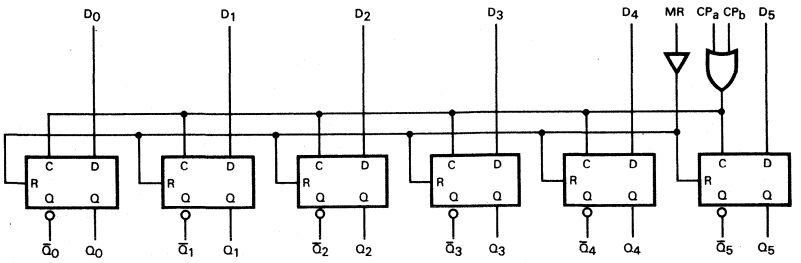


TRUTH TABLE
EACH FLIP-FLOP

D_n	CP_a	CP_b	MR	$Q_{n(t+1)}$
L	↑	L	L	L
H	↑	L	L	H
L	L	↑	L	L
H	L	↑	L	H
X	H	↑	L	$Q_{n(t)}$
X	↑	H	L	$Q_{n(t)}$
X	X	X	H	L

X = Immaterial
t,t+1 = Time before and after CP positive transition

LOGIC DIAGRAM



DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

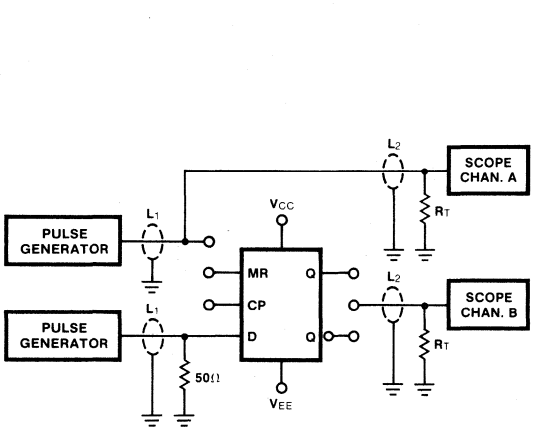
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
I_{IH}	Input Current HIGH MR Inputs Data Inputs Clock Inputs			 450 225 520	μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	-198	-141	-98	mA	Inputs open

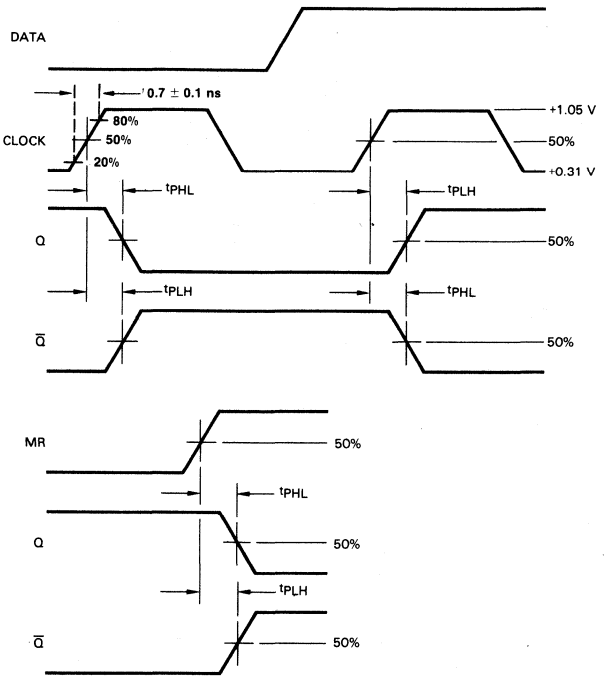
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PHL}, t_{PLH}	Propagation Delay, Clock to Output	0.95	1.60	2.10	ns	See Figure 1
t_{PLH}	Propagation Delay, MR to Output	1.35	2.25	3.00	ns	
t_{TLH}, t_{THL}	Transition Time (20% to 80%) (80% to 20%)	0.55	0.90	1.50	ns	
f_{TOG}	Toggle Frequency	400	550		MHz	See Figure 2
t_s	Set-Up Time Data to Clock MR to Clock	 0.60 1.50	 0.20 1.00		ns	See Figure 3
t_h	Hold Time Data to Clock MR to Clock	 0.30 -0.50	 -0.20 -1.00		ns	

NOTE: These limits apply to the flatpak. Add 200 ps maximum limit to propagation delays for the DIP package.

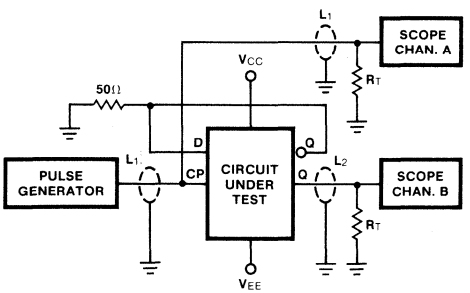
SWITCHING TEST CIRCUITS AND WAVEFORMS

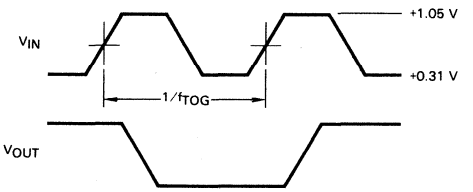




V_{CC} = +2 V, V_{EE} = −2.5 V
L_1 and L_2 = equal length 50Ω impedance lines
R_T equal 50Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50Ω to GND
C_L = Jig & Stray Capacitance ≤ 3 pF

Fig. 1 Propagation Delay





V_{CC} = +2 V, V_{EE} = −2.5 V
L_1 and L_2 = equal length 50Ω impedance lines
R_T equal 50Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50Ω to GND
C_L = Jig & Stray Capacitance ≤ 3 pF

Fig. 2 Toggle Frequency

t_s is the minimum time before the transition of the enable or clock that information must be present at the data input.

t_h is the minimum time after the transition of the enable or clock that information must remain unchanged at the data input.

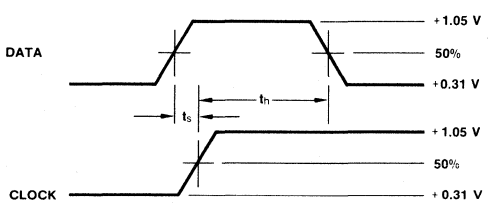


Fig. 3 Set-Up and Hold Times

F100155

QUAD MUX/LATCH

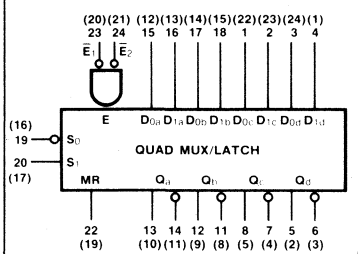
F100K SERIES ECL

DESCRIPTION – The F100155 contains four transparent latches, each of which can accept and store data from two sources. When both Enable ($\overline{E}_n$) inputs are LOW, the data that appears at an output is controlled by the Select (S_n) inputs, as shown in the operating mode table. In addition to routing data from either D_0 or D_1, the Select inputs can force the outputs LOW for the case where the latch is transparent (both Enables are LOW) and can steer a HIGH signal from either D_0 or D_1 to an output. The Select inputs can be tied together for applications requiring only that data be steered from either D_0 or D_1. A positive-going signal on either Enable input latches the outputs. A HIGH signal on the Master Reset (MR) input overrides all the other inputs and forces the Q outputs LOW.

PIN NAMES

$\overline{E}_n$	Enable Inputs
S_n	Select Inputs
MR	Master Reset
D_{nl}	Data Inputs
Q_n	Data Outputs

LOGIC SYMBOL

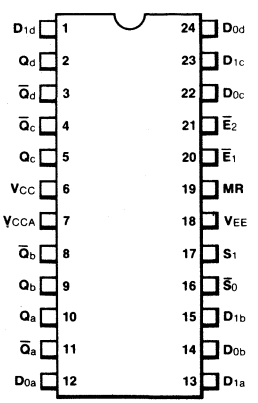


V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = 21 (18)

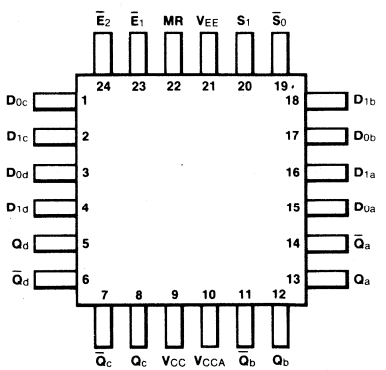
( ) = DIP

CONNECTION DIAGRAMS

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



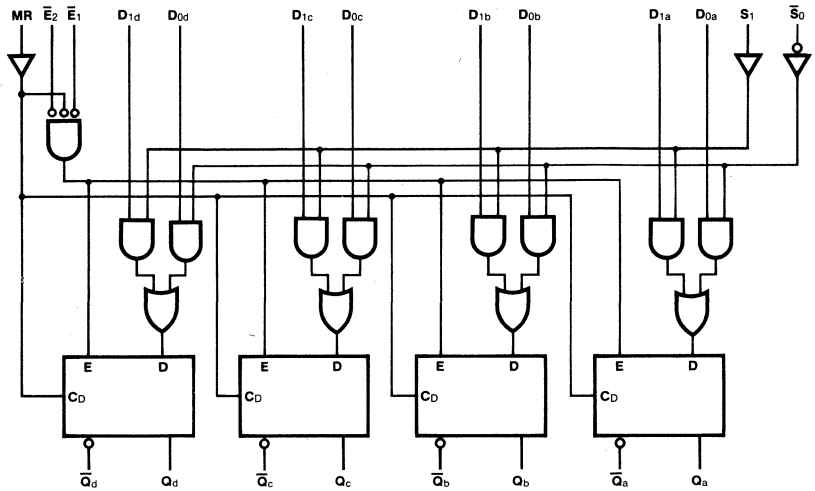
OPERATING MODE TABLE

CONTROLS				OUTPUTS
$\overline{E}_1$	$\overline{E}_2$	$\overline{S}_0$	S_1	Q_n
H	X	X	X	latched*
X	H	X	X	latched*
L	L	L	L	D_{0n}
L	L	L	H	$D_{0n} + D_{1n}$
L	L	H	L	L
L	L	H	H	D_{1n}

H = HIGH voltage level
L = LOW voltage level
X = Immaterial
* = Stores data present before $\overline{E}$ went HIGH

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LOGIC DIAGRAM



TRUTH TABLE

INPUTS							OUTPUTS	
MR	$\overline{E}_1$	$\overline{E}_2$	S_1	$\overline{S}_0$	D_{1a} D_{1b} D_{1c} D_{1d}	D_{0a} D_{0b} D_{0c} D_{0d}	$\overline{Q}_a$ $\overline{Q}_b$ $\overline{Q}_c$ $\overline{Q}_d$	Q_a Q_b Q_c Q_d
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	L	H	X	X	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	L	L	H	L	L	L	H	L
L	H	X	X	X	X	X	No Change	
L	X	H	X	X	X	X	No Change	

H = HIGH voltage level
L = LOW voltage level
X = Immaterial
* = Stores data present before $\overline{E}$ went HIGH

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

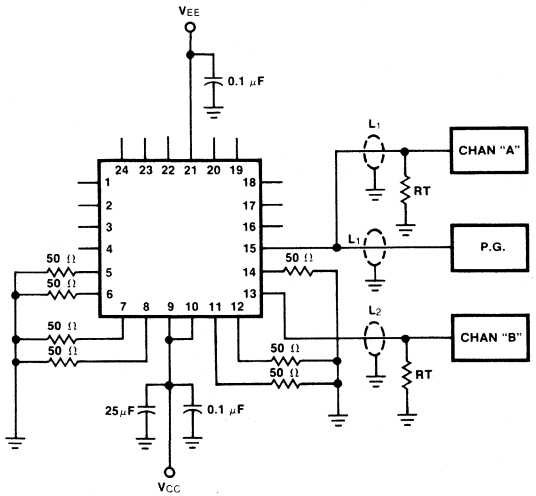
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
I_{IH}	Input Current HIGH				μA	$V_{IN} = V_{IHA}$
	S_n			220		
	$\overline{E}_n$			350		
	Data			340		
	MR			430		
I_{EE}	Supply Current	-133	-95	-66	mA	Inputs open

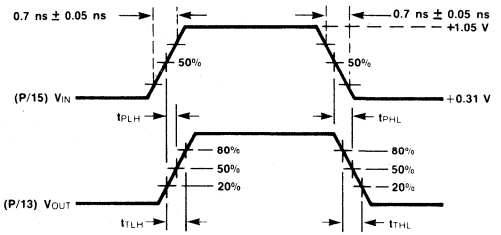
AC CHARACTERISTICS: $T_A = 25°C$, $V_{EE} = -4.5$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PHL} t_{PLH}	Propagation Delay, Data to Output	0.70	1.20	1.55	ns	See Figure 1
t_{PHL} t_{PLH}	Propagation Delay, Select to Output	1.50	2.50	3.25	ns	
t_{PHL} t_{PLH}	Propagation Delay, $\overline{\text{Enable}}$ to Output	1.00	1.70	2.20	ns	
t_{PHL} t_{PLH}	Propagation Delay, MR to Output	1.00	1.85	2.70	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.70	1.10	1.65	ns	
t_s	Set-Up Time				ns	See Figure 2
	Data to $\overline{\text{Enable}}$	0.60	0.30			
	Select to $\overline{\text{Enable}}$	2.30	1.50			
	MR to $\overline{\text{Enable}}$	1.50	1.00			
t_h	Hold Time				ns	
	Data to $\overline{\text{Enable}}$	0.30	-0.30			
	Select to $\overline{\text{Enable}}$	-0.50	-1.00			
	MR to $\overline{\text{Enable}}$	-0.70	-1.50			

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING TEST CIRCUIT AND WAVEFORMS





$V_{CC} = +2$ V, $V_{EE} = -2.5$ V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig & Stray Capacitance ≤ 3 pF

Fig. 1

t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

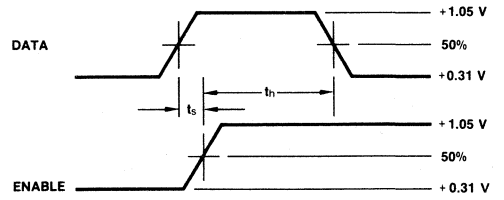


Fig. 2. Set-Up and Hold Times

F100156

MASK-MERGE

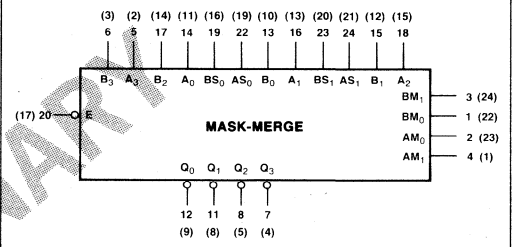
F100K SERIES ECL

DESCRIPTION – The F100156 merges two 4-bit words to form a 4-bit output word. The AM_j enable allows the merge of A_n into B_n by one, two, or three places (per the AS_j value) from the left. The BM_j enable similarly allows the merge of B_n into A_n from the left (per the BS_j value). The B_n merge overrides the A_n merge when both are enabled. This means A_n first merges into B_n and B_n then merges into the A_n merge. A B_n address (BS_j) greater than or equal to the A_n address (AS_j) thus forces the outputs to all B_n.

The merge outputs feed 4 latches, which have a common enable ($\overline{E}$) input. All inputs have a 50 kΩ (typical) pull-down resistor tied to V_{EE}. All four outputs do not have pull-down resistors, so they have wired "OR" capability and will require external resistors.

NOTE: When $\overline{E}$ is HIGH, $\overline{Q}_n$ outputs do not change.
When $\overline{E}$ is LOW, $\overline{Q}_n$ = A_n or B_n depending on which is selected.

LOGIC SYMBOL



V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)
( ) = DIP

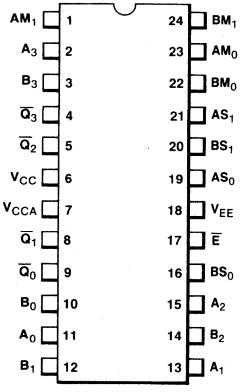
PIN NAMES

$\overline{E}$	Latch Enable Input
$\overline{Q}_n$	Data Outputs
A_n	Data Inputs
B_n	Data Inputs
AM_j	A Merge Enable Input
BM_j	B Merge Enable Input
AS_j	A_n Address Input
BS_j	B_n Address Input

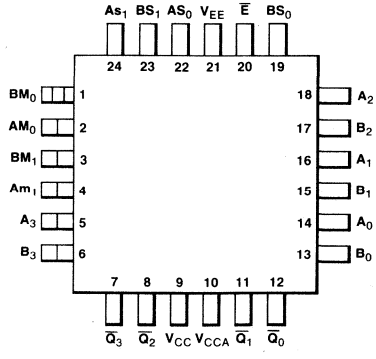
PRELIMINARY

CONNECTION DIAGRAMS

DIP (TOP VIEW)



FLATPAK (TOP VIEW)

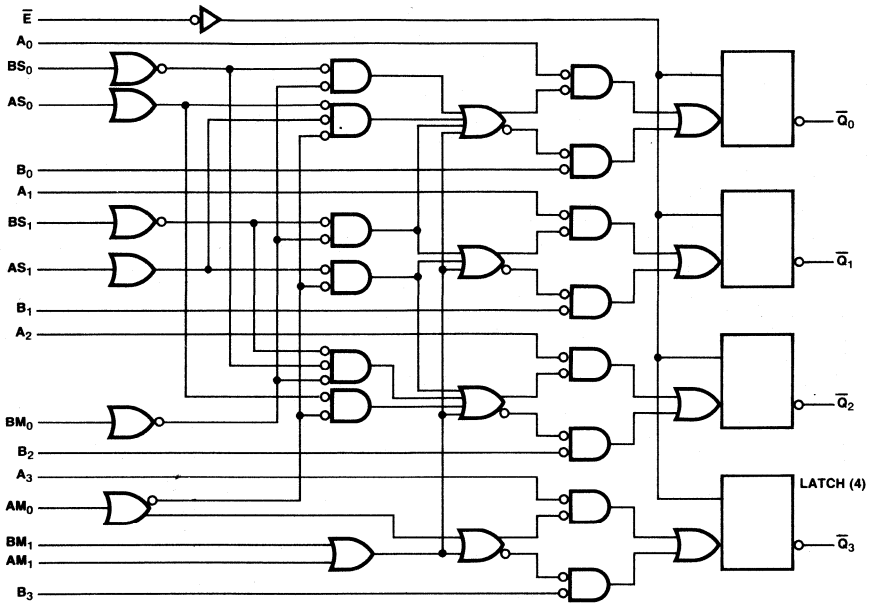


TRUTH TABLE

INPUTS									OUTPUTS				
BM_1	BM_0	AM_1	AM_0	BS_1	BS_0	AS_1	AS_0	$\overline{E}$	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	
X	X	H	X	X	X	X	X	L	B_0	B_1	B_2	B_3	
H	X	X	X	X	X	X	X	L	B_0	B_1	B_2	B_3	
L	L	L	L	X	X	X	X	L	A_0	A_1	A_2	A_3	
L	L	L	H	X	X	L	L	L	B_0	B_1	B_2	B_3	
L	L	L	H	X	X	L	H	L	A_0	B_1	B_2	B_3	
L	L	L	H	X	X	H	L	L	A_0	A_1	B_2	B_3	
L	L	L	H	X	X	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	L	L	L	X	X	L	A_0	A_1	A_2	A_3	
L	H	L	L	L	H	X	X	L	B_0	A_1	A_2	A_3	
L	H	L	L	H	L	X	X	L	B_0	B_1	A_2	A_3	
L	H	L	L	H	H	X	X	L	B_0	B_1	B_2	A_3	
L	H	L	H	L	L	L	H	L	A_0	B_1	B_2	B_3	
L	H	L	H	L	L	H	L	L	A_0	A_1	B_2	B_3	
L	H	L	H	L	L	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	H	L	H	H	L	L	B_0	A_1	B_2	B_3	
L	H	L	H	L	H	H	H	L	B_0	A_1	A_2	B_3	
L	H	L	H	H	L	H	H	L	B_0	B_1	A_2	B_3	
L	H	L	H	H	H	H	H	L	B_0	B_1	B_2	B_3	ADDRESS (BS) ≥ ADDRESS (AS)
L	H	L	H	H	H	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	L	L	L	L	B_0	B_1	B_2	B_3	
X	X	X	X	X	X	X	X	H	Q_0	Q_1	Q_2	Q_3	

H = HIGH Level
L = LOW Level
X = Don't Care
(Either H or L)

LOGIC DIAGRAM



DC CHARACTERISTICS: V_{EE} = −4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

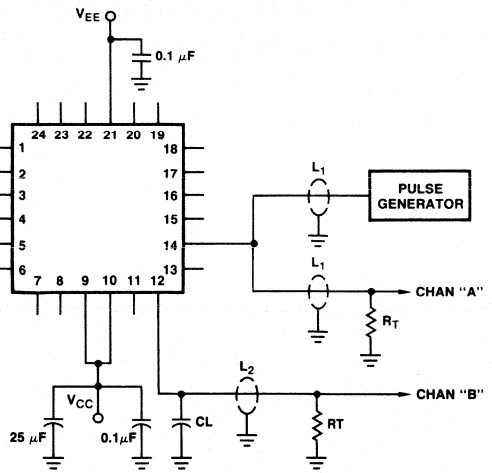
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
I_{IH}	Input Current HIGH A_n, B_n BM_j, AM_j, BS_j, AS_j, $\overline{E}$			 340 265	μA	V_{IN} = V_{IHA}
I_{EE}	Supply Current	−214	−153	−107	mA	Inputs Open

AC CHARACTERISTICS: T_A = 25°C, V_{EE} = −4.5 V, V_{CC} = GND

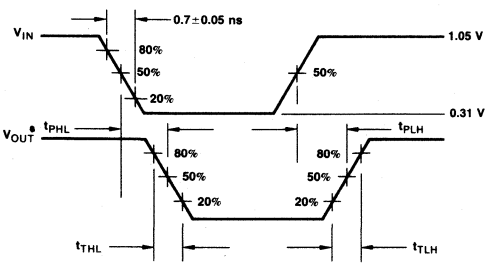
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PHL} t_{PLH}	Propagation Delay, A_n, B_n to $\overline{Q}_n$		1.10		ns	Figure 1
t_{PHL}, t_{PLH}	Propagation Delay, $\overline{E}$ to $\overline{Q}_n$		1.70		ns	
t_{PHL}, t_{PLH}	Propagation Delay, Address to $\overline{Q}_n$		2.70		ns	
t_{PHL} t_{PLH}	Propagation Delay AM_j, BM_j to $\overline{Q}_n$		2.70		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%		0.90		ns	
t_s	Set-Up Time Data to $\overline{E}$ AM_j, BM_j to $\overline{E}$ AS_j, BS_j to $\overline{E}$	 −0.30 2.30 2.30			ns	
t_h	Hold Time Data to $\overline{E}$ AM_j to $\overline{E}$ AS_j, BS_j to $\overline{E}$	 1.50 −0.70 −0.70			ns	

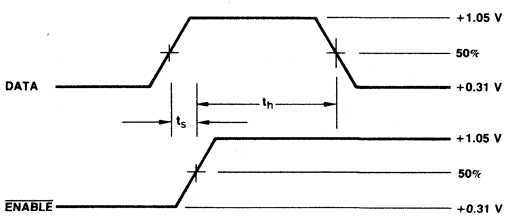
NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING TEST CIRCUIT AND WAVEFORMS



V_{CC} = +2 V, V_{EE} = −2.5 V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig and Stray Capacitance ≤ 3 pF





t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

Figure 1

10

F100158

8-BIT SHIFT MATRIX

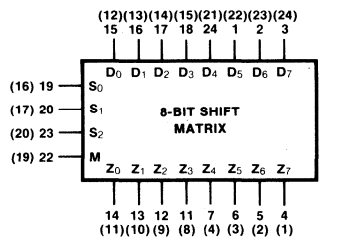
F100K SERIES ECL

DESCRIPTION — The F100158 contains a combinatorial network which performs the function of an 8-Bit Shift Matrix. Three control lines (S_n) are internally decoded and define the number of places which an 8-bit word present at the inputs (D_n) is shifted to the left and presented at the outputs (Z_n). A Mode Control input (M) is provided which if LOW, forces LOW all outputs to the right of the one that contain D_7. This operation is sometimes referred to as "LOW backfill". If M is HIGH, an end-round shift is performed such that D_0 appears at the output to the right of the one that contains D_7. This operation is commonly referred to as "barrel shifting".

PIN NAMES

D_n	Data Inputs
S_n	Select Inputs
M	Mode Control
Z_n	Data Outputs

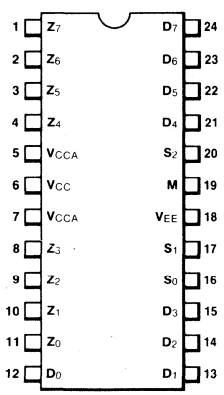
LOGIC SYMBOL



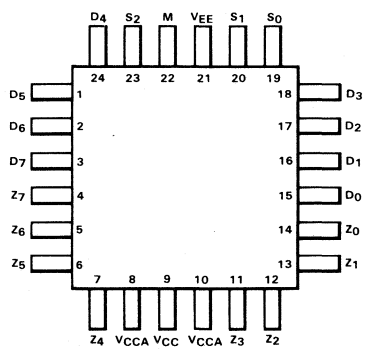
V_{CC} = Pin 9 (6)
V_{CCA} = Pins 8, 10 (5), (7)
V_{EE} = Pin 21 (18)
( ) = DIP

CONNECTION DIAGRAMS

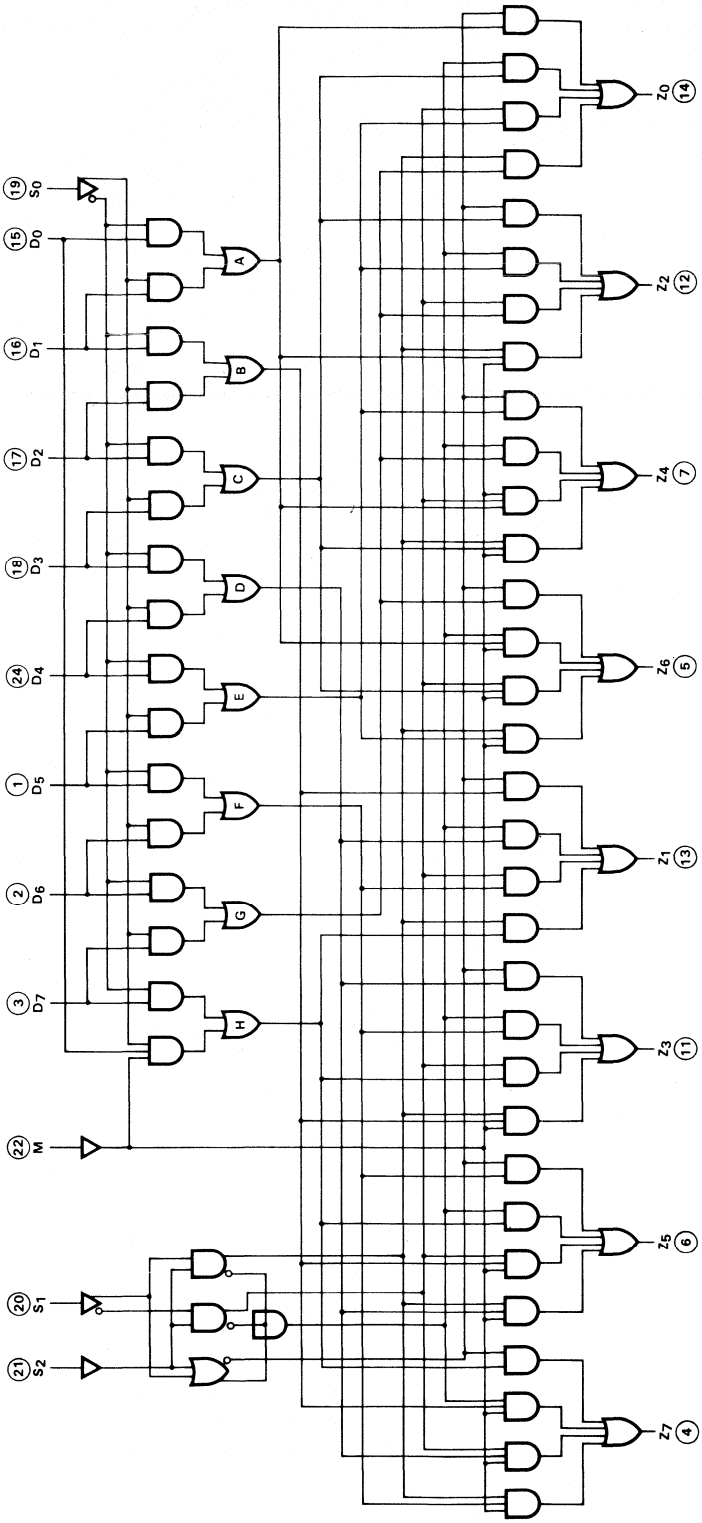
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



LOGIC DIAGRAM



V_{CC} = Pin 9
V_{CCA} = Pins 8, 10
V_{EE} = Pin 21

10

TRUTH TABLE

INPUTS				OUTPUTS							
M	S_0	S_1	S_2	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
X	L	L	L	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
L	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	L
L	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	L	L
L	H	H	L	D_3	D_4	D_5	D_6	D_7	L	L	L
L	L	L	H	D_4	D_5	D_6	D_7	L	L	L	L
L	H	L	H	D_5	D_6	D_7	L	L	L	L	L
L	L	H	H	D_6	D_7	L	L	L	L	L	L
L	H	H	H	D_7	L	L	L	L	L	L	L
H	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0
H	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1
H	H	H	L	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2
H	L	L	H	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3
H	H	L	H	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4
H	L	H	H	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5
H	H	H	H	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6

H = HIGH voltage level
L = LOW voltage level
X = Immaterial

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

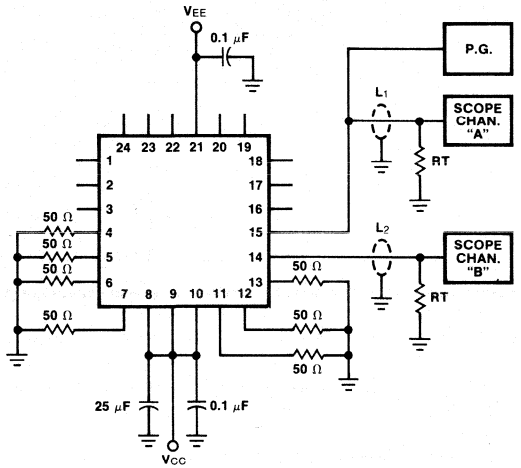
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH All Inputs			220	μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	-168	-120	-84	mA	Inputs open

AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL} t_{PLH}	Propagation Delay, D_n to Output	1.10	1.80	2.70	ns	See Switching and Waveforms, Figure 1
t_{PHL} t_{PLH}	Propagation Delay, M to Output	2.00	2.30	4.90	ns	
t_{PHL} t_{PLH}	Propagation Delay, S_n to Output	1.90	2.30	4.70	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	1.55	2.20	ns	

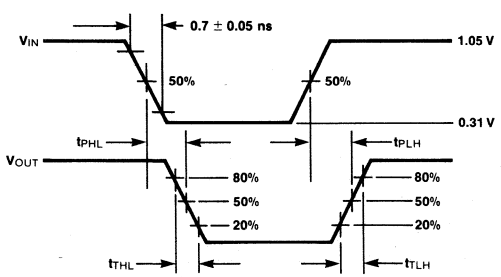
NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING TEST CIRCUIT AND WAVEFORMS



V_{CC} = +2 V, V_{EE} = -2.5 V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig & Stray Capacitance ≤ 3pF

WAVEFORM I



WAVEFORM II

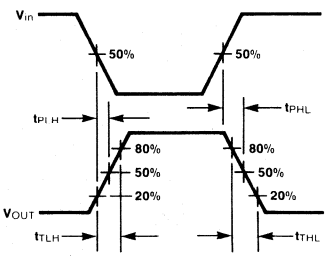


Fig. 1

APPLICATIONS

The following technique uses two ranks of F100158s to shift a 64-bit word from 0 to 63 places. Although two stage delays are required (one for each rank), the total shift only takes about 4 ns. This technique performs a bit shift on each 8-bit byte in the first rank and then a modulo-8 byte shift on the 64-bit word in the second rank.

BASIC 16-BIT 0 — 7 PLACE SHIFTER

Figure 2 shows the basic 0—7 place shift technique which can be expanded to accomodate any word length. Each 8-bit byte requires a pair of F100158s operating in the LOW backfill mode. The address lines for each pair of ICs are driven out of phase by three OR gates. Inputs for the two ICs are taken from two bytes transposed in order; outputs are transposed and emitter-OR tied. One device shifts right from location 0 and the other shifts left from location 7. The bits shifted off one pair are picked up by the next pair of F100158s or — in the case of the last one in the rank — returned to the first device. The net result is a 0 — 7 place shift of the entire word.

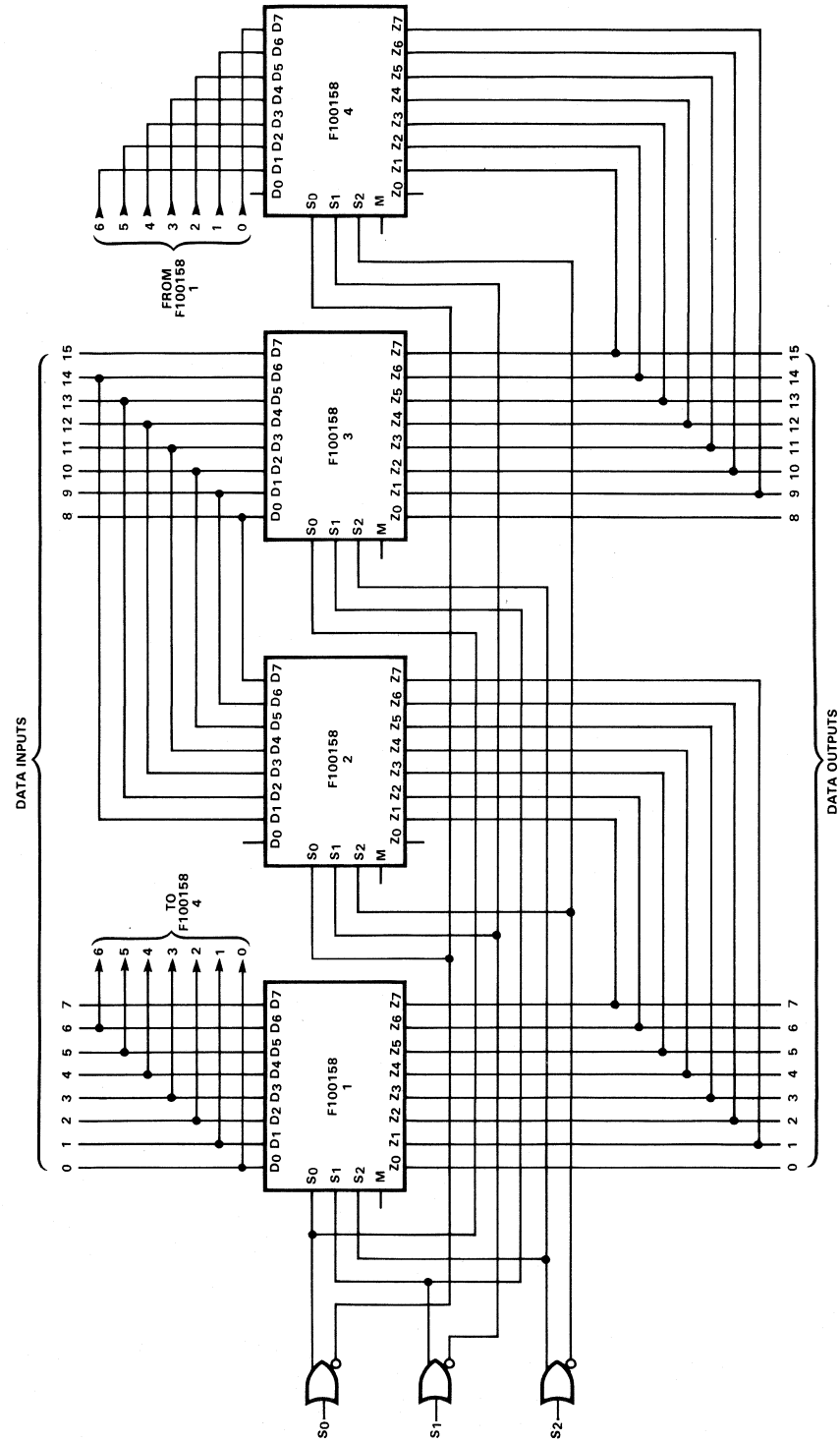


Fig. 2 Basic 16-Bit 0 — 7 Place Shifter

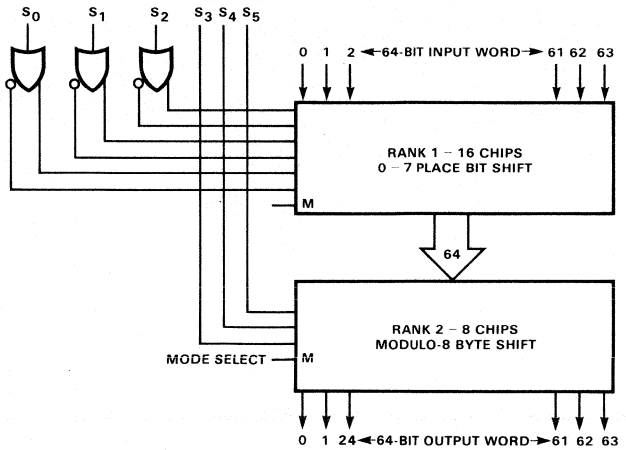


Fig. 3 64-Bit 0 — Place Barrel Shifter

EXPANDING TO 64-BIT WORD AND 64-PLACE SHIFT

This basic 0 — 7 place shift technique can be expanded to accomodate a 64-bit word shifted from 0 to 63 places, however two ranks of F100158s are required *(Figure 3)*. The first rank is identical to the one illustrated in *Figure 2* except it contains a total of 16 devices. The second rank consists of eight additional F100158s connected in the modulo-8 configuration shown in *Figure 4*.

The modulo-8 rank is used to simulate an 8-bit simultaneous shift since the F100158 cannot shift in 8-bit jumps. The modulo-8 configuration is achieved by wiring the first rank and the output device to the second rank as illustrated in blue in *Figure 4*. The LSB of each output byte in the first rank is wired to one of the eight inputs of the first F100158 in the second rank. The next least significant bit of each first-rank F100158 pair, however, is connected to the inputs of the second F100158 in the second rank. The other first-ranked outputs are connected in a similar fashion to the remainder of the second-rank inputs. Ultimately, the outputs of the second rank must then be connected to reform the final usable 64-bit word so that the bits are again ordered from 0 — 63.

The effect is that each single-location shift in the second rank appears to be an eight place shift in the final word due to the way the inputs and outputs of the second rank are connected. The combination of the two ranks produces the 64-place shift of the entire word.

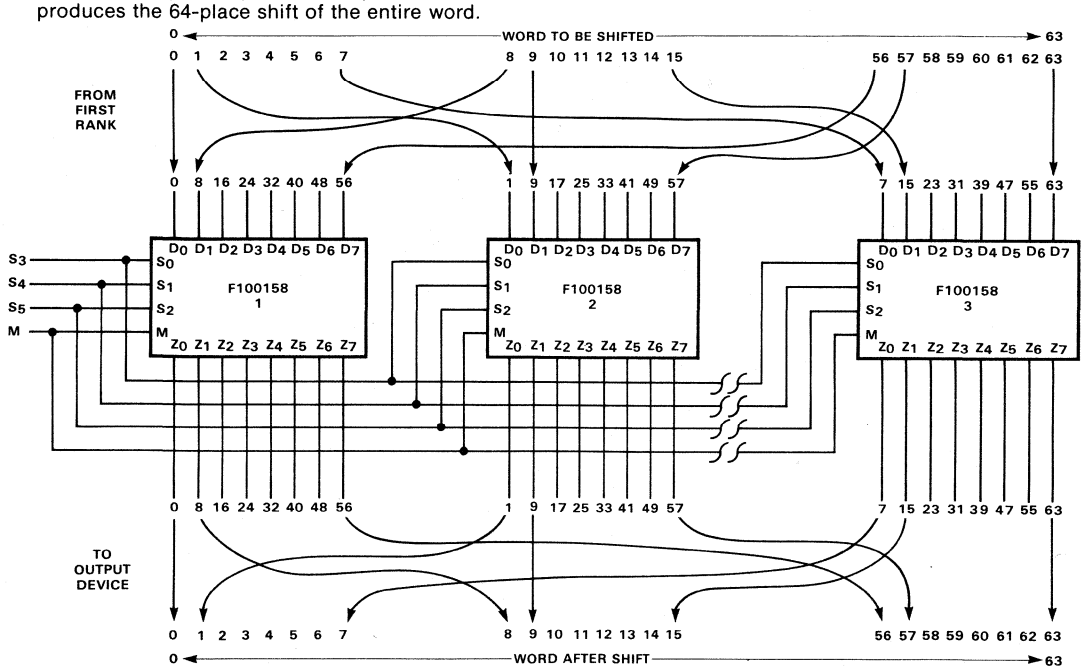


Fig. 4 Modulo-8 Shift

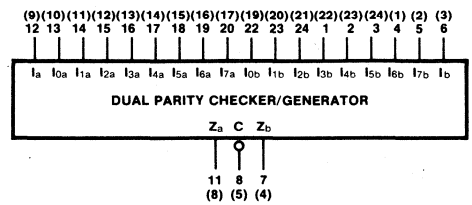
F100160

DUAL PARITY CHECKER/GENERATOR

F100K SERIES ECL

DESCRIPTION — The F100160 is a Dual Parity Checker/Generator. Each half has nine inputs, with the output being HIGH when an even number of inputs are HIGH. One of the nine inputs (I_a or I_b) has the shorter through-put delay and is therefore preferred as the expansion input for generating parity for 16 or more bits. The F100160 also has a Compare ($\overline{C}$) output which allows the circuit to compare two 8-bit words. The C output is LOW when the two words match, bit for bit.

LOGIC SYMBOL



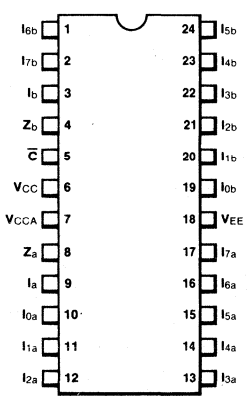
V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)
( ) = DIP

PIN NAMES

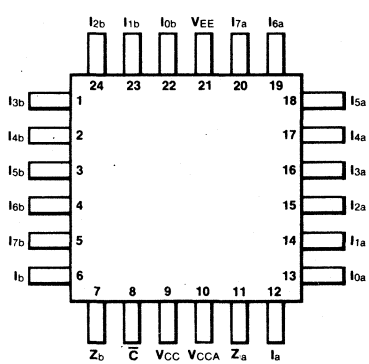
I_n	Data Inputs
$\underline{Z}$	Parity Odd
$\overline{C}$	Compare Output

CONNECTION DIAGRAMS

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



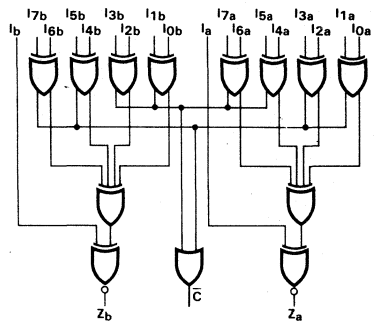
TRUTH TABLE
(Each Half)

Sum of HIGH Inputs	Output Z
EVEN	HIGH
ODD	LOW

Comparator Function:

$\overline{C} = (13 \oplus 14) + (15 \oplus 16) + (17 \oplus 18) + (19 \oplus 20) + (22 \oplus 23) + (24 \oplus 1) + (2 \oplus 3) + (4 \oplus 5)$

LOGIC DIAGRAM



DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
I_{IH}	Input Current HIGH I_b, I_a Others			 340 220	μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	-115	-82	-57	mA	Inputs open

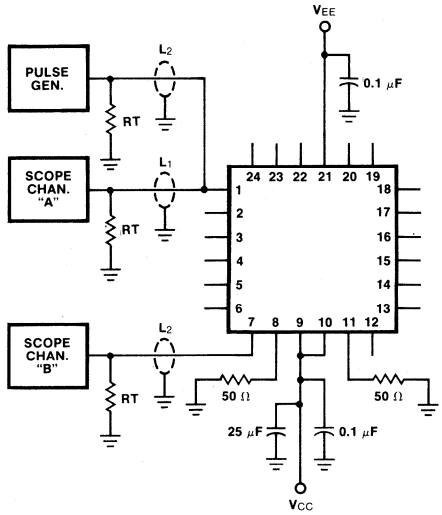
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

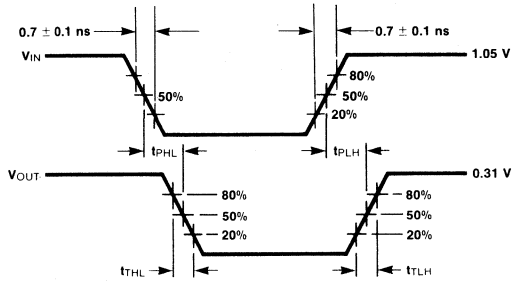
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PHL} t_{PLH}	Propagation Delay, I_{na}, I_{nb} to Z	1.80	3.00	3.90	ns	Figure 1
t_{PHL} t_{PLH}	Propagation Delay, I_{na}, I_{nb} to $\overline{C}$	1.30	2.20	2.90	ns	
t_{PHL} t_{PLH}	Propagation Delay, I_a, I_b to Z	0.60	1.05	1.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.00	1.65	ns	

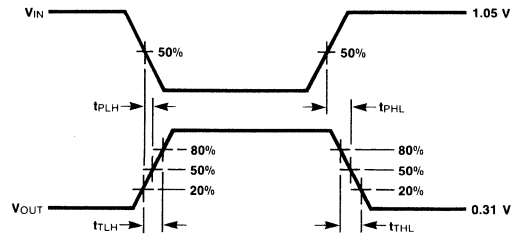
NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

10

SWITCHING TEST CIRCUIT AND WAVEFORMS







V_{CC} = +2 V, V_{EE} = -2.5 V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig & Stray Capacitances ≤ 3 pF

Fig. 1

F100163

DUAL 8-INPUT MULTIPLEXER

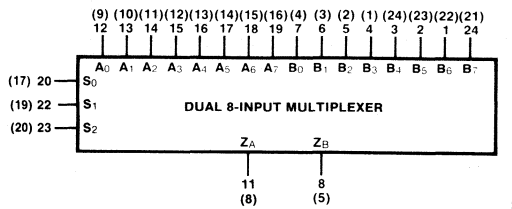
F100K SERIES ECL

DESCRIPTION — The F100163 is a dual 8-Input Multiplexer. The Data Select (Sn) inputs determine which bit (An and Bn) will be presented at the Outputs (Z_A and Z_B respectively). The same bit (0-7) will be selected for both the Z_A and Z_B output.

PIN NAMES

Z_n	Data Outputs
S_n	Data Selects
An, Bn	Data Inputs

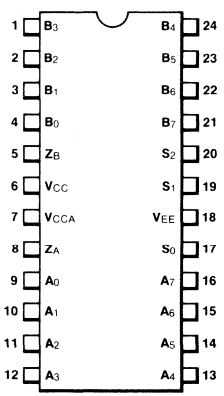
LOGIC SYMBOL



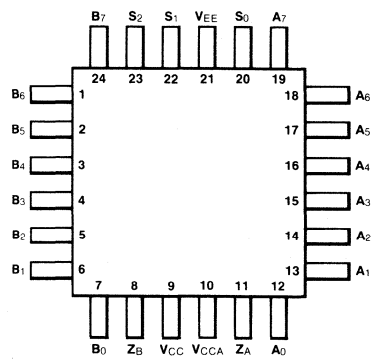
V_{CC} = 9 (6)
V_{CCA} = 10 (7)
V_{EE} = 21 (18)

CONNECTION DIAGRAMS

DIP (TOP VIEW)

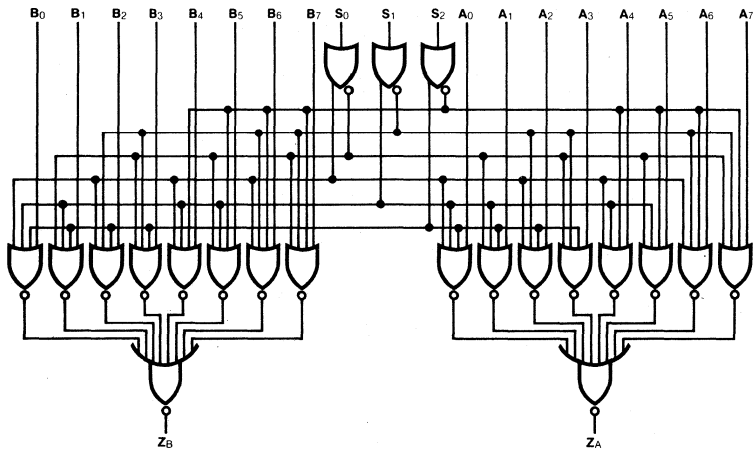


FLATPAK (TOP VIEW)



10

LOGIC DIAGRAM



PARTIAL TRUTH TABLE

INPUTS											OUTPUT
ADDRESS			DATA								
S_2	S_1	S_0	A_7 B_7	A_6 B_6	A_5 B_5	A_4 B_4	A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0	Z_A Z_B
L L	L L	L L								L H	L H
L L	L L	H H							L H		L H
L L	H H	L L						L H			L H
L L	H H	H H					L H				L H
H H	L L	L L				L H					L H
H H	L L	H H			L H						L H
H H	H H	L L		L H							L H
H H	H H	H H	L H								L H

H = High Level
L = Low Level
Blank = X = Irrelevant

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C +85°C

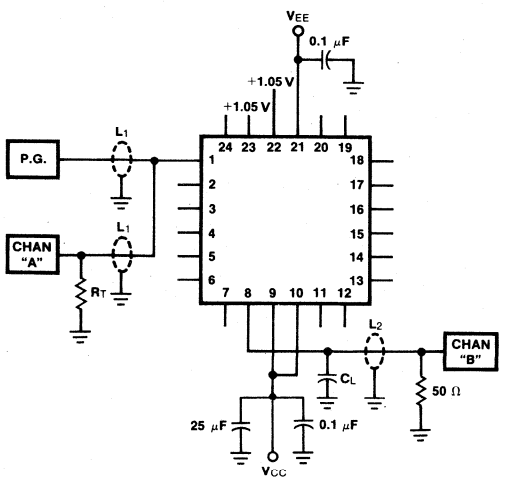
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH S_n A_n, B_n			 265 340	 μA	 $V_{IN} = V_{IHA}$
C_I	Input Capacitance S_n A_n, B_n			 4.0 6.0	 pF	
I_{EE}	Supply Current	-153	-109	-76	mA	Inputs Open

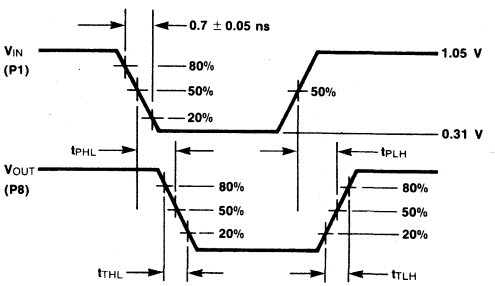
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL} t_{PLH}	Propagation Delay, Data to Output	0.08	1.30	1.70	ns	Figure 1
t_{PHL} t_{PLH}	Propagation Delay Select to Output	1.50	1.95	2.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.70	1.20	1.70	ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING TEST CIRCUIT AND WAVEFORMS





L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig and stray capacitance ≤ 3 pF

Fig 1

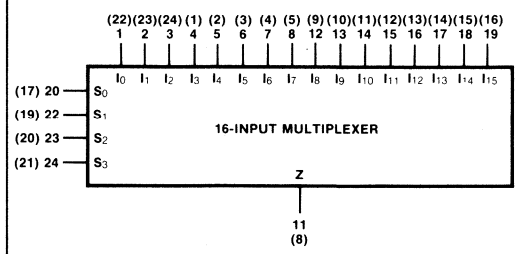
F100164

16-INPUT MULTIPLEXER

F100K SERIES ECL

DESCRIPTION — The F100164 is a 16-Input Multiplexer. Data paths are controlled by four select lines (S_0 — S_3). Their decoding is shown in the truth table. Output data polarity is the same as the selected input data.

LOGIC SYMBOL



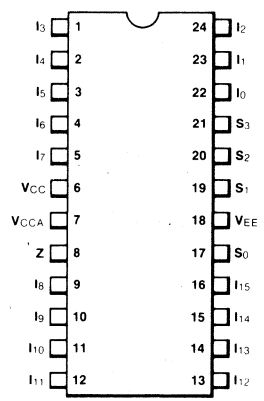
V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)
( ) = DIP

PIN NAMES

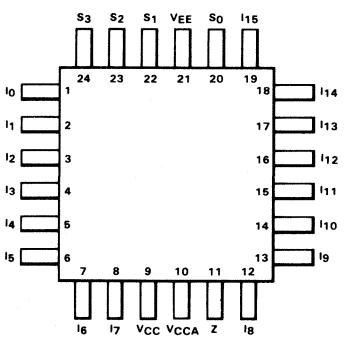
I_n	Data Inputs
S_n	Select Inputs
Z	Data Output

CONNECTION DIAGRAMS

DIP (TOP VIEW)



FLATPAK (TOP VIEW)

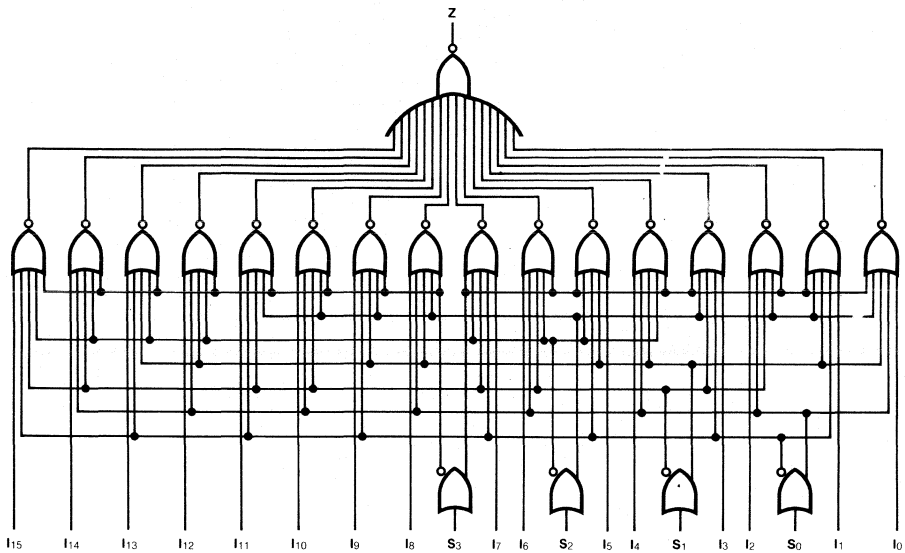


TRUTH TABLE

S_0	S_1	S_2	S_3	Z
L	L	L	L	I_0
H	L	L	L	I_1
L	H	L	L	I_2
H	H	L	L	I_3
L	L	H	L	I_4
H	L	H	L	I_5
L	H	H	L	I_6
H	H	H	L	I_7
L	L	L	H	I_8
H	L	L	H	I_9
L	H	L	H	I_{10}
H	H	L	H	I_{11}
L	L	H	H	I_{12}
H	L	H	H	I_{13}
L	H	H	H	I_{14}
H	H	H	H	I_{15}

H = HIGH voltage level
L = LOW voltage level

LOGIC DIAGRAM



DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
I_{IH}	Input Current HIGH				μA	$V_{IN} = V_{IHA}$
	I_n			280		
	S_0, S_1			240		
	S_2, S_3			200		
I_{EE}	Supply Current	-98	-70	-49	mA	Inputs open

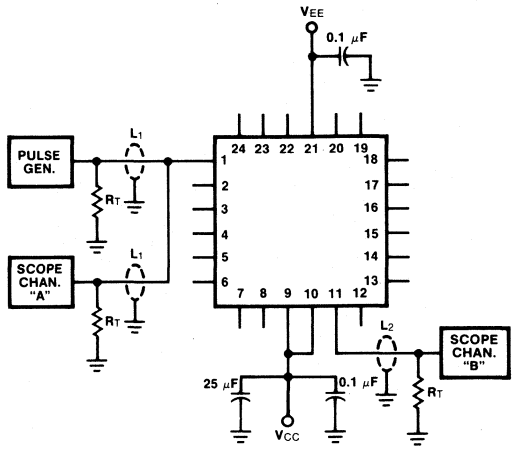
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

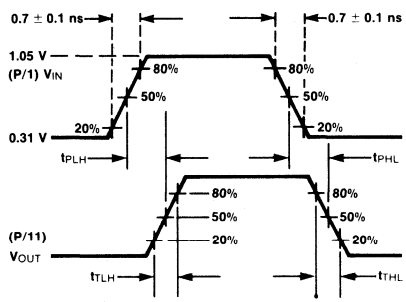
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PHL} t_{PLH}	Propagation Delay, I_n to Z	1.0	1.65	2.15	ns	See Switching and Waveforms
t_{PHL} t_{PLH}	Propagation Delay, S_0/S_1 to Z	1.45	2.40	3.20	ns	
t_{PHL} t_{PLH}	Propagation Delay, S_2/S_3 to Z	1.10	1.85	2.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.65	1.00	1.60	ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

10

SWITCHING TEST CIRCUIT AND WAVEFORMS





V_{CC} = +2 V, V_{EE} = −2.5 V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig & Stray Capacitance ≤ 3 pF

F100165

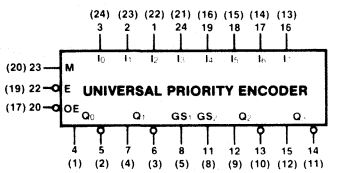
UNIVERSAL PRIORITY ENCODER

F100K SERIES ECL

DESCRIPTION – The F100165 contains eight input latches with a Common Enable ($\overline{E}$) followed by encoding logic which generates the binary address of the highest priority input having a HIGH signal. The circuit operates as a dual 4-input encoder when the Mode Control input (M) is LOW, and as a single 8-input encoder when M is HIGH. In the 8-input mode, Q_0, Q_1 and Q_2 are the relevant outputs, I_0 is the highest priority input and GS_1 is the relevant Group Signal output. In the dual mode, Q_0, Q_1 and GS_1 operate with $I_0 - I_3$. Q_2, Q_3 and GS_2 operate with $I_4 - I_7$. A GS output goes LOW when its pertinent inputs are all LOW.

inputs are latched when $\overline{E}$ goes HIGH. A HIGH signal on the Output Enable ($\overline{OE}$) input forces all Q outputs LOW and GS outputs HIGH. Expansion to accommodate more inputs can be done by connecting the GS output of a higher priority group to the $\overline{OE}$ input of the next lower priority group.

LOGIC SYMBOL

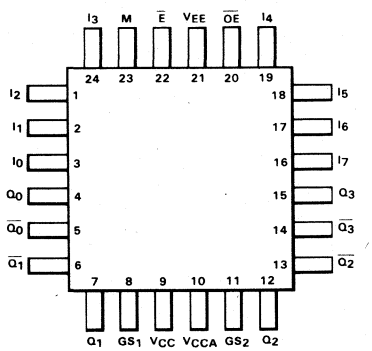


V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)
( ) = DIP

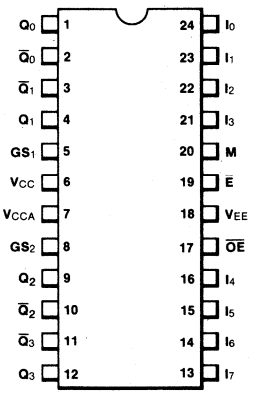
PIN NAMES

I_n	Data Inputs
$\overline{E}$	Input Enable
$\overline{OE}$	Output Enable
M	Mode Control
GS_n	Group Signal Output
Q_n	Data Outputs

CONNECTION DIAGRAM
DIP (TOP VIEW)

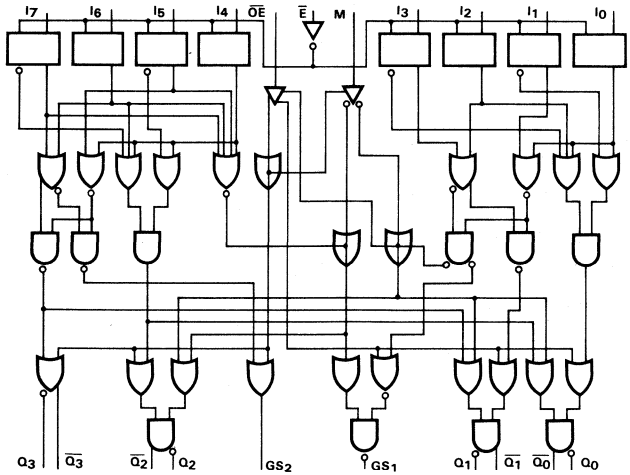


CONNECTION DIAGRAM
DIP (TOP VIEW)



10

LOGIC DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{OE}$	M	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Q_0	Q_1	Q_2	Q_3	GS_1	GS_2
L	L	L	H	X	X	X					L	L			H	
L	L	L	L	H	X	X					H	L			H	
L	L	L	L	L	H	X					L	H			H	
L	L	L	L	L	L	H					H	H			H	
L	L	L	L	L	L	L					L	L			L	
L	L	L					H	X	X	X			L	L		H
L	L	L					L	H	X	X			H	L		H
L	L	L					L	L	H	X			L	H		H
L	L	L					L	L	L	H			H	H		H
L	L	L					L	L	L	L			L	L		L
L	L	H	H	X	X	X	X	X	X	X	L	L	L	L	H	H
L	L	H	L	H	X	X	X	X	X	X	H	L	L	L	H	H
L	L	H	L	L	H	X	X	X	X	X	L	H	L	L	H	H
L	L	H	L	L	L	H	X	X	X	X	H	H	L	L	H	H
L	L	H	L	L	L	L	H	X	X	X	L	L	H	L	H	H
L	L	H	L	L	L	L	L	H	X	X	H	L	H	L	H	H
L	L	H	L	L	L	L	L	L	H	X	L	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	H	H	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H
X	H	X	X	X	X	X	X	X	X	X	L	L	L	L	H	H
H	L	L	X	X	X	X	X	X	X	X	Given by I_0-I_7 when E was low and M=L					
H	L	H	X	X	X	X	X	X	X	X	Given by I_0-I_7 when E was low and M=H					

H = High Level (Most Positive)
L = Low Level (Most Negative)
Blank = X = Don't Care (May be either High or Low)

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

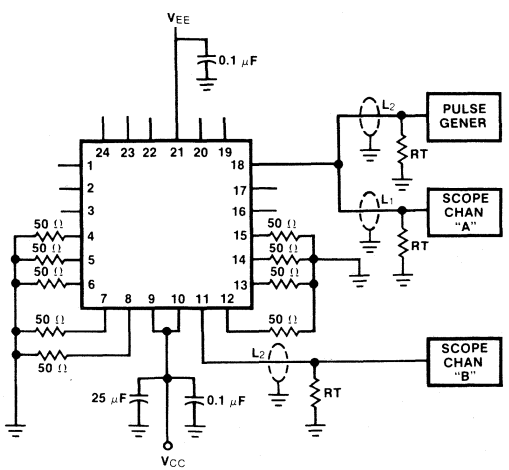
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH All Inputs			230	μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	-154	-110	-77	mA	Inputs open

AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL} t_{PLH}	Propagation Delay, Data to Q Outputs	2.10	3.00	3.90	ns	See Switching and Waveforms
t_{PHL} t_{PLH}	Propagation Delay, Data to GS Outputs	2.10	3.00	3.90	ns	
t_{PHL} t_{PLH}	Propagation Delay, $\overline{OE}$ to Q Outputs	1.0	3.00	3.40	ns	
t_{PHL} t_{PLH}	Propagation Delay, $\overline{OE}$ to GS Outputs	1.0	3.00	3.40	ns	
t_{PHL} t_{PLH}	Propagation Delay, M to Q Outputs	1.0	3.00	3.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	1.10	1.70	ns	

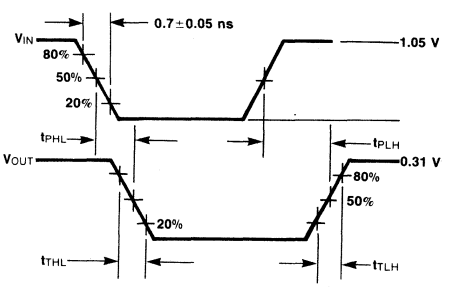
NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING AND WAVEFORMS

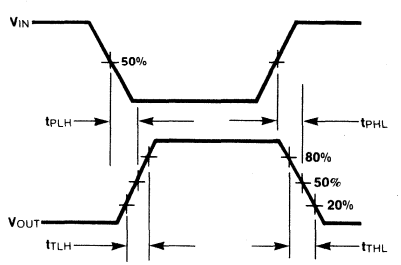


V_{CC} = +2 V, V_{EE} = -2.5 V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig & Stray Capacitance ≤ 3 pF

WAVEFORM I



WAVEFORM II



10

F100166

9-BIT COMPARATOR

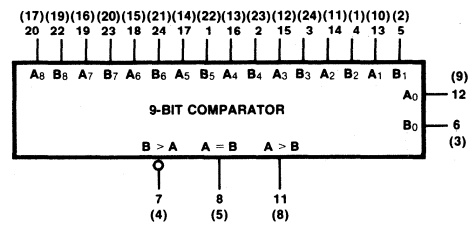
F100K SERIES ECL

DESCRIPTION – The F100166 is a 9-Bit Magnitude Comparator which compares the arithmetic value of two 9-bit words and indicates whether one word is greater than, or equal to the other. The outputs do not have pull down resistors, which provides the wire OR functions by tying several outputs together.

PIN NAMES

A_n	Data Inputs
B_n	Data Inputs
$\overline{B > A}$	Compare Outputs
A = B	Compare Outputs
A > B	Compare Outputs

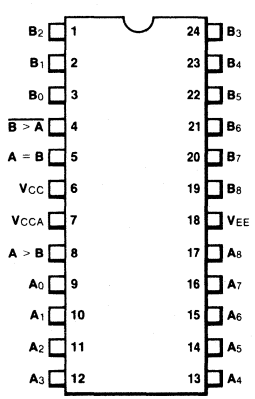
LOGIC SYMBOL



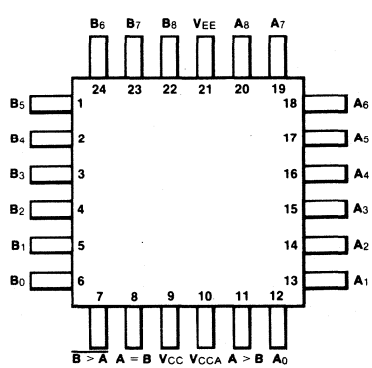
V_{CC} = 9 (6)
V_{CCA} = 10 (7)
V_{EE} = 21 (18)
( ) = DIP

CONNECTION DIAGRAMS

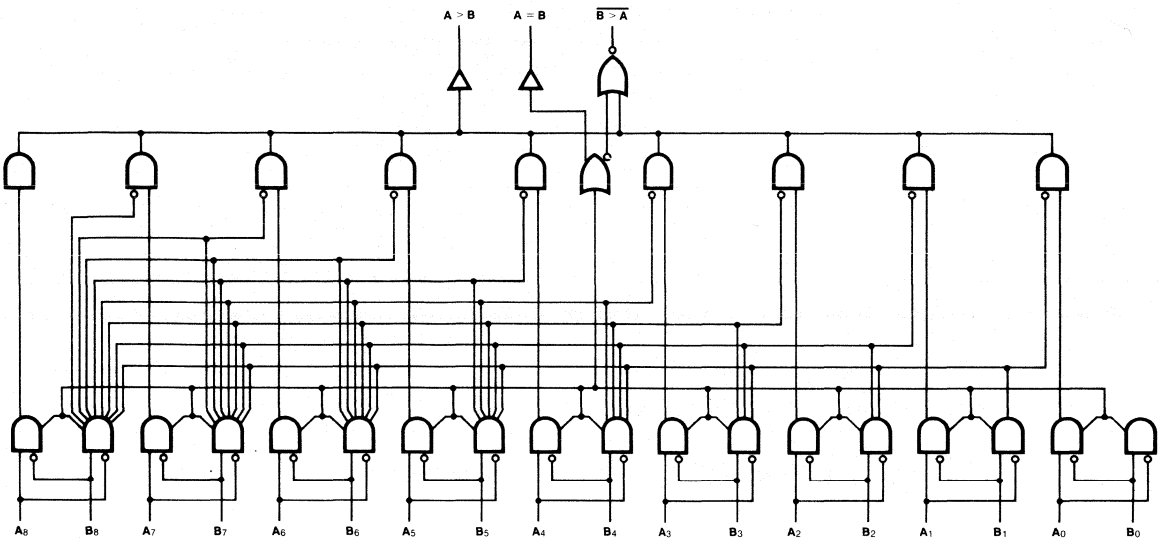
FLATPAK (TOP VIEW)



DIP (TOP VIEW)



LOGIC DIAGRAM



TRUTH TABLE

INPUTS									OUTPUTS		
A_8B_8	A_7B_7	A_6B_6	A_5B_5	A_4B_4	A_3B_3	A_2B_2	A_1B_1	A_0B_0	A > B	$\overline{B > A}$	A = B
H L									H	L	H
L H									L	H	H
$A_8=B_8$	H L								H	L	H
$A_8=B_8$	L H								L	H	H
$A_8=B_8$	$A_7=B_7$	H L							H	L	H
$A_8=B_8$	$A_7=B_7$	L H							L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	H L						H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	L H						L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	H L					H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	L H					L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	H L				H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	L H				L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	H L			H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	L H			L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	H L		H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	L H		L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	H L	H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	L H	L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L

H = HIGH; L = LOW; Blank = Don't Care (Either H or L)

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

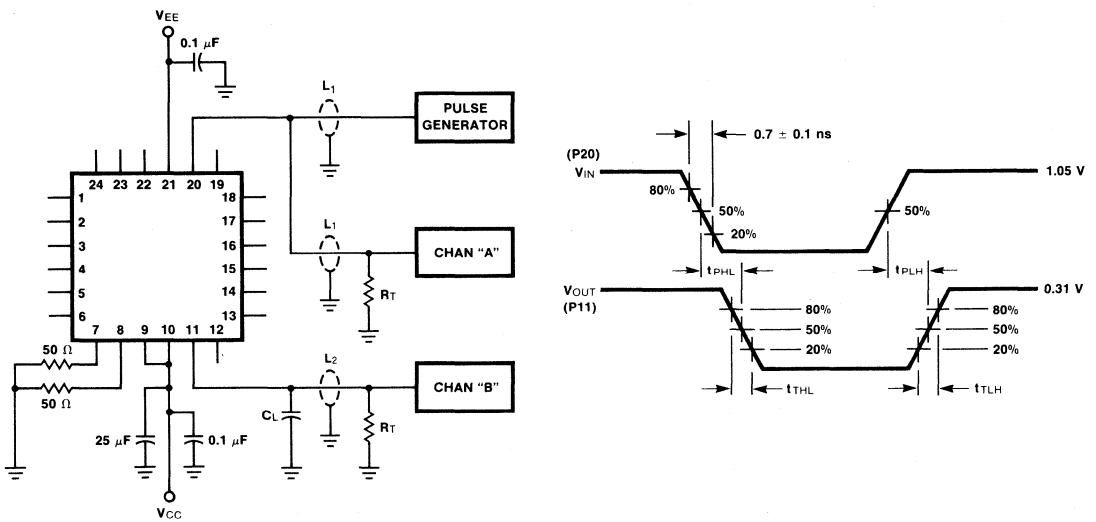
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH			250	μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	-238	-170	-119	mA	Inputs Open

AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL}, t_{PLH}	Propagation Delay	1.55	2.70	4.30	ns	Figure 1
t_{TLH}, t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	1.00	1.80	ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING TEST CIRCUIT AND WAVEFORM



V_{CC} = +2 V, V_{EE} = -2.5 V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig & Stray Capacitance ≤ 3 pF

Fig. 1

F100170

UNIVERSAL DEMUX/DECODE

F100K SERIES ECL

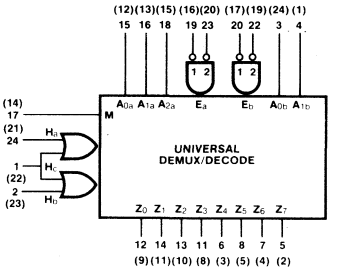
DESCRIPTION – The F100170 Universal Demux/Decoder functions as either a dual 1-of-4 decoder or as a single 1-of-8 decoder, depending on the signal applied to the Mode Control input (M). In the dual mode, each half has a pair of active LOW Enable (E) inputs. Pin assignments for the $\overline{E}$ inputs are such that in the 1-of-8 mode they can easily be tied together in pairs to provide two active LOW enables (pin 19 to 20 and Pin 22 to 23). Signals applied to auxiliary inputs H_a, H_b and H_c determine whether the outputs are active HIGH or active LOW. In the dual 1-of-4 mode the address inputs are A_{0a}, A_{1a} and A_{0b}, A_{1b} with A_{2a} unused (*i.e.*, left open, tied to V_{EE} or with LOW signal applied). In the 1-of-8 mode, the address inputs are A_{0a}, A_{1a}, A_{2a} with A_{0b} and A_{1b} LOW or open.

PIN NAMES

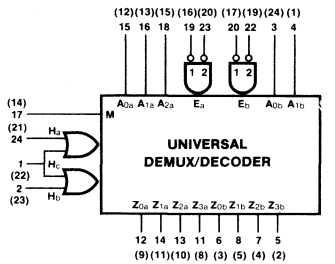
A_{nl}	Address Inputs
E_j	Enable Inputs
M	Mode Control
H_j	Auxiliary Inputs
Z_{nj}	Outputs

LOGIC SYMBOL

Single 1-of-8 Application



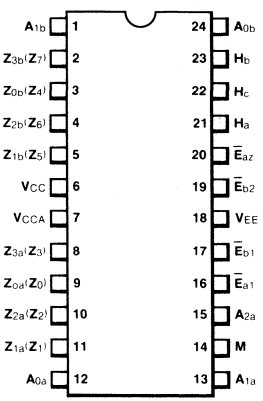
Dual 1-of-4 Application



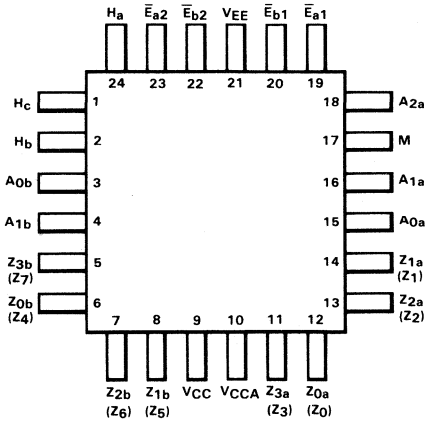
V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)
( ) = DIP

CONNECTION DIAGRAMS

DIP (TOP VIEW)

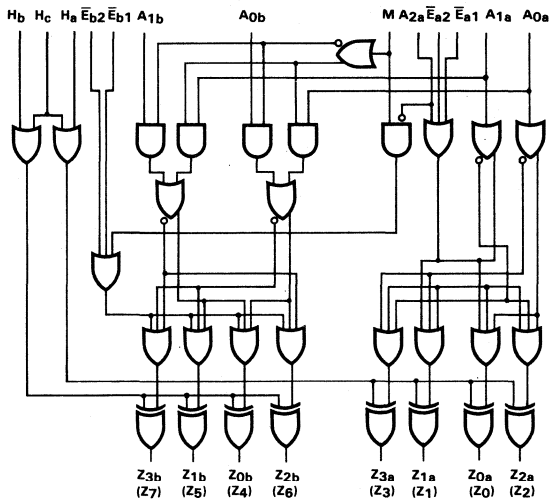


FLATPAK (TOP VIEW)



(Z_n) for 1-of-4 applications

LOGIC DIAGRAM



TRUTH TABLE

Dual 1-of-4 Mode
$M = A_{2a} = H_c$ = LOW

Inputs				Active HIGH Outputs (H_a and H_b inputs HIGH)				Active LOW Outputs (H_a and H_b inputs LOW)			
$\overline{E}_{a1}$ $\overline{E}_{b1}$	$\overline{E}_{a2}$ $\overline{E}_{b2}$	A_{1a} A_{1b}	A_{0a} A_{0b}	Z_{0a} Z_{0b}	Z_{1a} Z_{1b}	Z_{2a} Z_{2b}	Z_{3a} Z_{3b}	Z_{0a} Z_{0b}	Z_{1a} Z_{1b}	Z_{2a} Z_{2b}	Z_{3a} Z_{3b}
H	X	X	X	L	L	L	L	H	H	H	H
X	H	X	X	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

L = LOW voltage level
H = HIGH voltage level
X = Don't care

TRUTH TABLE

Single 1-of-8 Mode
M = HIGH; $A_{0b} = A_{1b} = H_a = H_b$ = LOW

Inputs					Active HIGH Outputs* (H_c input HIGH)							
$\overline{E}_1$	$\overline{E}_2$	A_{2a}	A_{1a}	A_{0a}	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

L = LOW voltage level
H = HIGH voltage level
X = Immaterial
*for H_c = LOW, output states are complemented
$E_1 = E_{a1}$ and E_{b1} wired; $E_2 = E_{a2}$ and E_{b2} wired

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH H_c, A_{0a}, A_{1a}, A_{2a} All Other Inputs			 310 250	μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	-153	-109	-76	mA	Inputs open

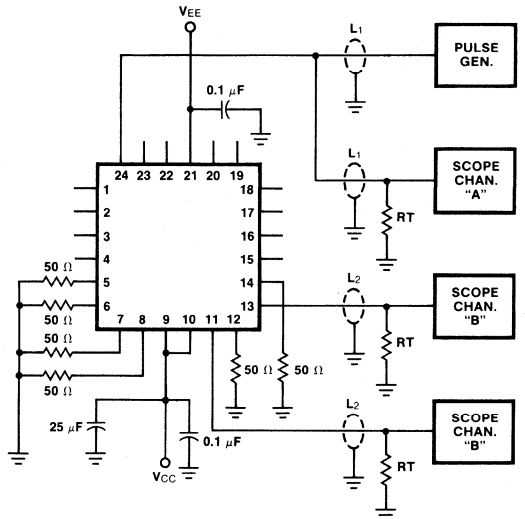
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

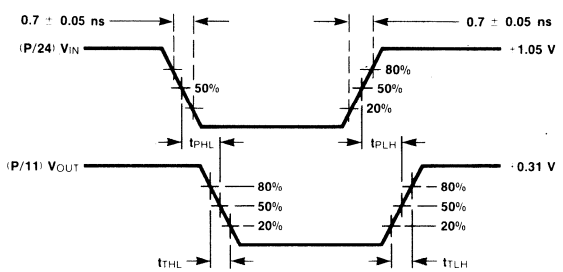
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL} t_{PLH}	Propagation Delay, $\overline{E}_a/\overline{E}_b$ to Z Outputs	1.00	1.45	2.05	ns	See Test Circuit and Waveforms
t_{PHL} t_{PLH}	Propagation Delay, A Inputs to Z Outputs	1.25	1.80	2.50	ns	
t_{PHL} t_{PLH}	Propagation Delay, H Inputs to Z Outputs	1.20	2.00	2.85	ns	
t_{PHL} t_{PLH}	Propagation Delay, M to Z Outputs	2.00	2.90	3.90	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.55	1.50	3.20	ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

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SWITCHING TEST CIRCUIT AND WAVEFORMS





V_{CC} = +2 V, V_{EE} = -2.5 V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from V_{CC} and V_{EE} to GND
All outputs are loaded with 50 Ω to GND
C_L = Jig & Stray Capacitance ≤ 3 pF

Fig. 1

F100171

TRIPLE 4-INPUT MUX WITH ENABLE

F100K SERIES ECL

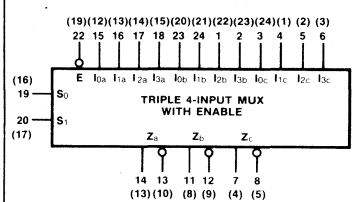
DESCRIPTION – The F100171 contains three 4-input multiplexers which share a common decoder (inputs S_0 and S_1). Output buffer gates provide true and complement outputs. A HIGH on the Enable input ($\overline{E}$) forces all true outputs LOW (see truth table).

PRELIMINARY

PIN NAMES

I_{ni}	Data Inputs
S_n	Select Inputs
$\overline{E}$	Enable Inputs
Z	Data Outputs

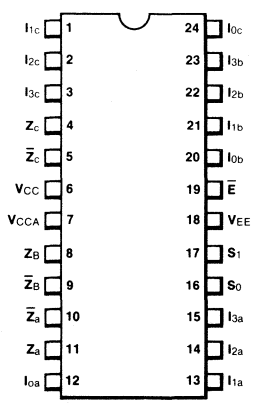
LOGIC SYMBOL



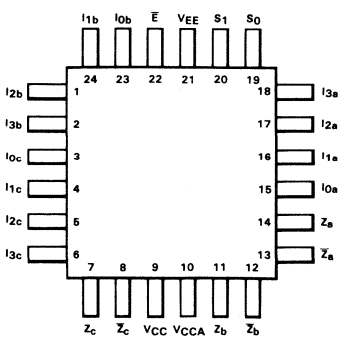
V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)
( ) = DIP

CONNECTION DIAGRAMS

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



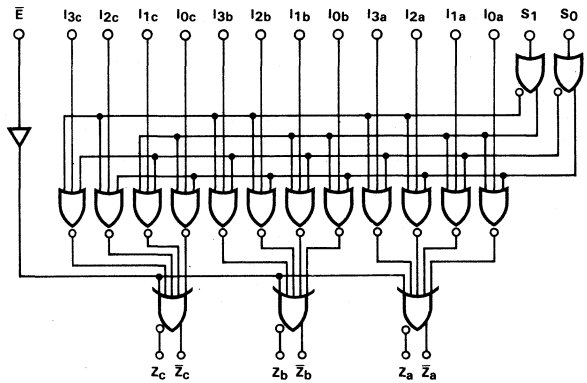
TRUTH TABLE

$\overline{E}$	S_0	S_1	Z_n
L	L	L	I_{0n}
L	H	L	I_{1n}
L	L	H	I_{2n}
L	H	H	I_{3n}
H	X	X	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

10

LOGIC DIAGRAM



DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

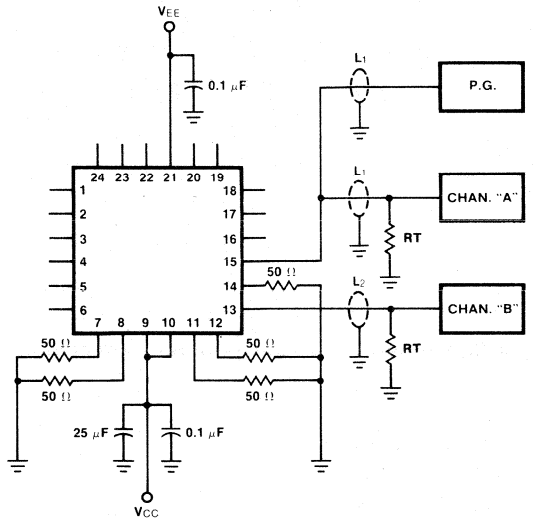
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH S_0, S_1, $\overline{E}$ Data			 300 340	μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	-114	-81	-56	mA	Inputs open

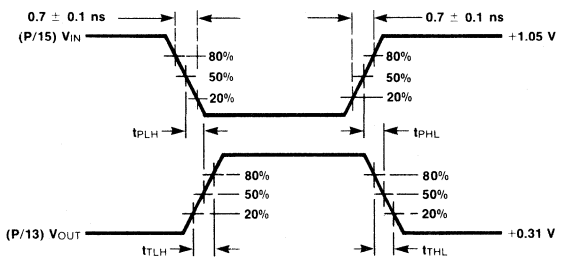
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL} t_{PLH}	Propagation Delay, Data to Z Outputs	0.55	1.00	1.50	ns	See Figure 1
t_{PHL} t_{PLH}	Propagation Delay, S_0/S_1 to Z Outputs	1.25	1.80	2.60	ns	
t_{PHL} t_{PLH}	Propagation Delay, $\overline{E}$ to Z Outputs	0.90	1.50	1.35	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	0.90	1.35	ns	
t_s	Set-Up Time Data to Enable				ns	See Figure 2
t_h	Hold Time Data to Enable				ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING TEST CIRCUIT AND WAVEFORMS





V_{CC} = +2 V, V_{EE} = −2.5 V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig & Stray Capacitance ≤ 3 pF

Fig. 1

t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

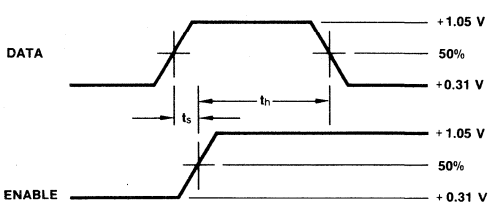


Fig. 2. Set-Up and Hold Times

F100179

CARRY LOOK-AHEAD

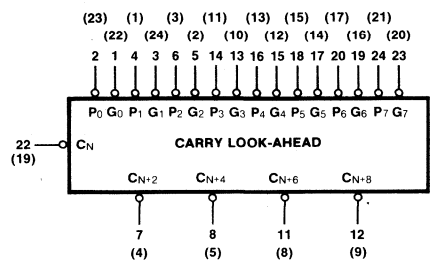
F100K SERIES ECL

DESCRIPTION —F100179 is a high speed carry look-ahead generator intended for use with the F100180 6-bit fast Adder and the F100181 4-bit ALU.

PIN NAMES

C_n	Carry In
P_n	Propagate Inputs
G_n	Generate Inputs
C_{N+}	Carry Out

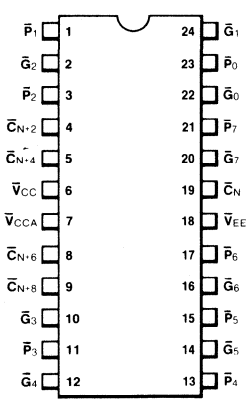
LOGIC SYMBOL



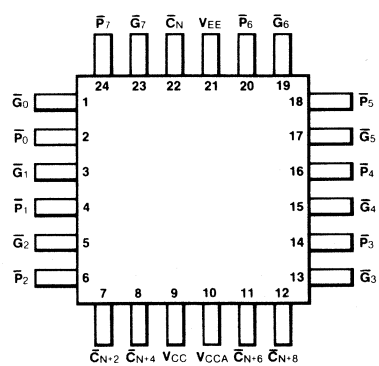
V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)
( ) = DIP

CONNECTION DIAGRAMS

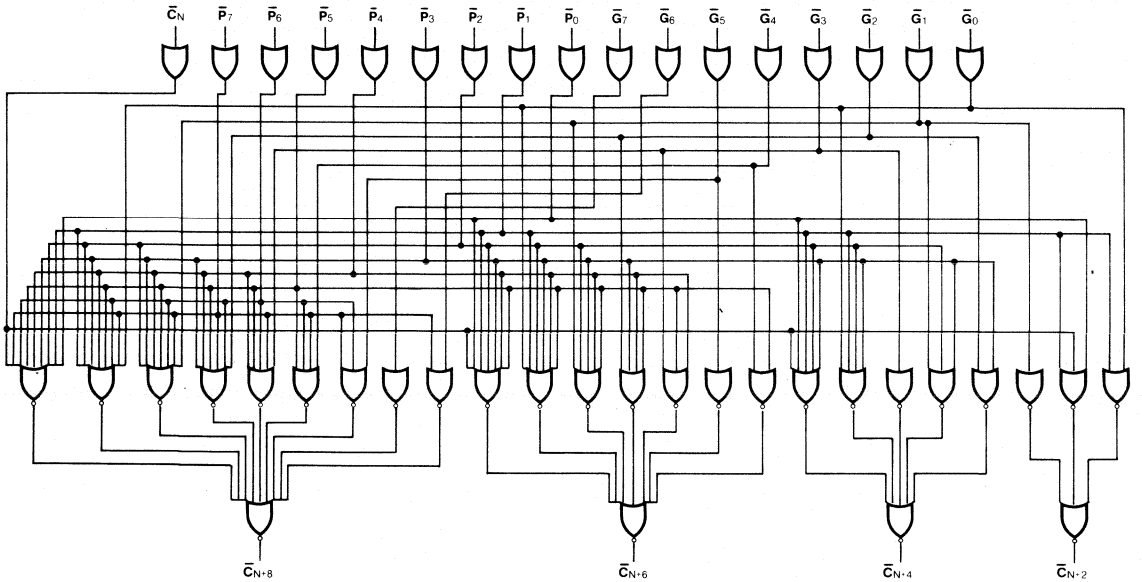
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



LOGIC DIAGRAM



TRUTH TABLES

For $\overline{C}_{N+2}$ Output

$\overline{C}_N$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{C}_{N+2}$
X	X	X	L	X	L
X	L	X	X	L	L
L	X	L	X	L	L
All other combinations					H

$$\overline{C}_{N+2} = \overline{G}_1 \cdot (\overline{P}_1 + \overline{G}_0) \cdot (\overline{P}_1 + \overline{P}_0 + \overline{C}_N)$$

H = HIGH
L = LOW
BLANK = X = DON'T CARE

For $\overline{C}_{N+4}$ Output

$\overline{C}_N$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{C}_{N+4}$
X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	L	X	X	L	L
X	X	X	L	X	X	L	X	L	L
X	L	X	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	L
All other combinations									H

$$\overline{C}_{N+4} = \overline{G}_3 \cdot (\overline{P}_3 + \overline{G}_2) \cdot (\overline{P}_3 + \overline{P}_2 + \overline{G}_1) \cdot (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \cdot (\overline{P}_3 + \overline{P}_2 + \overline{P}_0 + \overline{C}_N)$$

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For $\overline{C}_{N+6}$ Output

$\overline{C}_N$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{G}_4$	$\overline{P}_4$	$\overline{G}_5$	$\overline{P}_5$	$\overline{C}_{N+6}$
X	X	X	X	X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	X	X	X	X	L	X	X	L	L
X	X	X	X	X	X	X	L	X	X	L	X	L	L
X	X	X	X	X	L	X	X	L	X	L	X	L	L
X	X	X	L	X	X	L	X	L	X	L	X	L	L
X	L	X	X	L	X	L	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	X	L	X	L	L
All other combinations													H

$$\overline{C}_{N+6} = \overline{G}_5 \cdot (\overline{P}_5 + \overline{G}_4) \cdot (\overline{P}_5 + \overline{P}_4 + \overline{G}_3) \cdot (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{G}_2) \cdot (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{G}_1) \cdot (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \cdot (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_N)$$

For $\overline{C}_{N+8}$ Output

$\overline{C}_N$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{G}_4$	$\overline{P}_4$	$\overline{G}_5$	$\overline{P}_5$	$\overline{G}_6$	$\overline{P}_6$	$\overline{G}_7$	$\overline{P}_7$	$\overline{C}_{N+8}$
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	L	L
X	X	X	X	X	X	X	X	X	X	X	L	X	X	L	X	L	L
X	X	X	X	X	X	X	X	X	L	X	X	L	X	L	X	L	L
X	X	X	X	X	X	X	L	X	X	L	X	L	X	L	X	L	L
X	X	X	X	X	L	X	X	L	X	L	X	L	X	L	X	L	L
X	X	X	L	X	X	L	X	L	X	L	X	L	X	L	X	L	L
X	L	X	X	L	X	L	X	L	X	L	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	X	L	X	L	X	L	X	L	L
All other combinations																	H

$$\overline{C}_{N+8} = \overline{G}_7 \cdot (\overline{P}_7 + \overline{G}_6) \cdot (\overline{P}_7 + \overline{P}_6 + \overline{G}_5) \cdot (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{G}_4) \cdot (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{G}_3) \cdot (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{G}_2) \cdot (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{G}_1) \cdot (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \cdot (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_N)$$

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
I_{IH}	Input Current HIGH				μA	$V_{IN} = V_{IHA}$
	$\overline{G}_n$ Inputs			250		
	$\overline{P}_n$ Inputs			340		
I_{EE}	Supply Current	-231	-165	-115	mA	Inputs open

AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL} t_{PLH}	Propagation Delay, $\overline{G}_n/\overline{P}_n$ to $\overline{C}_{N+}$ Outputs	1.40	2.10	3.30	ns	Figure 1
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	1.10	1.70	ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING TEST CIRCUIT AND WAVEFORMS

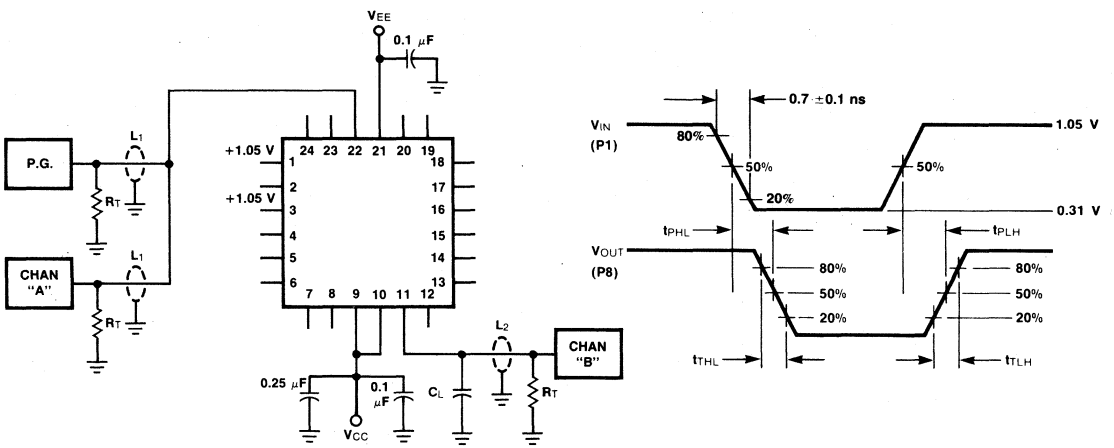


Fig. 1

10

F100180

FAST 6-BIT ADDER

F100K SERIES ECL

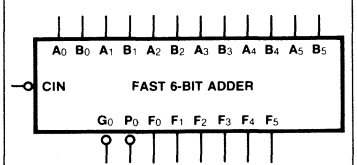
DESCRIPTION – The F100180 is a High Speed 6-Bit Adder capable of performing a full 6-bit addition of 2 operands in 2 ns. Inputs for the adder are active LOW Carry-In, Operand A, and Operand B; outputs are Function, active LOW Carry Generate, and active LOW Carry Propagate. When used with the F100179, Full Carry Lookahead, as a second order Lookahead Block, F100180 provides High speed addition of very long words.

PRELIMINARY

PIN NAMES

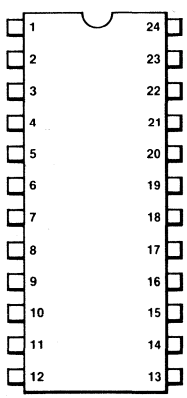
A_n	Operand A Inputs
B_n	Operand B Inputs
$\overline{C}_{IN}$	Carry In Input (Active Low)
$\overline{G}_o$	Carry Generate Output (Active Low)
$\overline{P}_o$	Carry Propagate Output (Active Low)
F_n	Function Outputs

LOGIC SYMBOL

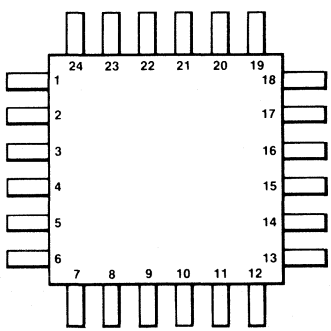


CONNECTION DIAGRAMS

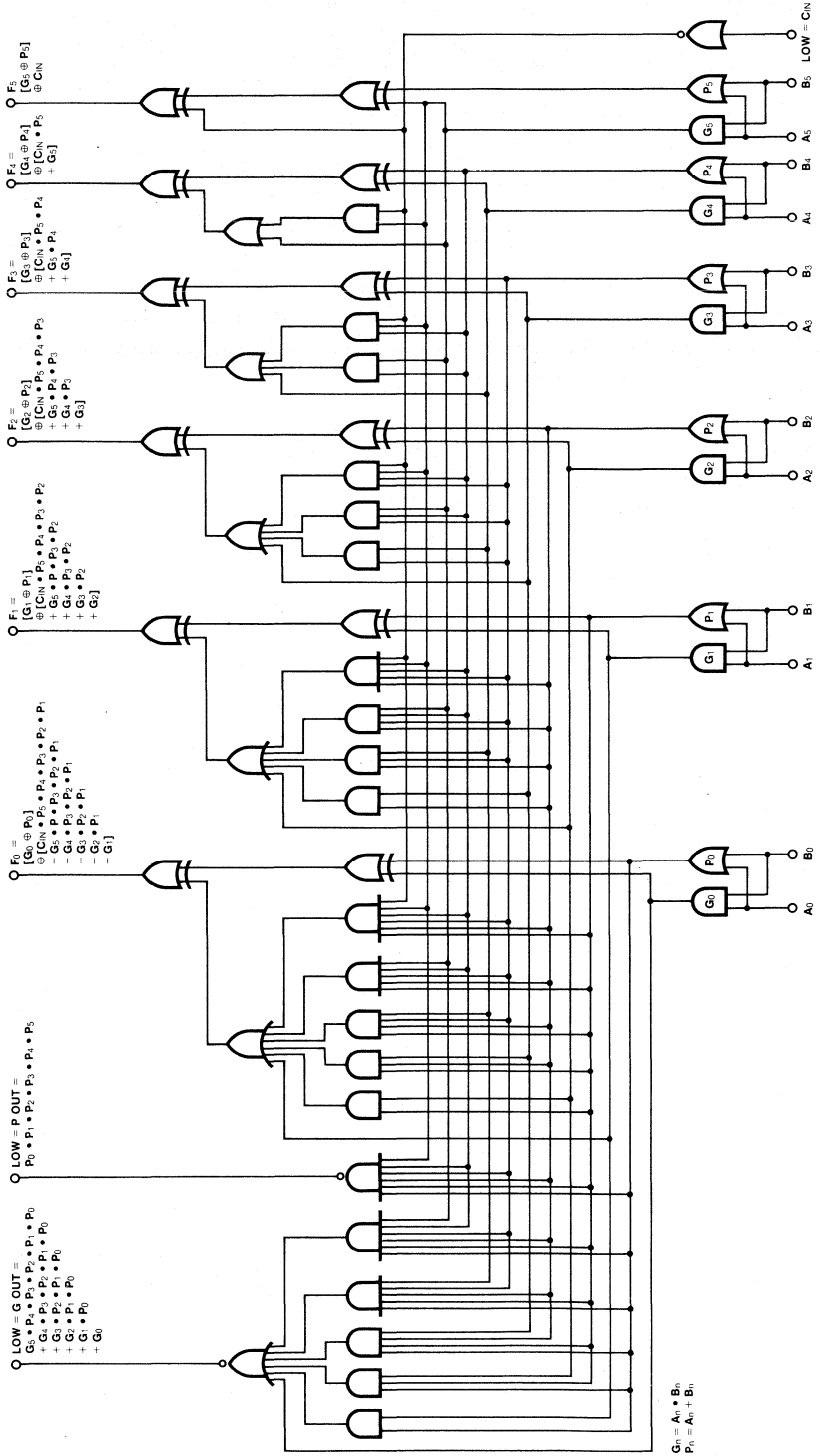
FLATPAK (TOP VIEW)



DIP (TOP VIEW)



LOGIC DIAGRAM



DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

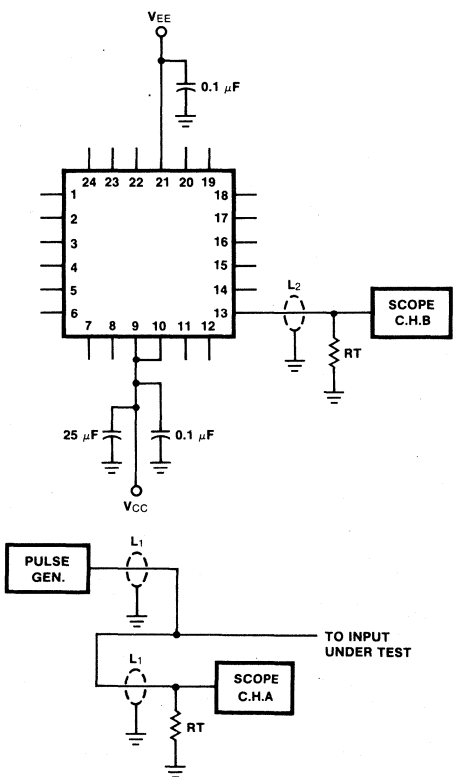
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH		195		μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current		-170		mA	Inputs Open

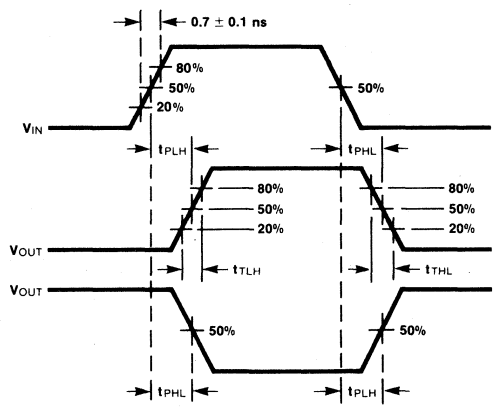
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL} t_{PLH}	Propagation Delay, A/B to F		2.00		ns	
t_{PHL} t_{PLH}	Propagation Delay, A/B to P		1.50		ns	
t_{PHL} t_{PLH}	Propagation Delay, A/B to G		2.00		ns	
t_{PHL} t_{PLH}	Propagation Delay, $\overline{C_{IN}}$ to F		2.00		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%		0.90		ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING TEST CIRCUIT AND WAVEFORM





V_{CC} = +2 V, V_{EE} = -2.5 V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig and Stray Capacitance ≤ 3 pF

Fig. 1

F100181

4-BIT BINARY/BCD ALU

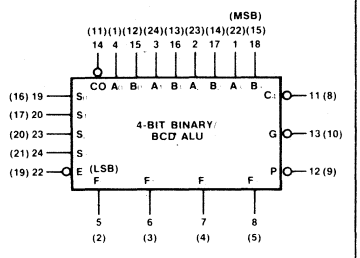
F100K SERIES ECL

DESCRIPTION – The F100181 performs eight logic operations and eight arithmetic operations on a pair of 4-bit words. The operating mode is determined by signals applied to the Select (S_n) inputs, as shown in the Function Select table. In addition to performing binary arithmetic, the circuit contains the necessary correction logic to perform BCD addition and subtraction. Output latches are provided to reduce overall package count and increase system operating speed. When the latches are not required, leaving the Enable ($\overline{E}$) input open makes the latches transparent.

The circuit uses internal lookahead carry to minimize delay to the F outputs and to the ripple Carry Output, C_4. Group carry lookahead Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are also provided, which are independent of the Carry In $\overline{C}_0$. The $\overline{P}$ output goes LOW when a plus operation produces fifteen (nine for BCD) or when a minus operation produces zero. Similarly, $\overline{G}$ goes LOW when the sum of A and B is greater than fifteen (nine for BCD) in plus mode, or when their difference is greater than zero in a minus mode.

PRELIMINARY

LOGIC SYMBOL



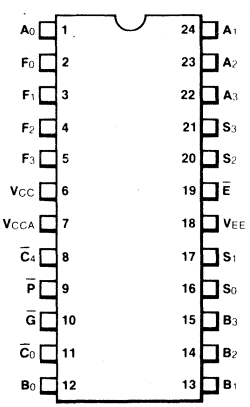
V_{CC} = Pin 9 (6)
V_{CCA} = Pin 10 (7)
V_{EE} = Pin 21 (18)
( ) = DIP

PIN NAMES

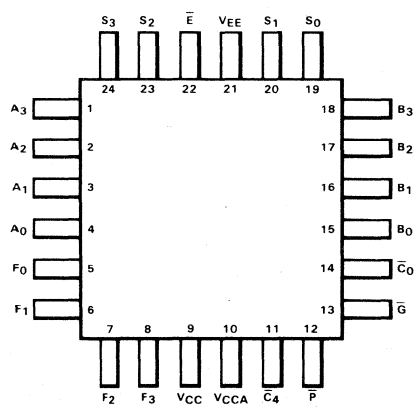
A_n	A Operand Inputs
$\overline{C}_0$	Carry In (Active LOW)
S_n	Function Select Inputs
$\overline{E}$	Latch Enable (Active LOW)
$\overline{P}$	Group Carry Lookahead Propagate (Active LOW)
$\overline{G}$	Group Carry Lookahead Generate (Active LOW)
B_n	B Operand Inputs
$\overline{C}_4$	Carry Out (Active LOW)
F_n	Function Outputs

CONNECTION DIAGRAMS

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



10

FUNCTION SELECT TABLE

S_3	S_2	S_1	S_0	FUNCTION
L	L	L	L	A plus B BCD
L	L	L	H	A minus B BCD
L	L	H	L	B minus A BCD
L	L	H	H	O minus B BCD
L	H	L	L	A plus B Binary
L	H	L	H	A minus B Binary
L	H	H	L	B minus A Binary
L	H	H	H	O minus B Binary
H	L	L	L	$F_n = A_n B_n + \overline{A}_n \overline{B}_n$
H	L	L	H	$F_n = A_n \overline{B}_n + \overline{A}_n B_n$
H	L	H	L	$F_n = A_n + B_n$
H	L	H	H	$F_n = A_n$
H	H	L	L	$F_n = \overline{B}_n$
H	H	L	H	$F_n = B_n$
H	H	H	L	$F_n = A_n B_n$
H	H	H	H	F_n = LOW

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

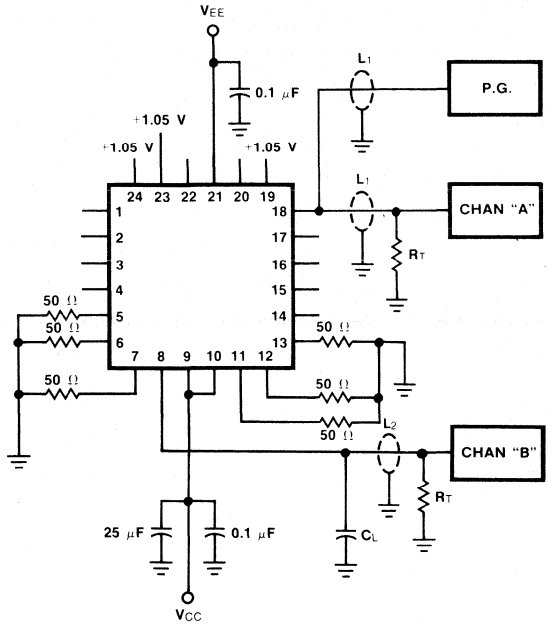
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH S_n, $\overline{OE}$ Other Inputs			 350 250	μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	-240	-170	-120	mA	Inputs open

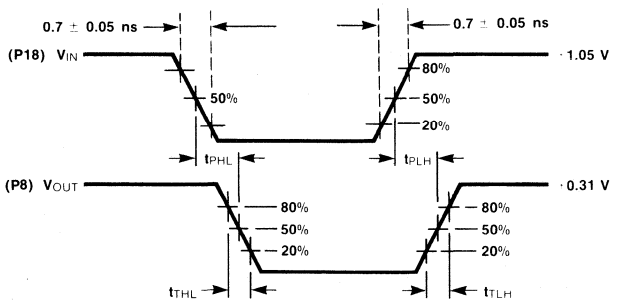
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = -4.5V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL} t_{PLH}	Carry In to Output, $\overline{C}_0$ to F_n	2.10	3.20	4.30	ns	See Figure 1
t_{PHL} t_{PLH}	Carry In to Carry Out, $\overline{C}_0$ to $\overline{C}_4$	1.50	2.40	3.30	ns	
t_{PHL} t_{PLH}	Operand Input to Group Carry Propagate, Generate, A_n, B_n to $\overline{P}$, $\overline{G}$	1.70	2.80	3.70	ns	
t_{PHL} t_{PLH}	Function Select to Group Carry Propagate, Generate, S_n to $\overline{P}$, $\overline{G}$	1.70	2.80	3.70	ns	
t_{PHL} t_{PLH}	Operand Input to Carry Out, A_n, B_n to $\overline{C}_4$	2.40	3.80	4.90	ns	
t_{PHL} t_{PLH}	Function Select to Carry Out, S_n to $\overline{C}_4$	2.40	3.80	4.90	ns	
t_{PHL} t_{PLH}	Operand Input to Output, A_n, B_n to F_n	2.80	4.50	5.90	ns	
t_{PHL} t_{PLH}	Function Select to Output, S_n to F_n	2.80	4.50	5.90	ns	
t_{PHL} t_{PLH}	Enable to Output, $\overline{E}$ to F_n	0.70	1.40	1.90	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	1.00	1.80	ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING TEST CIRCUIT AND WAVEFORMS





V_{CC} = +2 V, V_{EE} = −2.5 V
L_1 and L_2 = equal length 50 Ω impedance lines
R_T equal 50 Ω termination of scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All outputs are loaded with 50 Ω to GND
C_L = Jig & Stray Capacitance ≤ 3 pF

Fig. 1

10

F100194

QUINT DUPLEX BUS DRIVER (TRANSCEIVER)

F100K SERIES ECL

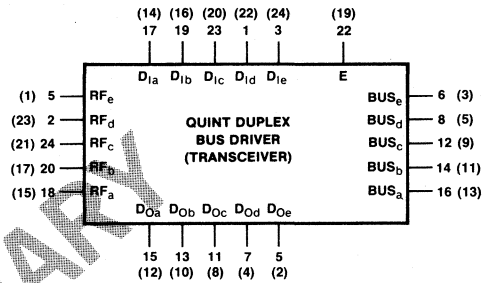
GENERAL DESCRIPTION – The F100194 is a Quint Line Driver/Receiver which is capable of transmitting and receiving full duplex digital signals on a high-speed bus line. Because of the current source line driver, two independent messages may be transmitted on one line at the same time.

The F100194 is designed to work with a wide range of line impedance by connecting a resistor equal to 1/2 the line impedance between RF_n inputs and V_{EE}. Each driver in the circuit will drive lines down 75 Ω, or the 5 drivers may be operated in parallel for lines down to 15 Ω.

The Enable (E) can be used to take all the devices off the line by putting all the outputs into a high impedance state.

PRELIMINARY

LOGIC SYMBOL



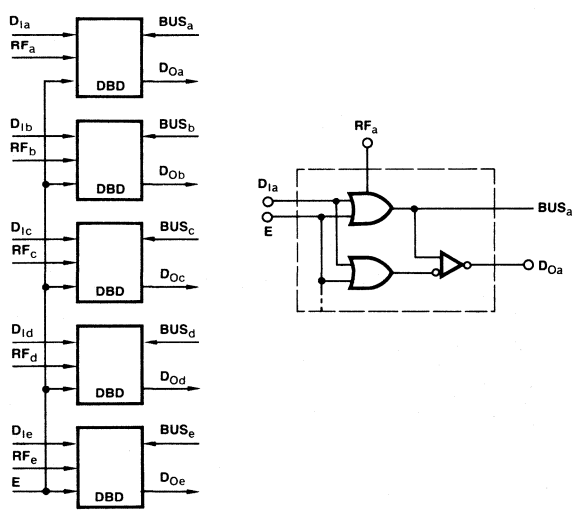
V_{CC} = 9 (6)
V_{CCA} = 10 (7)

V_{EE} = 21 (18)
( ) = DIP

PIN NAMES

E	Enable Input
DI_n	Data Input
RF_n	Reference Resistor Input
BUS_n	Output to Bus
DO_n	Data Output

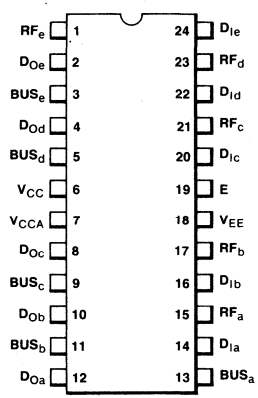
LOGIC DIAGRAM



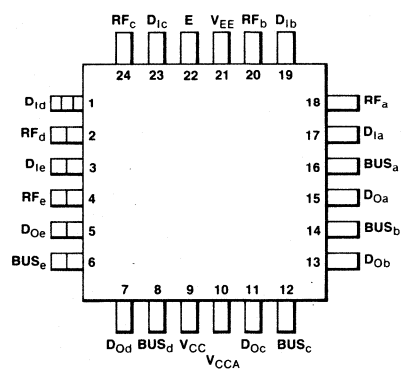
DBD = Duplex Bus Driver
V_{CC} = Pin 9, 10 (6, 7)
V_{EE} = Pin 21 (18)
( ) = DIP

CONNECTION DIAGRAMS

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



DC CHARACTERISTICS: V_{EE} = −4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH Data Inputs Enable Input Bus Input			 220 440 40	μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	−263	−198	−149	mA	Inputs Open
V_{BUS0}	Bus Driver Zero Voltage Level				mV	
V_{BUSH}	Bus Driver HIGH Voltage Level				mV	
V_{BUSL}	Bus Driver LOW Voltage Level				mV	
V_{BUS0A}	Bus Driver Zero Threshold Voltage Level				mV	
V_{BUSHA+} ②	Bus Driver HIGH Threshold Voltage Level				mV	
V_{BUSHA-} ③	Bus Driver HIGH Threshold Voltage Level				mV	
V_{BUSLA}	Bus Driver LOW Threshold Voltage Level				mV	

NOTE 1. Additional D.C. Characteristics are listed in this section under F100K Series ECL Family Characteristics.

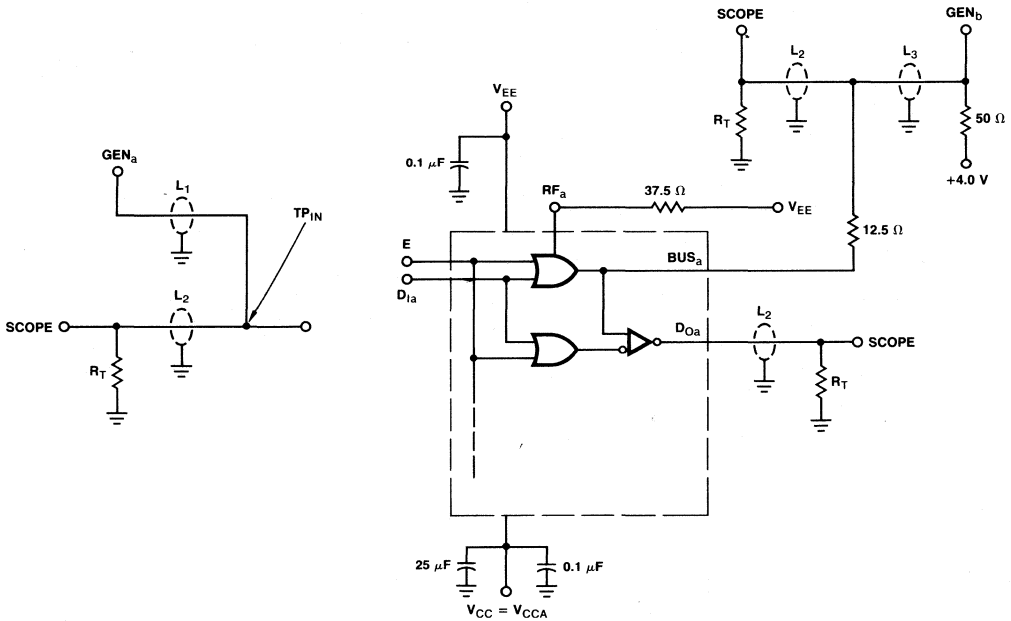
AC CHARACTERISTICS: T_A = 25°C, V_{EE} = −4.5 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL}, t_{PLH}	Propagation Delay, Inputs to Bus		0.90		ns	Figure 1
t_{PHL}, t_{PLH}	Propagation Delay, Enable to Bus		1.50		ns	
t_{PHL}, t_{PLH}	Propagation Delay, Bus to Output		1.20		ns	
t_{TLH} t_{THL}	Transition Time Bus Output 20% to 80%, 80% to 20%		0.80		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%		1.10		ns	

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

10

SWITCHING TEST CIRCUIT AND WAVEFORMS



Wire length should be ≤1/4 inch (6.4mm) from TP_{IN} to input pin and TP_{OUT} to output pin.

$V_{CC} = V_{CCA} = +2.0$ V
$V_{EE} = -2.5$ V
$L_1 = L_2 = L_3$ = Equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
All unused outputs terminated 50 Ω to GND
C_L = Jig and Stray Capacitance ≤ 3 pF.

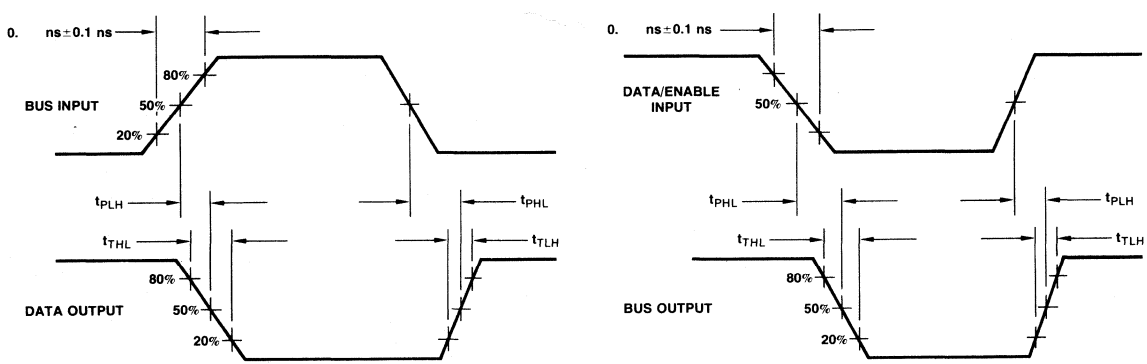
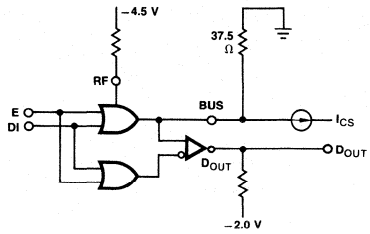


Figure 1

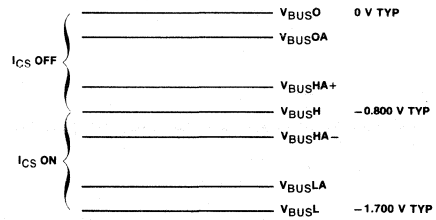
DC TEST CONFIGURATION



NOTE:
I_{CS} is used to represent second transceiver on bus.

D.C. TEST TRUTH TABLE

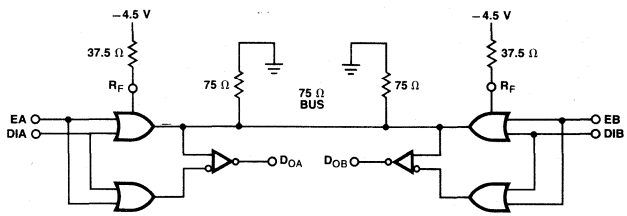
INPUTS		OUTPUTS	
E	D_I	BUS	D_{OUT}
L	L	V_{BUSH}	H
L	H	V_{BUSO}	H
L	L	V_{BUSL}	L
L	H	V_{BUSH}	L
H	H	V_{BUSO}	H



DC LOGIC LEVEL DESCRIPTION

The bus terminal (i.e., BUSA) can be at any one of three possible levels V_{Buso}, V_{BusH}, or V_{BusL} depending upon the combination of inputs applied. The inputs (DIA and E) cause the bus terminal to switch between two levels, V_{Buso} and V_{BusH} when the external current source (I_{CS}) is off, and V_{BusH} and V_{BuuusL} when the external current source is on. The bus output threshold voltage levels caused by applying input threshold voltages V_{ILA} and V_{IHA} at pins 3 and 4, are also translated depending upon the state of I_{CS}. These threshold levels are V_{BusOA} and V_{BusHA+} when I_{CS} is off, and V_{BusHA-} and V_{BusLA} when I_{CS} is on. These relative voltage levels are shown in the figure on the right.

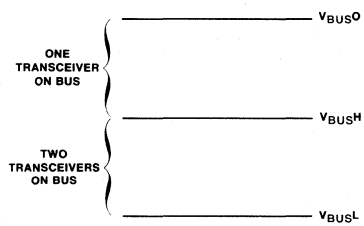
TYPICAL APPLICATION



TRUTH TABLE

INPUTS			OUTPUTS		
E	D_{IA}	D_{IB}	BUS	D_{OA}	D_{OB}
L	L	H	V_{BUSH}	H	L
L	H	L	V_{BUSH}	L	H
L	H	H	V_{BUSO}	H	H
L	L	L	V_{BUSL}	L	L

NOTE: H = Typical F100K V_{OH}
L = Typical F100K V_{OL}



TWO TRANSCEIVER SYSTEM OPERATION: (DBDA & DBDB)

When a signal is transmitted through DIA, the bus and DOB follow; however DOA does not respond to the signal. Likewise, a signal transmitted through DIB causes the bus to follow the signal with no response at DOB. Since the bus has three logic levels, transmission and reception of two simultaneous signals is possible.

The common Enable when high disables transmission from the 5 transceivers in the package but does not interfere with reception from an external transceiver.

F100K LOGIC GATE ARRAY

DESCRIPTION

The F100K Logic Gate Array is a 168 gate array consisting of a 6 x 6 array of internal cells, each cell consisting of 4-2 input gates and 24 output buffer gates arranged 12 on each side. Each of the 24 output buffer gates has 2 inputs and for every 2 output gates there is one set of 2 transistors for expansion to 4 inputs on one of the 2 gates. The possibility exists for having any combination between 24-2 input gates and 12-2 input gates plus 12-4 input gates.

The array size is 173 mils and 130 mils. The internal gate switch current is 2 mA and the external gate switch current is 6 mA. The propagation delays for gates driving one circuit load are typically:

Internal = 750 ps
External = 800 ps

The array appears as a black box to be voltage and temperature compensated and is designed for operation at V_{EE} = -4.5 V. The output levels and input thresholds are intended to be F100K compatible.

The internal gates are actually not fully compensated except that the bias driver produces a fully compensated V_{BB}. The external gates are fully compensated.

The array is designed for a 52-pin package using 2 V_{CC}, 2 V_{EE} and 48/I/O pins. There are actually 4 bonding pads per V_{CC} and V_{EE} pin to minimize voltage drops.

The array has space for 48 wiring channels in one direction on first layer metal. There are up to 78 wiring channels allocated on second layer metal in the other direction.

DEVELOPMENT AIDS

The ECL LSI-168 Array Development Aids generate manufacturing data for LSI ECL (Large Scale Integration Emitter Coupled Logic) circuits. The process is based upon the application of specific metalization patterns to a basic ECL array containing 168 switches. By standardizing the switch array and providing a variety of switch interconnection configurations (called gate functions), the process makes it feasible to use custom LSI circuitry in relatively low quantity products such as computer mainframes.

The process has three steps; layout, development, and fracturing.

LAYOUT

In the layout step, the user employs a set of ground rules, a fixed metalization drawing, and gate function metalization drawings to convert a logic diagram to a layout list containing gate type, gate position, and gate interconnection data for the circuit. This list, which is usually punched on cards, serves as input to the development step.

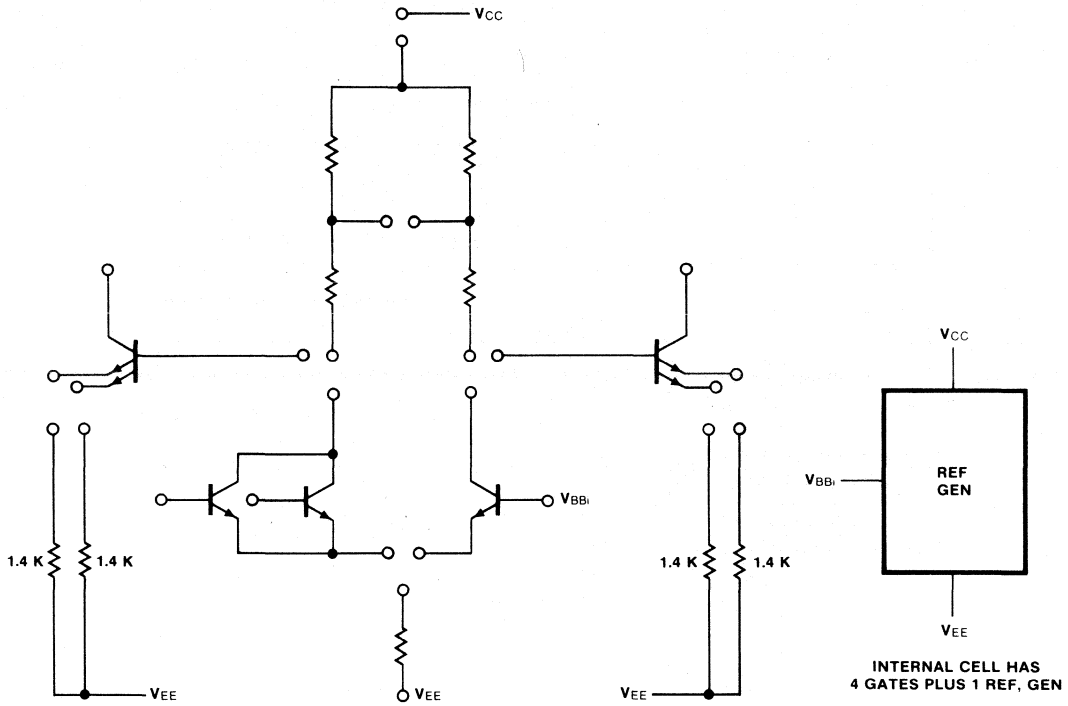
DEVELOPMENT

During this step, the user accesses a worldwide computer time share network to execute Array Development Aid programs that accept the layout list, produce a circuit data base, document gate interconnections, and report spacing/data format errors. One of the programs optionally produces a tape that can be used to generate a pen plot of the circuit. Several iterations of the development step result in a circuit data base that accurately specifies the circuit geometry required to perform the functions defined by the logic diagram.

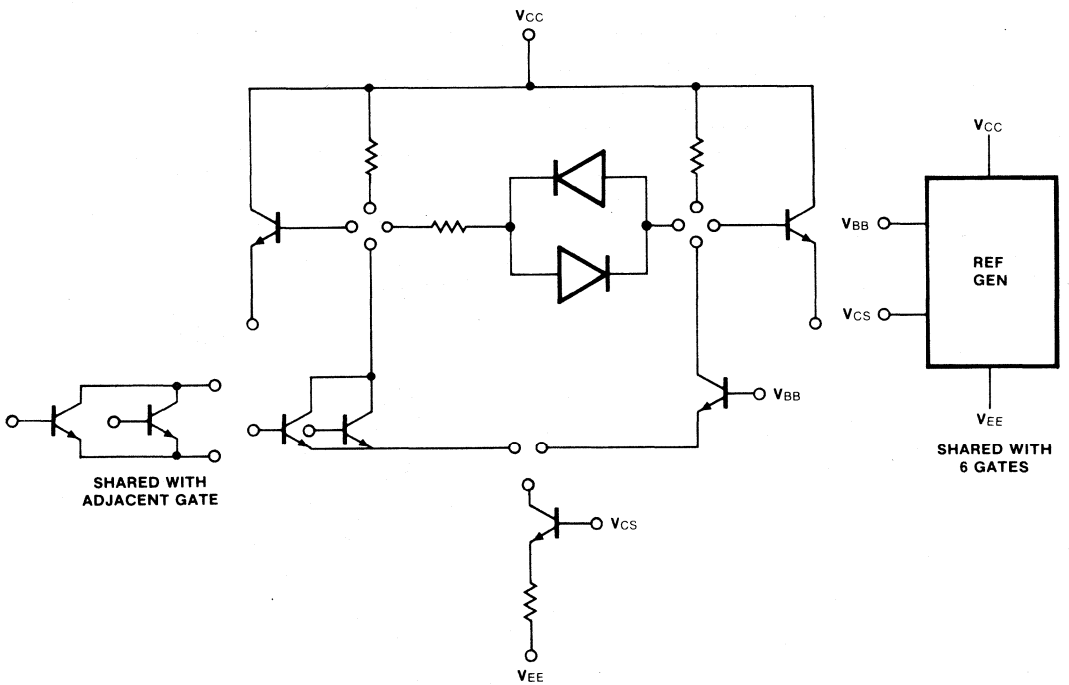
FRACTURING

In this step, the user again accesses the Array Development Aid programs that fracture the circuit data base and produce a pattern generator tape. Fairchild uses these tapes to produce the specific metalization masks that are applied to the basic 168-switch array to form the LSI circuit.

168 GATE, F100K GATE ARRAY



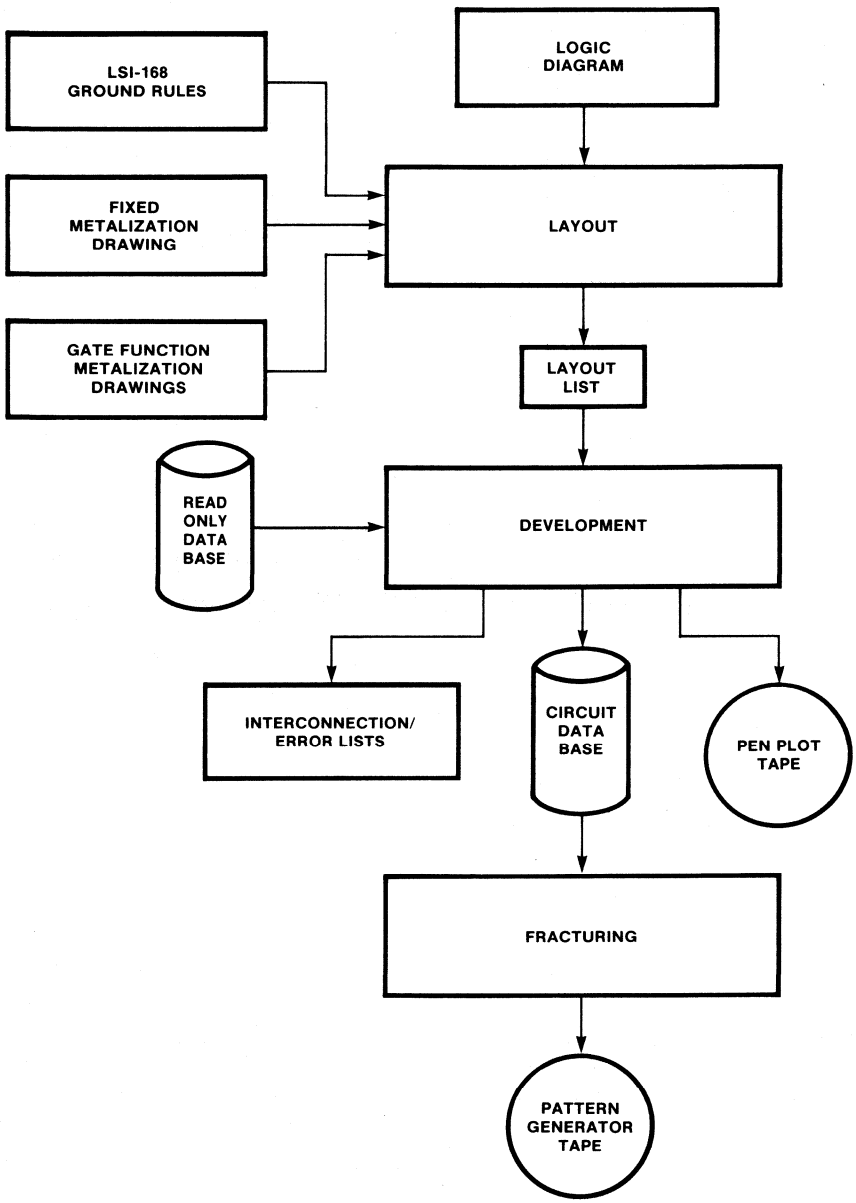
INTERNAL CELL GATE (1 OF 144 SHOWN)



EXTERNAL GATE (1 OF 24 SHOWN)

ADDITIONAL INFORMATION

Additional information about the LSI-168 Array Development Aids Process is available upon request.



ARRAY DEVELOPMENT AIDS PROCESS

INTRODUCTION

ECL FOR HIGH PERFORMANCE SYSTEMS 1

ECL CIRCUIT BASICS 2

ECL LOGIC DESIGN 3

TRANSMISSION LINE CONCEPTS 4

ECL INTERCONNECTIONS 5

POWER DISTRIBUTION AND THERMAL CONSIDERATIONS 6

F10K SERIES DATA SHEETS 7

F95K SERIES DATA SHEETS 8

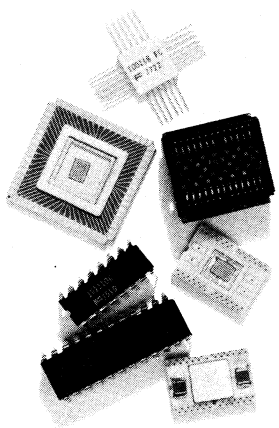
11C SERIES DATA SHEETS 9

F100K SERIES DATA SHEETS 10

ECL MEMORY DATA SHEETS 11

ORDER AND PACKAGE INFORMATION 12

FAIRCHILD FIELD SALES OFFICES, REPRESENTATIVES AND DISTRIBUTORS 13



F10145A • F10545A

16 x 4 REGISTER FILE (RAM)

F10K-VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION – The F10145A and F10545A are high-speed 64-bit Random Access Memories organized as a 16-word by 4-bit array. External logic requirements are minimized by internal address decoding, while memory expansion and data bussing are facilitated by the output disabling features of the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs.

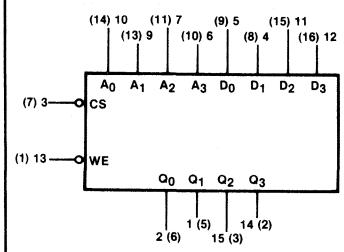
A HIGH signal on $\overline{CS}$ prevents read and write operations and forces the outputs to the LOW state. When $\overline{CS}$ is LOW, the $\overline{WE}$ input controls chip operations. A HIGH signal on $\overline{WE}$ disables the Data input (D_n) buffers and enables readout form the memory location determined by the Address (A_n) inputs. A LOW signal on $\overline{WE}$ forces the Q_n outputs LOW and allows data on the D_n inputs to be stored in the addressed location. Data exits in the same logical sense as presented at the data inputs, *i.e.*, the memory is non-inverting.

- **READ ACCESS TIME—7 ns TYP**
- **50 kΩ INPUT PULL-DOWN RESISTORS**
- **OUTPUTS CAN BE WIRED-OR FOR EASY MEMORY EXPANSION**
- **CHIP SELECT ACCESS TIME—4 ns TYP**
- **VOLTAGE COMPENSATED, INSENSITIVE TO POWER SUPPLY VARIATIONS**
- **FULLY COMPATIBLE WITH ALL 10,000 SERIES ECL**

PIN NAMES

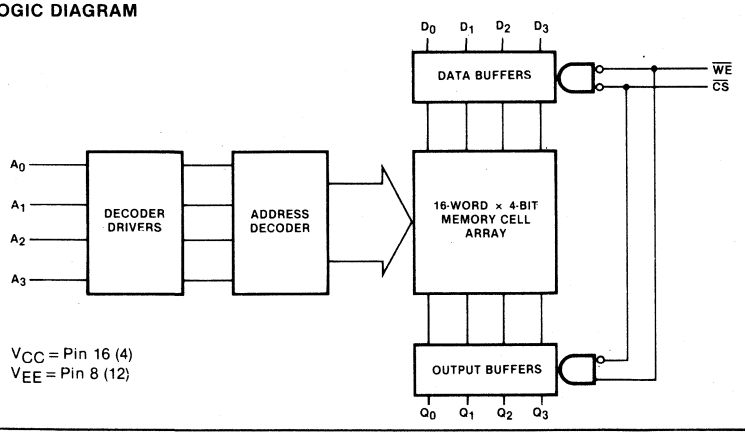
$\overline{CS}$	Chip Select
A_n	Address Lines
D_n	Data Input Lines
$\overline{WE}$	Write Enable
Q_n	Data Output Lines

LOGIC SYMBOL



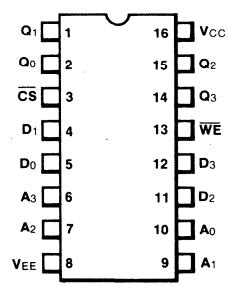
V_{CC} = Pin 16 (4)
V_{EE} = Pin 8 (12)
( ) = Flatpak

LOGIC DIAGRAM



V_{CC} = Pin 16 (4)
V_{EE} = Pin 8 (12)

CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



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DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

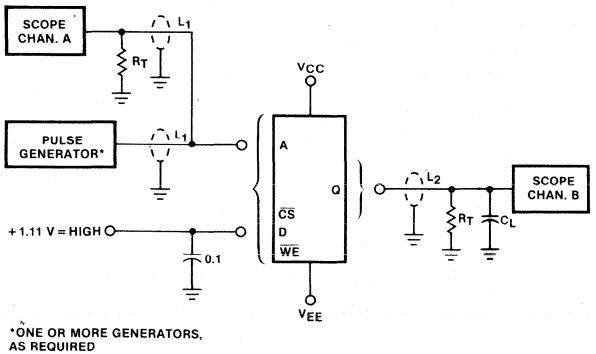
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH				μA	25°C	$V_{IN} = V_{IHA}$
	$\overline{CS}$, A0 — A3			200			
	$\overline{WE}$, D0 — D3			220			
I_{EE}	Supply Current	−150	−100		mA	25°C	Inputs and Outputs Open

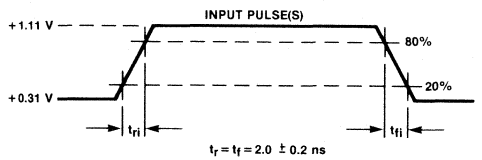
AC CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
	Access/Recovery Times					
t_{ACS}	Chip Select Access	3.0	4.5	6.0	ns	Figures 1, 3
t_{RCS}	Chip Select Recovery	3.0	4.5	6.0	ns	
t_{AA}	Address Access	4.5	6.5	9.0	ns	
	Write Times					
	Set-Up					
t_{WSD}	Data	4.5	3.0		ns	
t_{WSCS}	Chip Select	4.5	2.5		ns	
t_{WSA}	Address	3.5	1.5		ns	Figures 1, 2a
	Hold					
t_{WHD}	Data	−1.0	−2.5		ns	
t_{WHCS}	Chip Select	0.5	0.0		ns	
t_{WHA}	Address	1.0	−1.0		ns	
t_{WR}	Write Recovery Time	3.0	4.5	6.0	ns	Figures 1, 3
t_{WS}	Write Disable Time	3.0	4.5	6.0	ns	
t_w	Write Pulse Width, Min	4.0	2.5		ns	Figures 1, 2a
t_{CS}	Chip Select Pulse Width, Min	4.0	2.5		ns	
	Select Times					
	Set-Up					
t_{CSD}	Data	4.5	3.0		ns	
t_{CSW}	Write Enable	4.5	2.5		ns	
t_{CSA}	Address	3.5	1.5		ns	Figures 1, 2b
	Hold					
t_{CHD}	Data	−1.0	−2.5		ns	
t_{CHW}	Write Enable	0.5	0.0		ns	
t_{CHA}	Address	1.0	−1.0		ns	
	Transition Times					
t_{TLH}	20% to 80%	1.5	2.5	3.9	ns	Figures 1, 3
t_{THL}	80% to 20%	1.5	2.5	3.9	ns	

SWITCHING CIRCUIT AND WAVEFORMS

Fig. 1



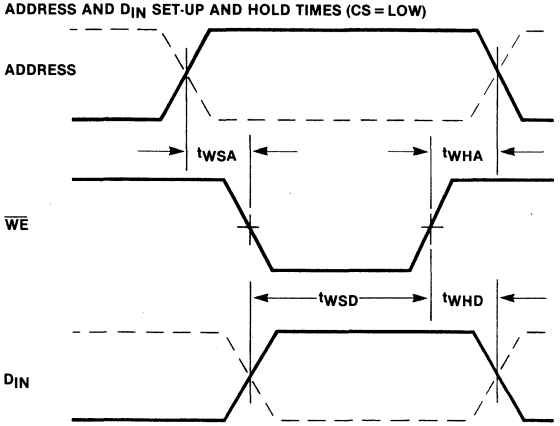


L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance ≤ 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V
Open input = LOW

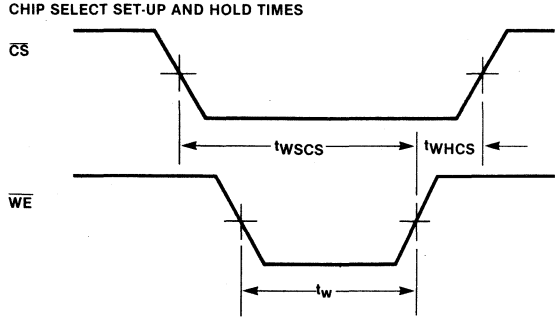
Fig. 2. WRITE MODES

2a. WRITE ENABLE STROBE

ADDRESS AND D_{IN} SET-UP AND HOLD TIMES (CS = LOW)

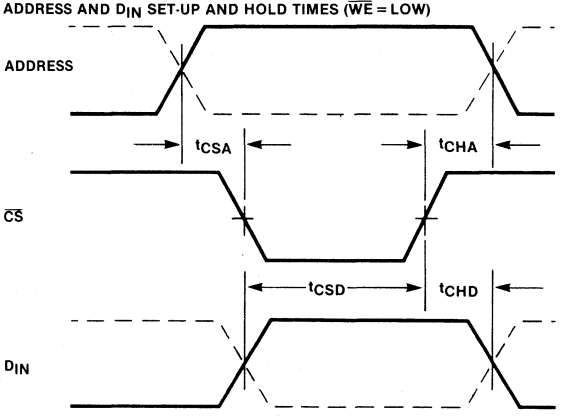


CHIP SELECT SET-UP AND HOLD TIMES

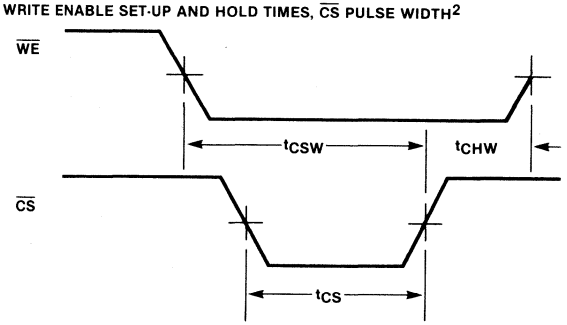


2b. CHIP SELECT STROBE

ADDRESS AND D_{IN} SET-UP AND HOLD TIMES ($\overline{WE}$ = LOW)



WRITE ENABLE SET-UP AND HOLD TIMES, $\overline{CS}$ PULSE WIDTH[2]

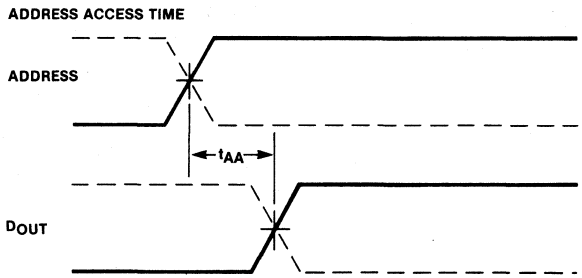


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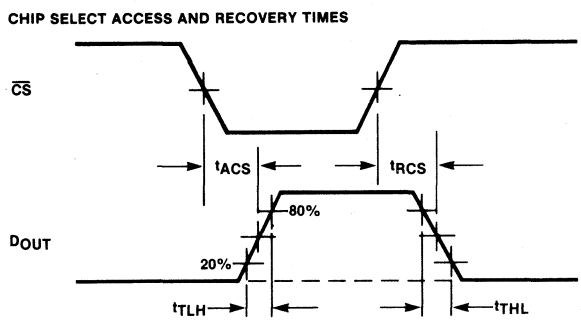
WAVEFORMS (Cont'd)

Fig. 3. READ MODES

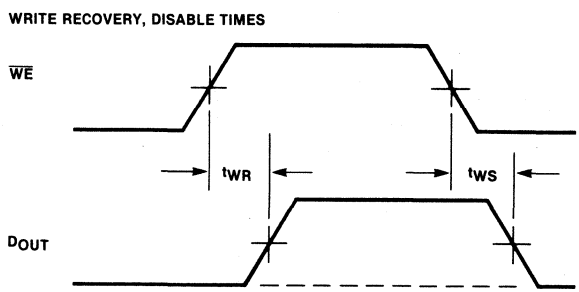
ADDRESS INPUT TO DATA OUTPUT ($\overline{WE}$ = HIGH, $\overline{CS}$ = LOW)



CHIP SELECT INPUT TO DATA OUTPUT ($\overline{WE}$ = HIGH)



WRITE ENABLE INPUT TO DATA OUTPUT ($\overline{CS}$ = LOW)



ECL ISOPLANAR MEMORY F10405

128×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

FAIRCHILD VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION – The F10405 is a 128-bit Read/Write Random Access Memory, organized 128 words by one bit. It has typical access time of 12 ns and is designed for high speed scratch pad, control and buffer storage applications. It is fully compatible with F10K voltage compensated ECL and is usable with fully compensated F95K ECL and uncompensated 10,000 ECL.

The F10405 has full address decoding on chip, separate Data In and non-inverted Data Out lines and three active LOW Chip Select lines.

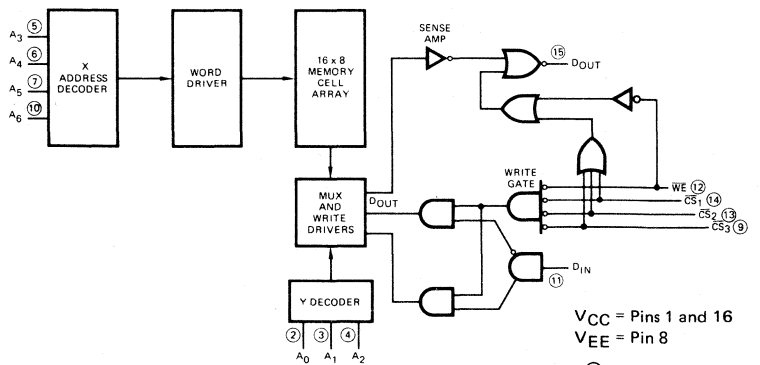
The F10405 is packaged in the hermetic ceramic 16-pin dual in-line package and specified for operation over the temperature range 0°C to 75°C.

- **FULLY COMPATIBLE WITH F10K ECL**
- **READ ACCESS TIME – 12 ns TYP**
- **50 kΩ INPUT PULL DOWN RESISTORS ON CHIP SELECT**
- **USABLE WITH F95K AND UNCOMPENSATED 10,000 ECL**
- **OUTPUTS CAN BE WIRED-OR FOR EASY MEMORY EXPANSION**
- **CHIP SELECT ACCESS TIME – 5 ns TYP**

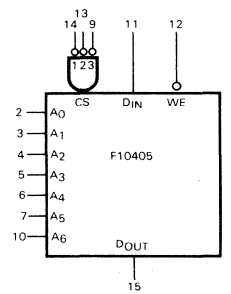
PIN NAMES

$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$	Chip Select Inputs
A_n	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

LOGIC DIAGRAM

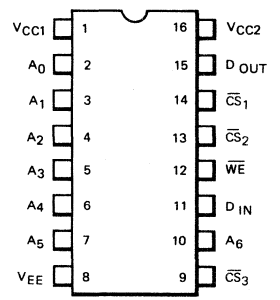


LOGIC SYMBOL



V_{CC} = GND (Pins 1 and i6)
V_{EE} = −5.2 V(Pin 8)

CONNECTION DIAGRAM
DIP (TOP VIEW)



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FUNCTIONAL DESCRIPTION — The F10405 is a fully decoded read/write random access ECL memory, organized 128 words by one bit. The desired word is selected by a 7-bit address (A0 to A6).

The Chip Selects and Write Enable are active LOW. Three Chip Selects are provided for memory expansion. This permits memory array expansion up to 1024 words with the 9538 decoder. For larger memories, the third Chip Select line permits the decoding of Chip Select, $\overline{CS}$, from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable, $\overline{WE}$ (pin 12). With $\overline{WE}$ held LOW, and the chip selected, the data at D_{IN} is written into the addressed location. To Read, $\overline{WE}$ is held HIGH, and the chip is selected. Data in the addressed location is presented at D_{OUT} and is read out non-inverted. The D_{OUT} is LOW except when reading a stored HIGH.

Open emitter outputs are provided on the F10405 to allow maximum flexibility in output wired-OR connections for memory expansion.

A write operation may be performed with the write pulse applied to one of the Chip Select inputs. The two other Chip Selects and the Write Enable must be LOW.

TABLE 1 – TRUTH TABLE

INPUT					OUTPUT	MODE
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}		
X	X	H*	X	X	L	NOT SELECTED
L	L	L	L	L	L	WRITE "0"
L	L	L	L	H	L	WRITE "1"
L	L	L	H	X	D_{OUT}	READ

L = LOW Voltage Levels = –1.7 V
H = HIGH Voltage Levels = –0.9 V
(Nominal values)
X = Don't Care
*One or more Chip Selects HIGH

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{EE} Pin Potential to Ground Pin	–7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	–30 mA to +0.1 mA

GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
MIN	TYP	MAX	Note 4
–5.46 V	–5.2 V	–4.94 V	0°C to +75°C

DC CHARACTERISTICS: V_{EE} = –5.2 V, V_{CC} = GND (Notes 1-4)

SYMBOL	CHARACTERISTIC	LIMITS (Note 6)			UNITS	CONDITIONS		
		B	TYP	A				
V_{OH}	Output Voltage HIGH	–1000		–840	mV	0°C	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to –2.0 V
		–960		–810		+25°C		
		–900		–720		+75°C		
V_{OL}	Output Voltage LOW	–1870		–1665	mV	0°C		
		–1850		–1650		+25°C		
		–1830		–1625		+75°C		
V_{OHC}	Output Voltage HIGH	–1020			mV	0°C	$V_{IN} = V_{IHB}$ or V_{ILA}	
		–980				+25°C		
		–920				+75°C		
V_{OLC}	Output Voltage LOW			–1645	mV	0°C		
				–1630		+25°C		
				–1605		+75°C		
V_{IH}	Input Voltage HIGH	–1145		–840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		–1105		–810		+25°C		
		–1045		–720		+75°C		
V_{IL}	Input Voltage LOW	–1870		–1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		–1850		–1475		+25°C		
		–1830		–1450		+75°C		
I_{IH}	Input Current HIGH			200	μA	0 to +75°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW (Chip Selects)	0.5		160	μA	+25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current		–90		mA	+25°C	Inputs and Output Open	

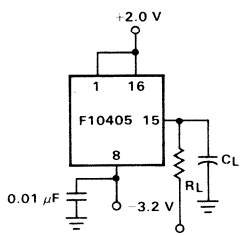
AC CHARACTERISTICS: V_{EE} = −5.2 V ±5%, Output Load = 50 Ω, 10 pF to −2.0 V, T_A = 0°C to +75°C (Note 4)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP Note 3	LIMITS MAX	UNITS	CONDITIONS
READ MODE						
t_{ACS}	Chip Select Access Time		5	8	ns	Fig. 1a & b Measured at 50% of Input to 50% of Output
t_{RCS}	Chip Select Recovery Time		5	8	ns	
t_{AA}	Address Access Time (Note 5)		12	15	ns	
WRITE MODE						
t_W	Write Pulse Width	8	6		ns	t_{WSA} = 4 ns
t_{WSD}	Data Set-up Time Prior to Write	4	3		ns	
t_{WHD}	Data Hold Time After Write	3	0		ns	Fig. 2 Measured at 50% of Input to Valid Output
t_{WSA}	Address Set-up Time	4	3		ns	t_W = 8 ns
t_{WHA}	Address Hold Time	3	2		ns	
t_{WSCS}	Chip Select Set-up Time	4	3		ns	
t_{WHCS}	Chip Select Hold Time	3	2		ns	
t_{WS}	Write Disable Time		6	9	ns	
t_{WR}	Write Recovery Time		6	10	ns	
RISE AND FALL TIME						
t_r	Output Rise Time		3		ns	Measured between 20% & 80% points. (Fig. 1a)
t_f	Output Fall Time		3		ns	
CAPACITANCE						
C_{IN}	Input Lead Capacitance		4	5	pF	
C_{OUT}	Output Lead Capacitance		7	8	pF	

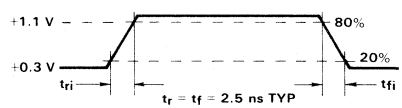
NOTES:
1. Conditions for testing not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{EE} = −5.2 V, +25°C, and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F. P. M. and a two minute warm-up period.
   Thermal resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F. P. M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET.
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
   "A" the value closest to positive infinity.
   "B" the value closest to negative infinity.

AC TEST LOAD AND WAVEFORM

LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels
C_L = 10 pF including Jig and Stray Capacitance
R_L = 50 Ω to −2.0 V

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FUNCTIONAL DESCRIPTION – The F10410 is a fully decoded 256-bit Read/Write Random Access Memory, organized 256 words by one bit. Word selection is achieved by means of an 8-bit address A_0 to A_7.

The active LOW Chip Select inputs are provided for increased logic flexibility. This permits memory array expansion up to 2048 words with the 10161 decoder. For larger memories, the fast chip select time permits the decoding of Chip Select, $\overline{CS}$, from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, pin 14). With $\overline{WE}$ held LOW, and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH, and the chip selected. Data in the addressed location is presented at D_{OUT} and is read out non-inverted. The D_{OUT} is LOW except when reading a stored HIGH.

Open emitter outputs are provided on the F10410 to allow maximum flexibility in output wired-OR connection for memory expansion.

TABLE 1 – TRUTH TABLE

INPUT					OUTPUT	MODE
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}		
X	X	H*	X	X	L	NOT SELECTED
L	L	L	L	L	L	WRITE "0"
L	L	L	L	H	L	WRITE "1"
L	L	L	H	X	D_{OUT}	READ

*One or more Chip Selects HIGH

NOTE:
L = LOW Voltage Levels = –1.7 V
H = HIGH Voltage Levels = –0.9 V (Nominal Values)
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to 150°C
Temperature (Ambient) Under Bias	–55°C to 125°C
V_{EE} Pin Potential to Ground Pin	–7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	–30 mA to +0.1 mA

GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
MIN	TYP	MAX	Note 4
–5.46 V	–5.2 V	–4.94 V	0°C to 75°C

DC CHARACTERISTICS: V_{EE} = –5.2 V, Output Load = 50 Ω to –2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	B LIMIT	TYP (Note 3)	A LIMIT	UNITS	CONDITIONS		
V_{OH}	Output HIGH Voltage	–1000		–840	mV	0°C		
		–960		–810		+25°C		
		–900		–720		+75°C		
V_{OL}	Output LOW Voltage	–1870		–1665	mV	0°C	$V_{IN} = V_{IHA}$ or V_{ILB}	
		–1850		–1650		+25°C		
		–1830		–1625		+75°C		Loading is 50 Ω to –2.0 V
V_{OHC}	Output HIGH Voltage	–1020			mV	0°C		
		–980				+25°C		
		–920				+75°C		
V_{OLC}	Output LOW Voltage			–1645	mV	0°C	$V_{IN} = V_{IHB}$ or V_{ILA}	
				–1630		+25°C		
				–1605		+75°C		
V_{IH}	Input HIGH Voltage	–1145		–840	mV	0°C	Guaranteed Input Voltage	
		–1105		–810		+25°C	HIGH for All Inputs	
		–1045		–720		+75°C		
V_{IL}	Input LOW Voltage	–1870		–1490	mV	0°C	Guaranteed Input Voltage	
		–1850		–1475		+25°C	LOW for All Inputs	
		–1830		–1450		+75°C		
I_{IH}	Input HIGH Current			220	μA	0 to +75°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input LOW Current ($\overline{CS}$)	0.5		170	μA	+25°C	$V_{IN} = V_{ILB}$	
	All Others	–50						
I_{EE}	Power Supply Current		–85		mA	+75°C	All Inputs and Outputs Open	
	(Pin 8)	–130	–95		mA	0°C		

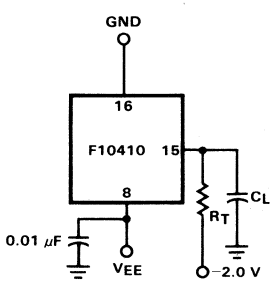
AC CHARACTERISTICS: V_{EE} = −5.2 V ±5%, Output Load = 50 Ω, 30 pF to −2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	PARAMETER	MIN LIMIT	TYP (Note 3)	MAX LIMIT	UNITS	CONDITIONS
READ MODE						
t_{ACS}	Chip Select Access Time		7	12	ns	Fig. 1a & b Measured at 50% of Input to Valid Output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH}). Note 5.
t_{RCS}	Chip Select Recovery Time		7	12	ns	
t_{AA}	Address Access Time		18	30	ns	
WRITE MODE						
t_W	Write Pulse Width	25	15		ns	t_{WSA} = 8 ns
t_{WSD}	Data Set-up Time Prior to Write	5	3		ns	
t_{WHD}	Data Hold Time After Write	5	3		ns	
t_{WSA}	Address Set-up Time	8	5		ns	t_W = 25 ns Fig. 2 Measured at 50% of Input to Valid Output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})
t_{WHA}	Address Hold Time	5	0		ns	
t_{WSCS}	Chip Select Set-up Time	5	3		ns	
t_{WHCS}	Chip Select Hold Time	5	3		ns	
t_{WS}	Write Disable Time	3	7		ns	
t_{WR}	Write Recovery Time		8	20	ns	
RISE AND FALL TIME						
t_r	Output Rise Time		5		ns	Measured between 20% & 80% points. (Fig. 1a)
t_f	Output Fall Time		5		ns	
CAPACITANCE						
C_{IN}	Input Lead Capacitance		4	5	pF	Measure with a Pulse Technique
C_{OUT}	Output Lead Capacitance		7	8	pF	

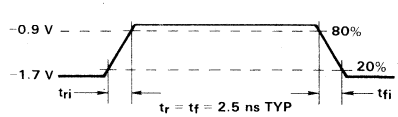
NOTES:
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{EE} = −5.2 V, T_A = +25°C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and two minute warm up period. Typical thermal resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET:
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
   "A" the value closest to positive infinity.
   "B" the value closest to negative infinity.

AC TEST LOAD AND WAVEFORMS

LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels
C_L = 30 pF including Jig and Stray Capacitance
R_L = 50 Ω to −2.0 V

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READ MODE PROPAGATION DELAY
FROM CHIP SELECT

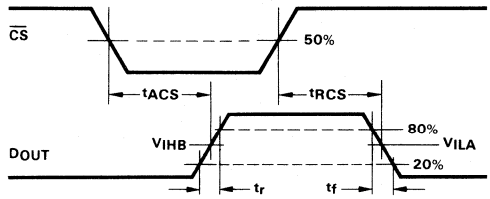


Fig. 1a

READ MODE PROPAGATION DELAY
FROM ADDRESS

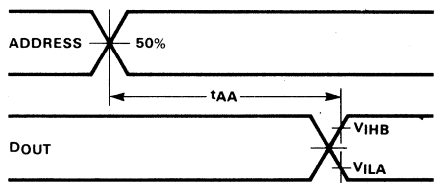


Fig. 1b

WRITE MODE

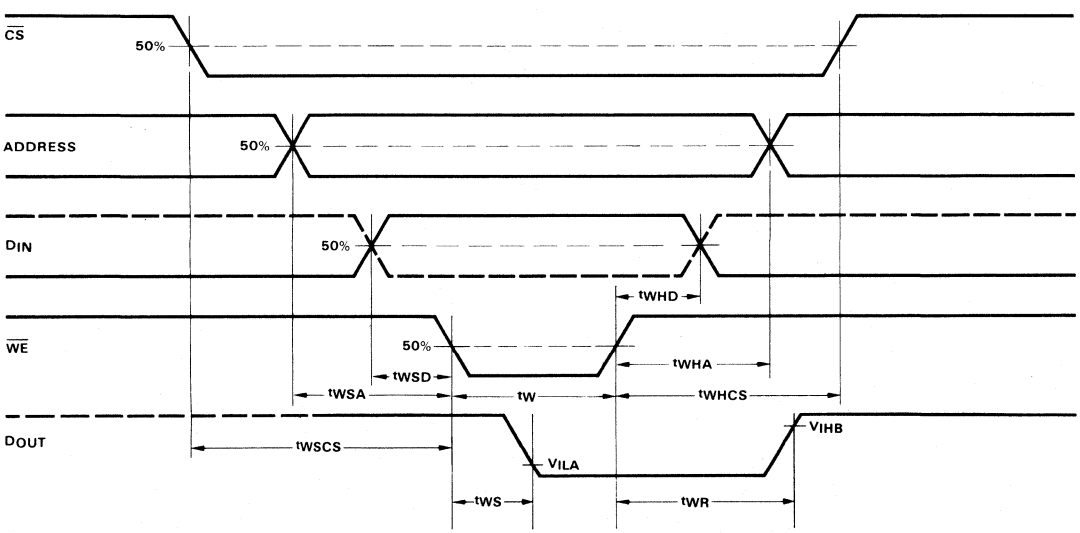


Fig. 2

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

4096 WORD X N–BIT SYSTEM

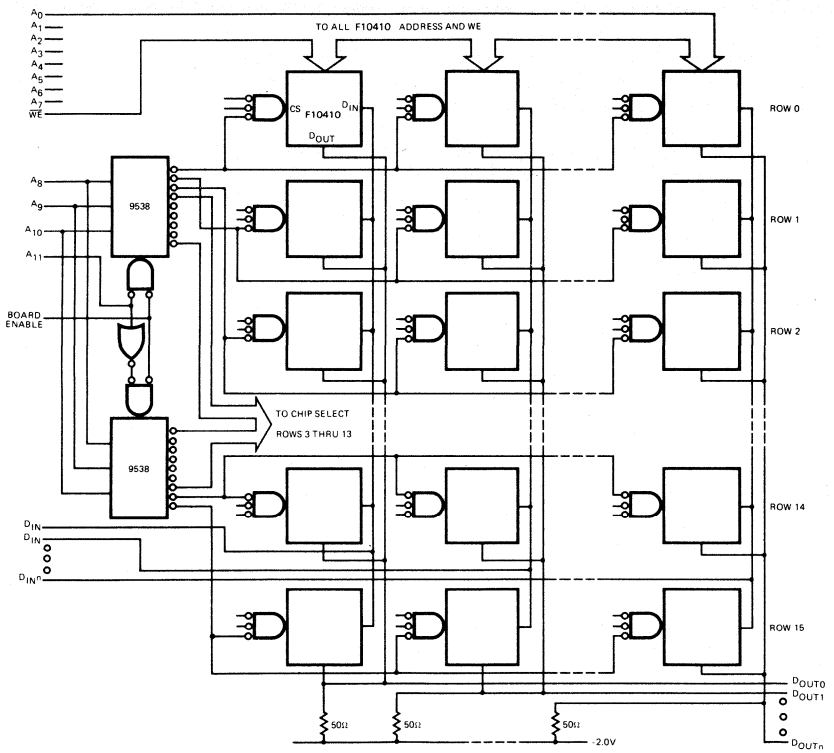


Fig. 3.

ECL ISOPLANAR MEMORY F10411

256×1—BIT FULLY DECODED RANDOM ACCESS MEMORY

FAIRCHILD VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION – The F10411 is a low voltage 256-bit Read/Write Random Access Memory, organized 256 words by one bit. It has a 20 ns typical access time and is designed for high speed scratchpad, control and buffer storage applications. The device includes full address decoding on the chip, has separate Data In and non-inverted Data Out lines, and has three active LOW Chip Select lines.

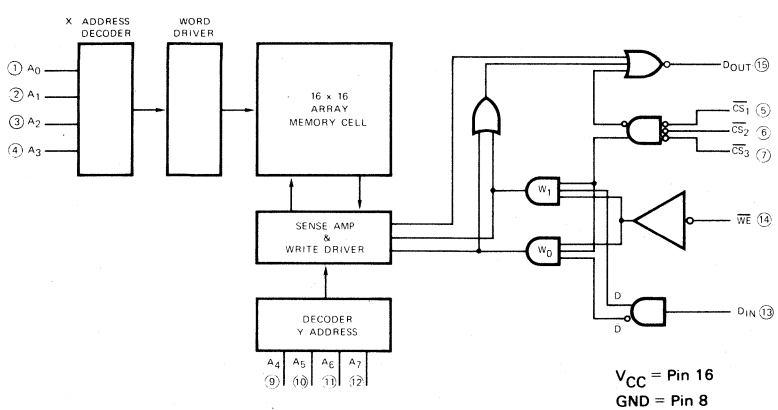
The F10411 is compatible with the F10K and uncompensated 10K ECL families and includes on-chip voltage compensation for improved noise margin. The device is packaged in the hermetic ceramic 16-pin dual in-line package and specified for operation over the temperature range 0°C to 75°C.

- **OPERATES WITH REDUCED POWER SUPPLY VOLTAGE**
- **READ ACCESS TIME – 20 ns TYP**
- **CHIP SELECT ACCESS TIME – 7 ns TYP**
- **POWER DISSIPATION – 1.4 mW / BIT TYP**
- **50 kΩ INPUT PULL-DOWN RESISTORS ON CHIP SELECT**
- **OUTPUTS CAN BE WIRED-OR FOR EASY MEMORY EXPANSION**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**
- **ORGANIZED 256 WORDS X 1 BIT**

PIN NAMES

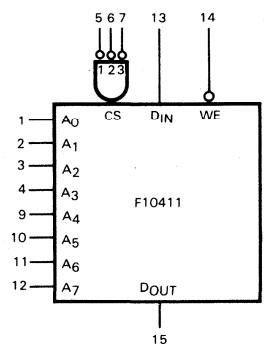
$\overline{CS}_1 - \overline{CS}_3$	Chip Select Inputs
$A_0 - A_7$	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

LOGIC DIAGRAM



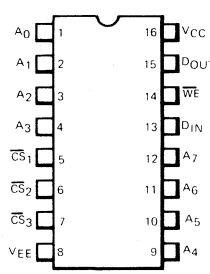
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = 16
V_{EE} = 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION – The F10411 is a fully decoded 256-bit Read/Write Random Access Memory, organized 256 words by one bit. Word selection is achieved by means of an 8-bit address, A_0 thru A_7.

The active LOW Chip Select inputs are provided for increased logic flexibility. This permits memory array expansion up to 2048 words with the 10161 decoder. For larger memories, the fast chip select time permits the decoding of Chip Select, $\overline{CS}$, from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, pin 14). With $\overline{WE}$ held LOW, and the chip selected, the data at D_{IN} is written into the addressed location. To read $\overline{WE}$ is held HIGH, and the chip selected. Data in the addressed location is presented at D_{OUT} and is read out non-inverted. The D_{OUT} is LOW except when reading a stored HIGH.

Open emitter outputs are provided on the F10411 to allow maximum flexibility in output wired-OR connection for memory expansion.

TABLE I – TRUTH TABLE

INPUTS					OUTPUT	MODE
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}		
X	X	H*	X	X	L	Not Selected
L	L	L	L	L	L	Write "0"
L	L	L	L	H	L	Write "1"
L	L	L	H	X	D_{OUT}	Read

L = LOW Voltage Levels = −1.7 V
H = HIGH Voltage Levels = −0.9 V
(Nominal values)
X = Don't Care
*One or more Chip Selects HIGH

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to 150°C
Temperature (Ambient) Under Bias	−55°C to 125°C
V_{EE} Pin Potential to Ground Pin	−7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	−30 mA to +0.1 mA

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GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
MIN	TYP	MAX	Note 4
−4.46 V	−4.25 V	−4.04 V	0°C to 75°C

DC CHARACTERISTICS: V_{EE} = −4.25 V, Output Load = 50 Ω to −2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	LIMITS B LIMIT	LIMITS TYP (Note 3)	LIMITS A LIMIT	UNITS	T_A	CONDITIONS	
V_{OH}	Output HIGH Voltage	−1000 −960 −900		−840 −810 −720	mV	0°C +25°C +75°C	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1870 −1850 −1830		−1605 −1590 −1565	mV	0°C +25°C +75°C		
V_{OHC}	Output HIGH Voltage	−1020 −980 −920			mV	0°C +25°C +75°C	$V_{IN} = V_{IHB}$ or V_{ILA}	
V_{OLC}	Output LOW Voltage			−1585 −1570 −1545	mV	0°C +25°C +75°C		
V_{IH}	Input HIGH Voltage	−1045 −1025 −1000		−735 −705 −615	mV	0°C +25°C +75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input LOW Voltage	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C +25°C +75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input HIGH Current			200	μA	0 to +75°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input LOW Current (CS) All Others	0.5 −50		150	μA	+25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current (Pin 8)	 −125	−80 −90		mA mA	+75°C 0°C	All Inputs and Outputs Open	

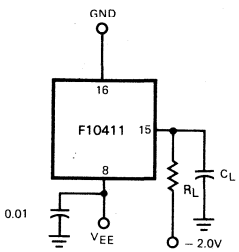
AC CHARACTERISTICS: V_{EE} = −4.25 V ±5%, Output Load = 50 Ω, 30 pF to −2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	LIMITS MIN LIMIT	LIMITS TYP (Note 3)	LIMITS MAX LIMIT	UNITS	CONDITIONS	
READ MODE							
t_{ACS}	Chip Select Access Time		7	12	ns		Fig. 1a and b Measured at 50% of Input to Valid Output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH}). Note 5.
t_{RCS}	Chip Select Recovery Time		7	12	ns		
t_{AA}	Address Access Time		20	35	ns		
WRITE MODE							
t_W	Write Pulse Width	30	20		ns	t_{WSA} = 10 ns	
t_{WSD}	Data Set-Up Time Prior to Write	7	3		ns		
t_{WHD}	Data Hold Time After Write	7	3		ns		
t_{WSA}	Address Set-Up Time	10	6		ns	t_W = 30 ns	Fig. 2 Measured at 50% of Input to Valid Output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})
t_{WHA}	Address Hold Time	5	0		ns		
t_{WSCS}	Chip Select Set-Up Time	5	3		ns		
t_{WHCS}	Chip Select Hold Time	5	3		ns		
t_{WS}	Write Disable Time	3	7		ns		
t_{WR}	Write Recovery Time		9	20	ns		
RISE AND FALL TIME							
t_r	Output Rise Time		5		ns		Measured between 20% and 80% points. (Fig. 1a)
t_f	Output Fall Time		5		ns		
CAPACITANCE							
C_{IN}	Input Load Capacitance		4	5	pF		Measure with a Pulse Technique
C_{OUT}	Output Load Capacitance		7	8	pF		

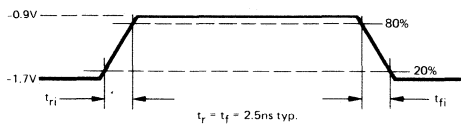
NOTES:
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at $V_{EE} = -4.25$ V, $T_A = +25°C$ and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and a two minute warm-up period. Typical thermal resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C / Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C / Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C / Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET.
   The symbols and terms used in this data sheet have been chosen to agree with the lateststandards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
   "A" the value closest to positive infinity.
   "B" the value closest to negative infinity.

AC TEST LOAD AND WAVEFORMS

LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels
C_L = 30 pF including Jig and Stray Capacitance
R_L = 50 Ω to −2.0 V

READ MODE PROPAGATION DELAY FROM CHIP SELECT

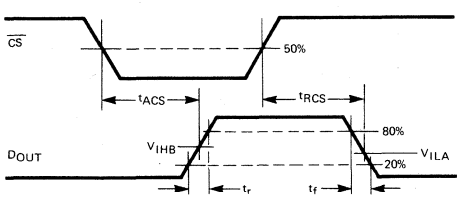


Fig. 1a

READ MODE PROPAGATION DELAY FROM ADDRESS

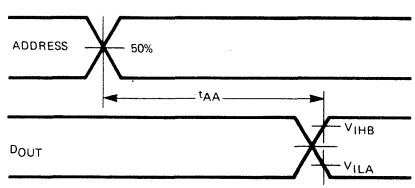


Fig. 1b

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WRITE MODE

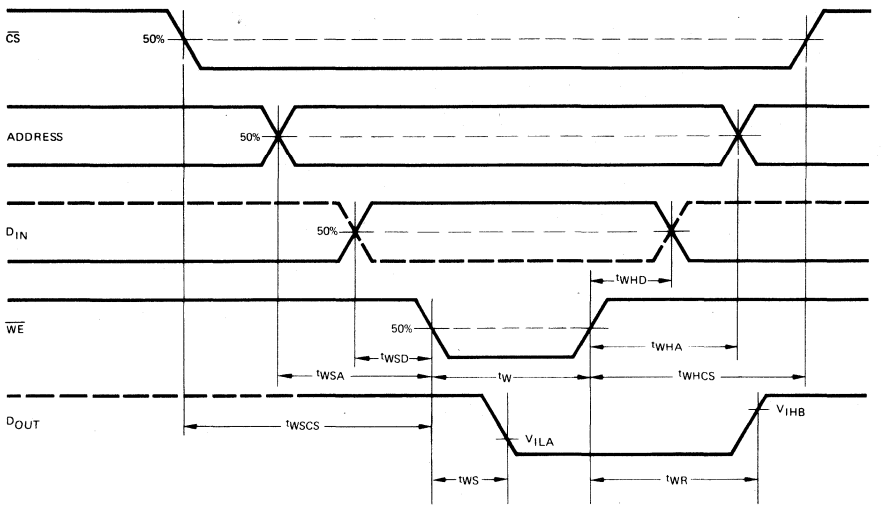


Fig. 2

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

4096-WORD X N-BIT SYSTEM

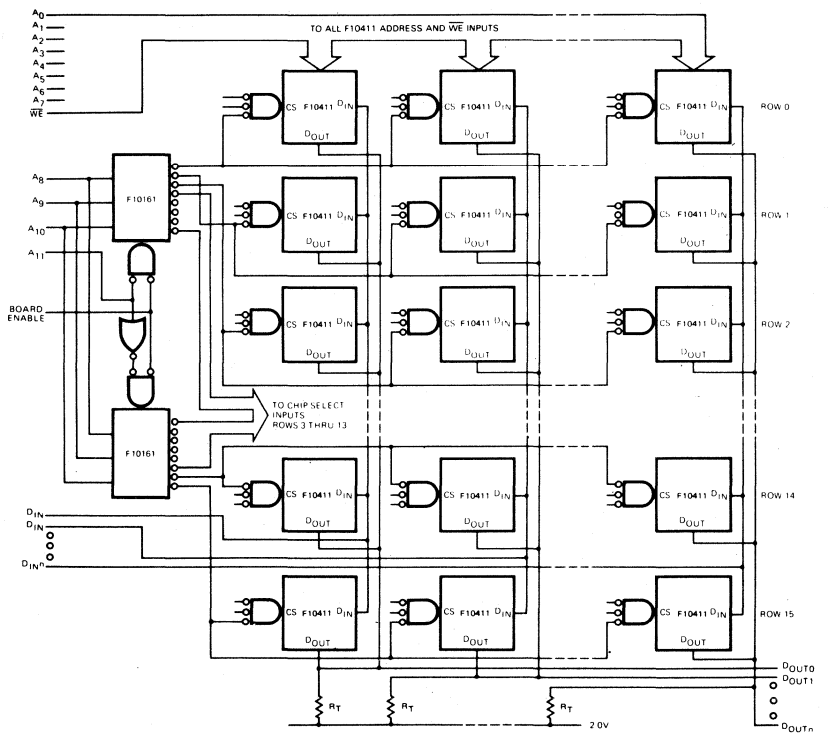


Fig. 3

ECL ISOPLANAR MEMORY F10414

256 × 1-BIT FULLY DECODED RANDOM ACCESS MEMORY

FAIRCHILD VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION – The F10414 is a 256-bit Read/Write random access Memory, organized 256 words by one bit. It has typical access time of 7 ns and is designed for high speed scratch pad, control and buffer storage applications. The device includes full address decoding on the chip, has separate Data In and non-inverted Data Out lines, and has three active LOW Chip Select lines.

The F10414 is compatible with the F10K and uncompensated 10K ECL families and includes on-chip voltage compensation for imporved noise margin. The device is packaged in the hermetic ceramic 16-pin dual in-line package and specified for operation over the temperature range 0°C to 75°C.

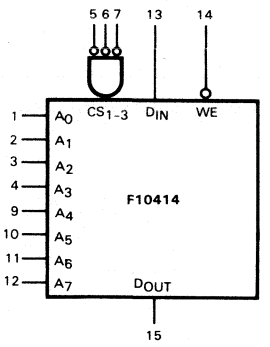
- **VERY HIGH SPEED**
- **COMPATIBLE WITH F10K AND UNCOMPENSATED ECL LOGIC**
- **READ ACCESS TIME – 7 ns TYPICAL**
- **CHIP SELECT ACCESS TIME – 4 ns TYPICAL**
- **POWER DISSIPATION – 1.8 mW/BIT**
- **50 kΩ INPUT PULL-DOWN RESISTORS ON CHIP SELECT**
- **OUTPUTS CAN BE WIRED-OR FOR EASY MEMORY EXPANSION**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**
- **ORGANIZED – 256 WORDS X 1 BIT**

PIN NAMES

$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$	Chip Select Inputs
A_0 - A_7	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

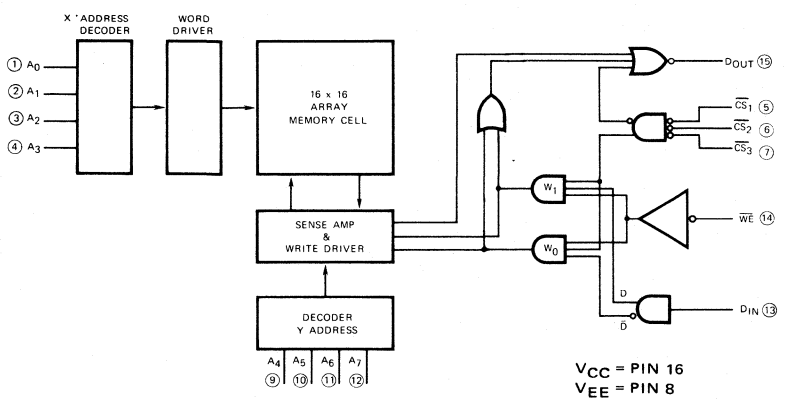
PRELIMINARY

LOGIC SYMBOL



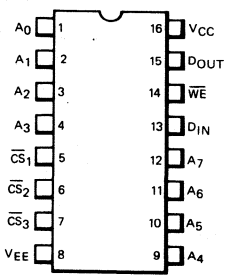
V_{CC} = PIN 16
V_{EE} = PIN 8

LOGIC DIAGRAM



V_{CC} = PIN 16
V_{EE} = PIN 8
○ = PIN NUMBERS

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

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FUNCTIONAL DESCRIPTION – The F10414 is a fully decoded 256-bit Read/Write Random Access Memory, organized 256 words by one bit. Word selection is achieved by means of an 8-bit address A_0 to A_7.

The active LOW chip select inputs are provided for increased logic flexibility. This permits memory array expansion up to 2048 words with the 10161 decoder. For larger memories, the fast chip select time permits the decoding of Chip Select, CS, from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable, ($\overline{WE}$, pin 14). With $\overline{WE}$ held LOW, and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH, and the chip selected. Data in the addressed location is presented at D_{OUT} and is read out non-inverted. The D_{OUT} is LOW except when reading a stored HIGH.

Open emitter outputs are provided on the F10414 to allow maximum flexibility in output wired-OR connection for memory expansion.

TABLE 1 – TRUTH TABLE

INPUT					OUTPUT	MODE
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}		
X	X	H*	X	X	L	NOT SELECTED
L	L	L	L	L	L	WRITE "0"
L	L	L	L	H	L	WRITE "1"
L	L	L	H	X	D_{OUT}	READ

*One or more Chip Selects HIGH

NOTE:
L = LOW Voltage Levels = –1.7 V
H = HIGH Voltage Levels = –0.9 V (Nominal Values)
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to 150°C
Temperature (Ambient) Under Bias	–55°C to 125°C
V_{EE} Pin Potential to Ground Pin	–7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	–30 mA to +0.1 mA

GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
MIN	TYP	MAX	Note 4
–5.46 V	–5.2 V	–4.94 V	0°C to 75°C

DC CHARACTERISTICS: V_{EE} = –5.2 V, Output Load = 50 Ω to –2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	B LIMIT	TYP (Note 3)	A LIMIT	UNITS	CONDITIONS		
V_{OH}	Output HIGH Voltage	–1000		–840	mV	0°C	V_{IN} = V_{IHA} or V_{ILB}	Loading is 50 Ω to –2.0 V
		–960		–810		+25°C		
		–900		–720		+75°C		
V_{OL}	Output LOW Voltage	–1870		–1665	mV	0°C		
		–1850		–1650		+25°C		
		–1830		–1625		+75°C		
V_{OHC}	Output HIGH Voltage	–1020			mV	0°C	V_{IN} = V_{IHB} or V_{ILA}	
		–980				+25°C		
		–920				+75°C		
V_{OLC}	Output LOW Voltage			–1645	mV	0°C		
				–1630		+25°C		
				–1605		+75°C		
V_{IH}	Input HIGH Voltage	–1145		–840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		–1105		–810		+25°C		
		–1045		–720		+75°C		
V_{IL}	Input LOW Voltage	–1870		–1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		–1850		–1475		+25°C		
		–1830		–1450		+75°C		
I_{IH}	Input HIGH Current			220	μA	0 to +75°C	V_{IN} = V_{IHA}	
I_{IL}	Input LOW Current ($\overline{CS}$)	0.5		170	μA	+25°C	V_{IN} = V_{ILB}	
	All Others	–50						
I_{EE}	Power Supply Current		–90		mA	+75°C	All Inputs and Outputs Open	
	(Pin 8)		–100		mA	0°C		

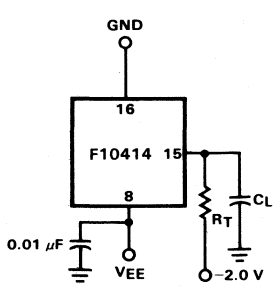
AC CHARACTERISTICS: V_{EE} = −5.2 V ±5%, Output Load = 50 Ω, 10 pF to −2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	PARAMETER	MIN LIMIT	TYP (Note 3)	MAX LIMIT	UNITS	CONDITIONS
READ MODE						
t_{ACS}	Chip Select Access Time		4		ns	Fig. 1a & b Measured at 50%
t_{RCS}	Chip Select Recovery Time		4		ns	of Input to Valid Output
t_{AA}	Address Access Time		7		ns	(V_{ILA} for V_{OL} or V_{IHB} for V_{OH}). Note 5.
WRITE MODE						
t_W	Write Pulse Width	6	4		ns	t_{WSA} = 3 ns
t_{WSD}	Data Set-up Time Prior to Write		0		ns	
t_{WHD}	Data Hold Time After Write		0		ns	
t_{WSA}	Address Set-up Time		1		ns	t_W = 6 ns Fig. 2 Measured at 50% of
t_{WHA}	Address Hold Time		0		ns	Input to Valid Output
t_{WSCS}	Chip Select Set-up Time		0		ns	(V_{ILA} for V_{OL} or
t_{WHCS}	Chip Select Hold Time		1		ns	V_{IHB} for V_{OH})
t_{WS}	Write Disable Time		4		ns	
t_{WR}	Write Recovery Time		5		ns	
RISE AND FALL TIME						
t_r	Output Rise Time		4		ns	Measured between 20% &
t_f	Output Fall Time		4		ns	80% points. (Fig. 1a)
CAPACITANCE						Measure with a
C_{IN}	Input Lead Capacitance		4	5	pF	Pulse Technique
C_{OUT}	Output Lead Capacitance		7	8	pF	

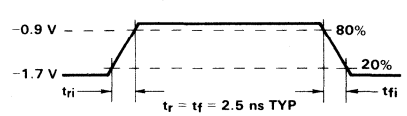
NOTES:
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{EE} = −5.2 V, T_A = +25°C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and two minute warm up period. Typical thermal resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET:
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
   "A" the value closest to positive infinity.
   "B" the value closest to negative infinity.

AC TEST LOAD AND WAVEFORMS

LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels
C_L = 10 pF including Jig and Stray Capacitance
R_L = 50 Ω to −2.0 V

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READ MODE PROPAGATION DELAY
FROM CHIP SELECT

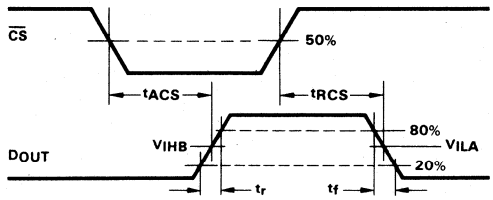


Fig. 1a

READ MODE PROPAGATION DELAY
FROM ADDRESS

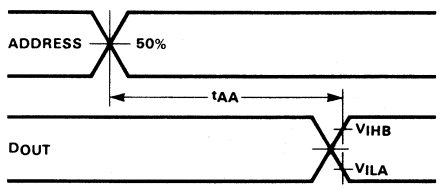


Fig. 1b

WRITE MODE

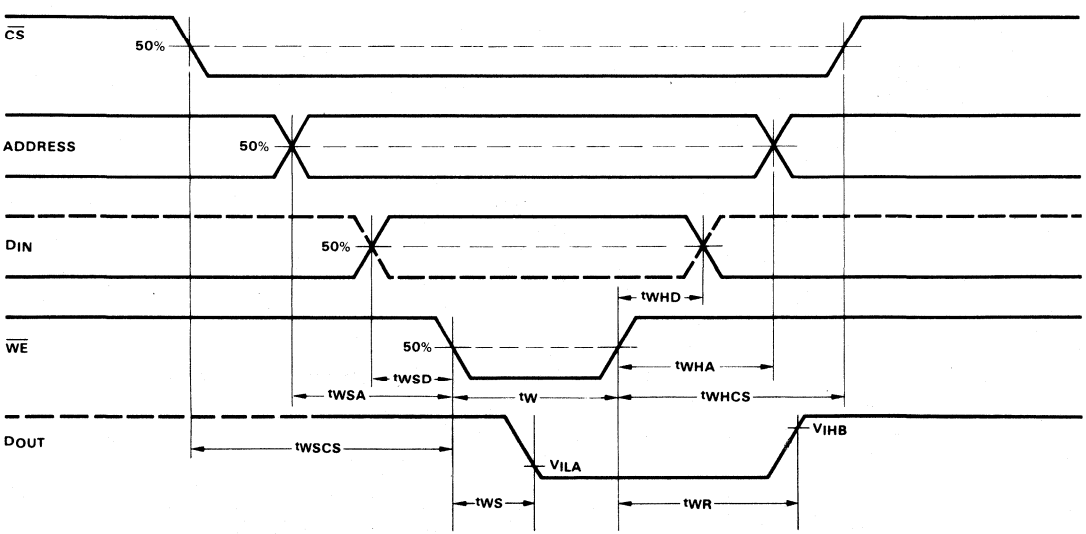


Fig. 2

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

4096 WORD X N–BIT SYSTEM

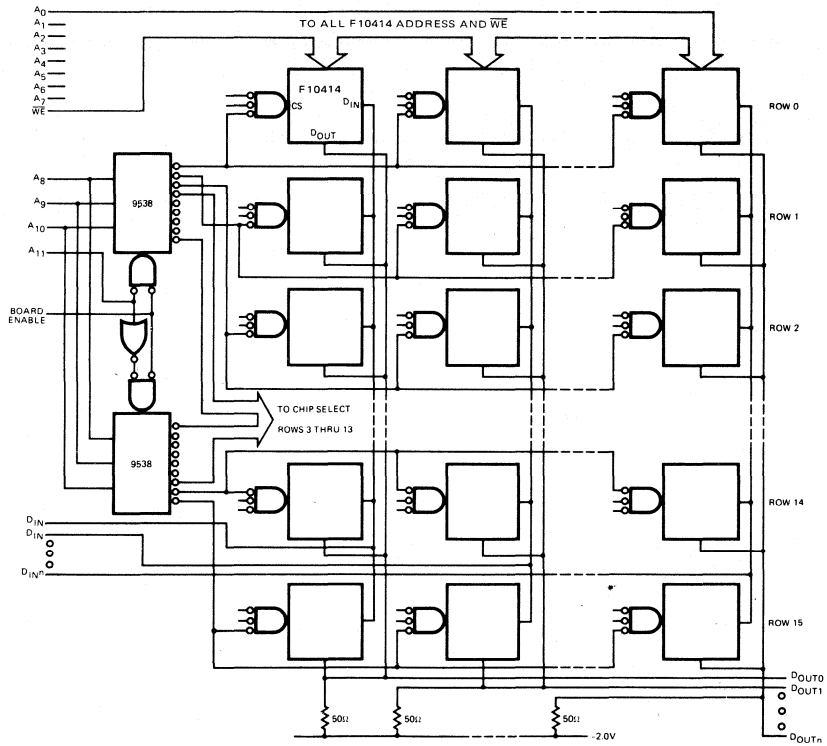


Fig. 3.

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ECL ISOPLANAR MEMORY F10415 / F10415A

1024×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

FAIRCHILD VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION – The F10415 and F10415A are 1024-bit Read/Write Random Access Memories organized 1024 words by one bit. They are designed for high speed scratch pad, control and buffer storage applications. Both include full address decoding on the chip, have separate Data In and non-inverted Data Out lines, and active LOW Chip Select lines. They are compatible with F10K and uncompensated 10K ECL families and include on-chip voltage compensation for improved noise margin.

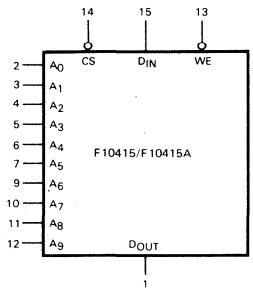
The F10415 and F10415A are packaged in a hermetic ceramic 16-pin dual in-line package and are specified for operation over the temperature range 0°C to 75°C.

- **COMPATIBLE WITH F10K AND UNCOMPENSATED 10K ECL LOGIC**
- **TYPICAL READ ACCESS TIME**
  F10415 – 25 ns
  F10415A – 12 ns
- **TYPICAL CHIP SELECT ACCESS TIME**
  F10415 – 7 ns
  F10415A – 5 ns
- **ORGANIZED 1024 WORDS X 1 BIT**
- **OPEN EMITTER OUTPUT FOR EASE OF MEMORY EXPANSION**
- **POWER DISSIPATION 0.5 mW/BIT**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**

PIN NAMES

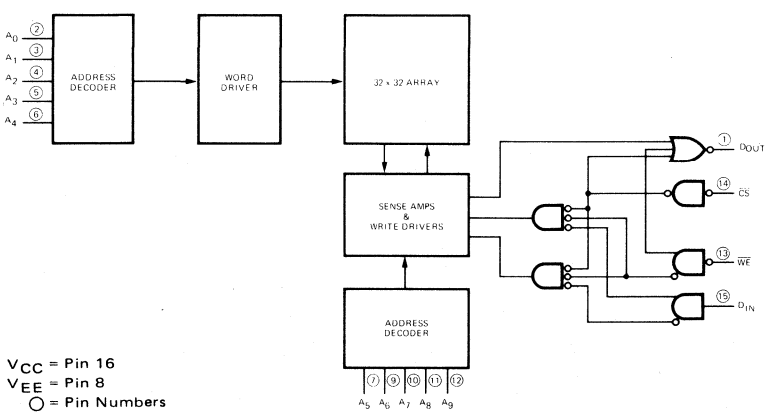
$\overline{CS}$	Chip Select Input
A_0 to A_9	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

LOGIC SYMBOL



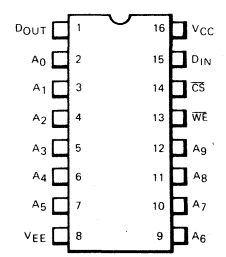
V_{CC} = Pin 16
V_{EE} = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
V_{EE} = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The F10415 and F10415A are fully decoded 1024-bit Read/Write Random Access Memories organized 1024 words by one bit. Bit selection is acheived by means of a 10-bit address, A_0 to A_9. One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select access time permits the decoding of Chip Select ($\overline{CS}$) from the address without increasing address access time. The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$). With $\overline{WE}$ and $\overline{CS}$ held LOW, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and $\overline{CS}$ held LOW. Data in the specified location is presented at D_{OUT} and is non-inverted.

An unterminated emitter-follower output is provided on the F10415 and F10415A to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F10415s or F10415As can be tied together. In other applications the wired-OR is not used. In either case an external 50 Ω pull down resistor to –2 V or an equivalent network must be used to provide a LOW at the output when it is off.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{EE} Pin Potential to Ground Pin	–7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	–30 mA to +0.1 mA

TABLE 1 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	OPEN EMITTER	
H	X	X	L	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	L	WRITE "1"
L	H	X	D_{OUT}	READ

L = LOW Voltage Levels = –1.7 V
H = HIGH Voltage Levels = –0.9 V
(Nominal values)
X = Don't Care

GUARANTEED OPERATING RANGES

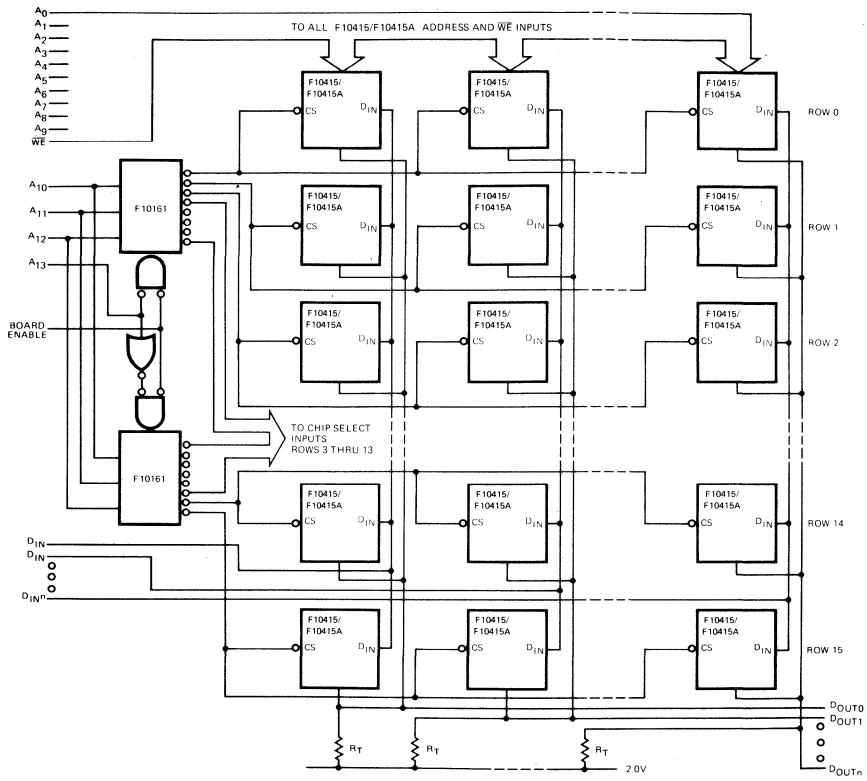
PART NUMBER	SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	See Note 4
F10415DC, F10415ADC	–5.46 V	–5.2 V	–4.94 V	0°C to 75°C

DC CHARACTERISTICS: V_{EE} = –5.2 V, Output Load = 50 Ω and 30 pF to –2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	B LIMIT	TYP (Note 3)	A LIMIT	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	–1000		–840	mV	0°C	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to –2.0 V
		–960		–810		+25°C		
		–900		–720		+75°C		
V_{OL}	Output Voltage LOW	–1870		–1665	mV	0°C		
		–1850		–1650		+25°C		
		–1830		–1625		+75°C		
V_{OHC}	Output Voltage HIGH	–1020			mV	0°C	$V_{IN} = V_{IHB}$ or V_{ILA}	
		–980				+25°C		
		–920				+75°C		
V_{OLC}	Output Voltage LOW			–1645	mV	0°C		
				–1630		+25°C		
				–1605		+75°C		
V_{IH}	Input Voltage HIGH	–1145		–840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		–1105		–810		+25°C		
		–1045		–720		+75°C		
V_{IL}	Input Voltage LOW	–1870		–1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		–1850		–1475		+25°C		
		–1830		–1450		+75°C		
I_{IH}	Input Current HIGH			220	μA	0 to +75°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW, $\overline{CS}$	0.5		170	μA	+25°C	$V_{IN} = V_{ILB}$	
	All others	–50						
I_{EE}	Power Supply Current		–90		mA	+75°C	All Inputs and Outputs Open	
	(Pin 8)	–150	–105			0°C		

NOTES:
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified Limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{EE} = –5.2 V, T_A = 25°C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET:
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.

APPLICATIONS(Cont'd)



16,384-WORD X n-BIT SYSTEM
Fig. 4

ECL ISOPLANAR MEMORY F10470

4096 × 1-BIT FULLY DECODED RANDOM ACCESS MEMORY

FAIRCHILD VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION – The F10470 is a 4096-bit Read/Write Random Access Memory organized 4096 words by one bit. It is designed for high speed scratch pad, control and buffer storage applications. The Device includes full address decoding on the chip, has separate Data In and non-invertered Data Out lines, and active LOW Chip Select lines. They are compatible with F10K and uncompensated 10K ECL families and include on-chip voltage compensation for improved noise margin.

The F10470 is packaged in a hermetic ceramic 18-pin dual in-line package and is specified for operation over the temperature range 0°C to 75°C.

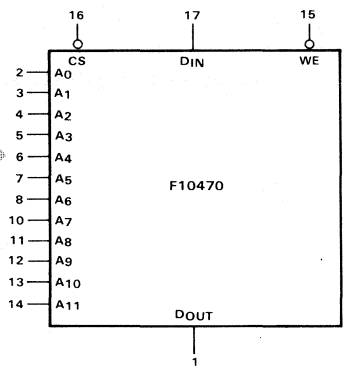
- **COMPATIBLE WITH F10K AND UNCOMPENSATED 10K ECL LOGIC**
- **TYPICAL READ ACCESS TIME – 30 ns**
- **TYPICAL CHIP SELECT ACCESS TIME – 10 ns**
- **ORGANIZED 4096 WORDS X 1 BIT**
- **OPEN EMITTER OUTPUT FOR EASE OF MEMORY EXPANSION**
- **POWER DISSIPATION 0.25 mW/BIT**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**
- **REPLACES FOUR 1024 BY ONE RAMs**

PIN NAMES

$\overline{CS}$	Chip Select Input
$A_0 - A_{11}$	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

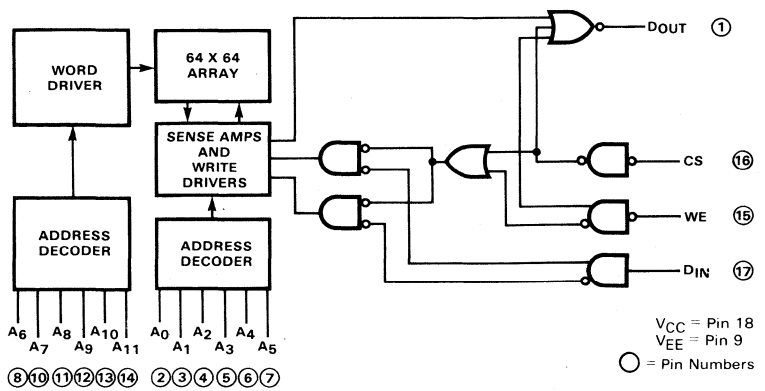
PRELIMINARY

LOGIC SYMBOL



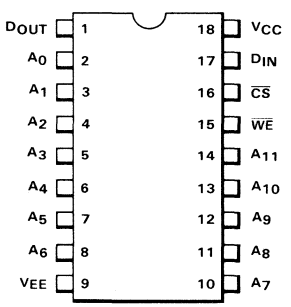
V_{CC} = Pin 18
V_{EE} = Pin 9

LOGIC DIAGRAM



V_{CC} = Pin 18
V_{EE} = Pin 9
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

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READ MODE PROPAGATION DELAY FROM CHIP SELECT

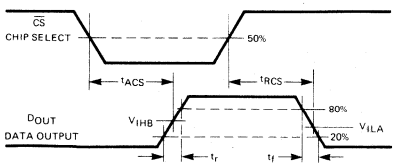


Fig. 1a

READ MODE PROPAGATION DELAY FROM ADDRESS

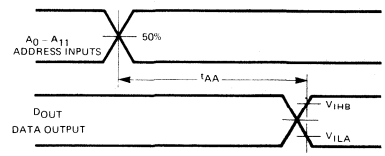


Fig. 1b

WRITE MODE

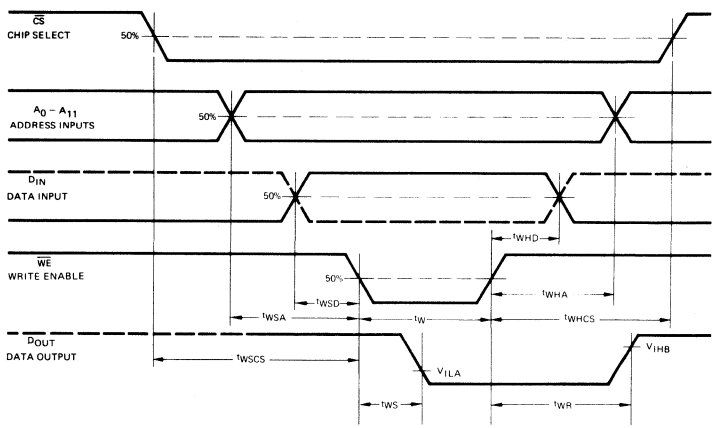


Fig. 2

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

F100142

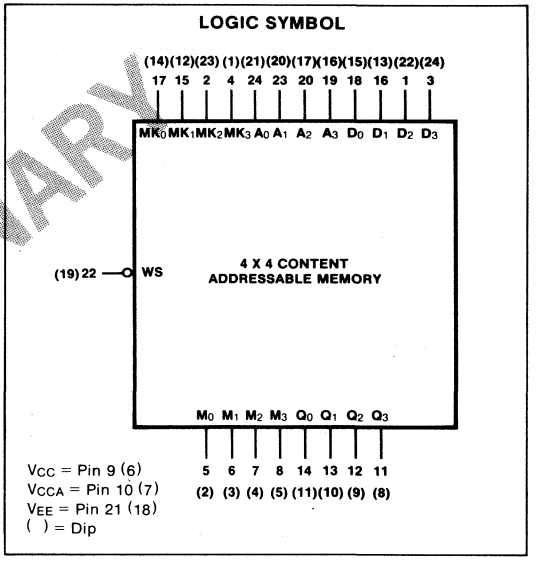
4 x 4 CONTENT ADDRESSABLE MEMORY

F100K SERIES ECL

)ESCRIPTION — The F100142 is a 4 word x 4 bit Content Addressable Memory (CAM). Each Word location has its own Address Select ne. Reading or Writing is accomplished when the Address Select line s LOW. In the Read mode, Data from the addressed location appears t the Data (Q_i) outputs. In the Write mode, Data is stored in the ddressed location. A LOW Write Strobe selects the Write mode, a IIGH Write Strobe selects the Read mode. Each Data input has its wn Mask input that blocks data storage when the Mask is HIGH. The)ata input word is simultaneously compared with each of the four nemory Words. If a Search Compare results in a Match, this output vill go LOW. A HIGH Mask input on any bit forces a Match of that bit. :ach input has a 50 k Ω (typical) pull-down resistor tied to V_{EE}. The)utputs require external resistance terminations as they are not erminated internally through resistance to the V_{EE} supply.

PRELIMINARY

LOGIC SYMBOL

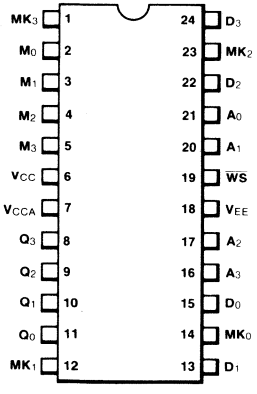


IN NAMES

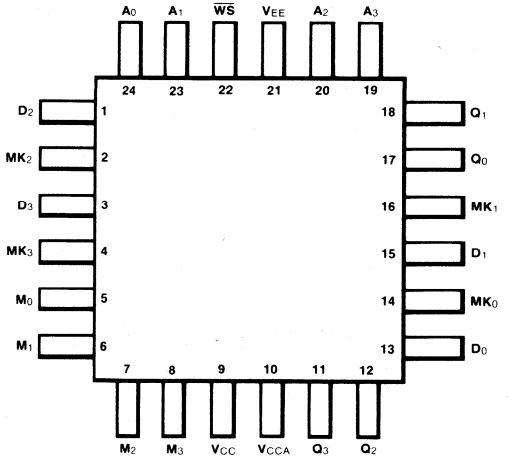
MK_n	Data Mask Inputs
A_n	Address Inputs
D_n	Data Inputs
M_n	Match Outputs
Q_n	Data Outputs
$\overline{WS}$	Write Strobe

CONNECTION DIAGRAM

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



11

AC CHARACTERISTICS: $T_A = 25°C$, $V_{EE} = -4.5$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{AH}	Address Hold After Write Time		0.0		ns	
t_{MH}	Mask In Hold To Inhibit Write Time		1.2		ns	Figure 2
t_{AD}	Address To Data Out		2.7		ns	Figure 2, 3
t_{DM}	Data In To Match Out Time		3.3		ns	
t_{MM}	Mask In To "Enable Partial" Match Out Time		2.2		ns	Figure 4
t_{AS}	Address Set Up Before Write Time		0.0		ns	
t_{DS}	Data In Setup Before Write Time		-0.2		ns	Figure 2
t_{MS}	Mask In Setup To Inhibit Write Time		-1.1		ns	
t_W	Write Pulse Width		2.0		ns	Figure 1
t_{DD}	Data In To New Data Out		5.0		ns	
t_{WD}	Write To New Data Out		5.0			Figure 2
t_{DH}	Data In Hold After Write Time		0.5			
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%			1.0	ns	Figure 1

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING WAVEFORMS

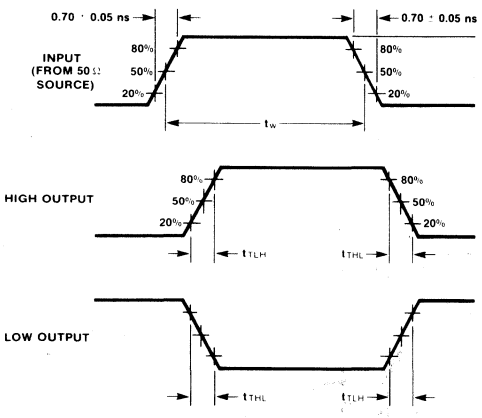


Fig. 1 Output Rise and Fall Times and Waveforms

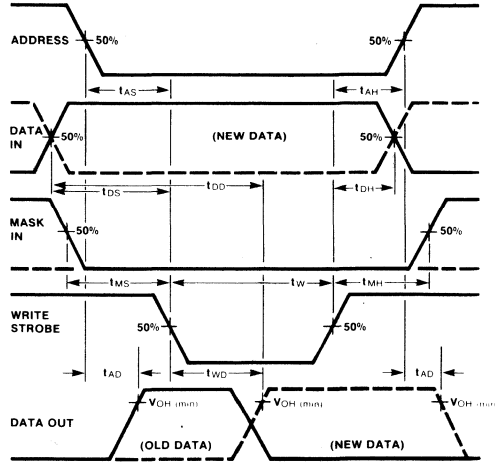


Fig. 2 Write Mode and Read/Write Mode Waveforms

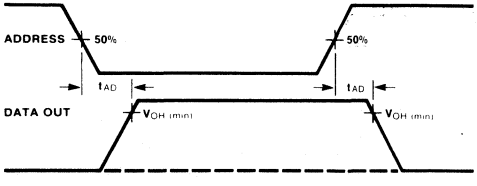


Fig. 3 Read Mode Waveforms

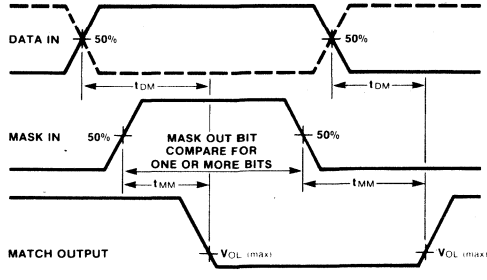


Fig. 4 Search Mode Waveforms

F100145

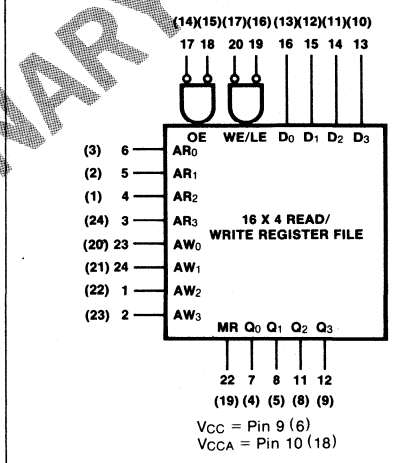
16×4 READ/WRITE REGISTER FILE

F100K SERIES ECL

DESCRIPTION — The F100145 is a 64-bit Register File organized as 16 words of four bits each. Separate address inputs for Read (AR_n) and Write (AW_n) operations reduce overall cycle time by allowing one address to be setting-up while the other is being executed. Operating speed is also enhanced by four output latches which store data from the previous read operation while writing is in progress. When both Write Enable ($\overline{WE}$) inputs are LOW, the circuit is in the WRITE mode and the latches are in a HOLD mode. When either $\overline{WE}$ input is HIGH, the circuit is in the READ mode, but the outputs can be forced LOW by a HIGH signal on either of the Output Enable ($\overline{OE}$) inputs. This makes it possible to tie one $\overline{WE}$ input and one $\overline{OE}$ input together to serve as an active LOW Chip Select ($\overline{CS}$) input. When this wired $\overline{CS}$ input is HIGH, reading will still take place internally and the resulting data will enter the latches and become available as soon as the $\overline{CS}$ signal goes LOW, provided that the other $\overline{OE}$ input is LOW. A HIGH signal on the Master Reset (MR) input overrides all other inputs, clears all cells in the memory, resets the output latches and forces the outputs LOW.

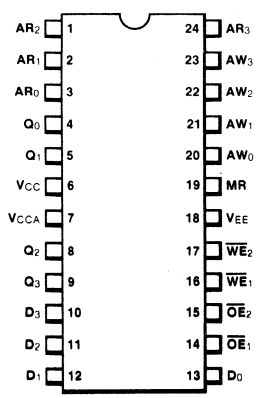
PRELIMINARY

LOGIC SYMBOL

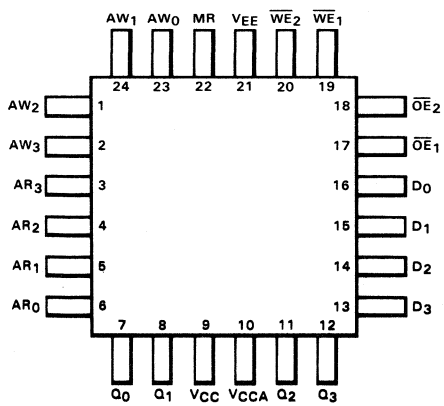


CONNECTION DIAGRAMS

DIP (TOP VIEW)

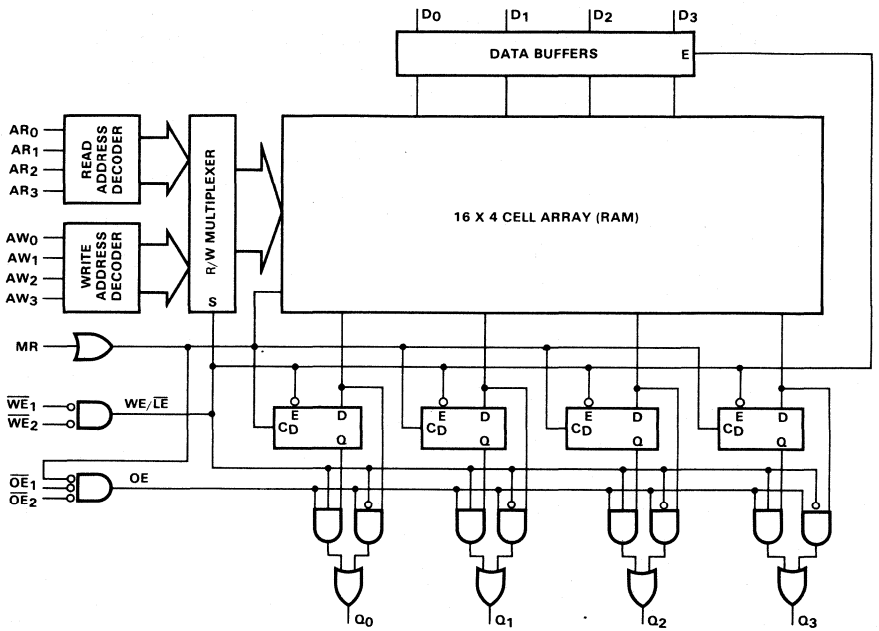


FLATPAK (TOP VIEW)



11

LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than indicated.

DC CHARACTERISTICS: V_{EE} = -4.5 V, V_{CC} = GND, T_A = 0°C to +85°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH WE/$\overline{LE}$ Other Inputs			 270 220	μA	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	-119	-170	-247	mA	Inputs open

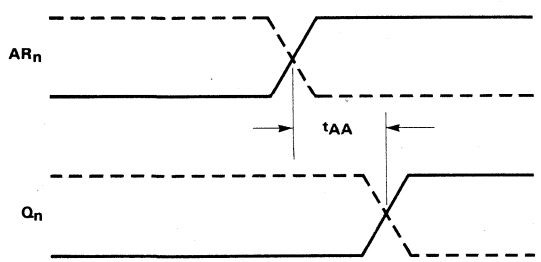
AC CHARACTERISTICS: $T_A = 25°C$, $V_{EE} = -4.5$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
	Access/Recovery Timing					
t_{AA}	Address Access		5.5		ns	Figure 1a
t_{OR}	Output Recovery		2.2		ns	Figure 1e
t_{OD}	Output Disable		2.2		ns	
	Read Timing					
t_{RSA1}	Address Set-up		2.0		ns	Figure 1b
t_{WEQ}	Output Delay		4.5		ns	
	Output Latch Timing					
t_{RSA2}	Address Set-up		5.5		ns	Figure 1c
t_{RHA}	Address Hold		-5.0		ns	Figure 1d
	Write Timing					
t_{WSA}	Address Set-up		2.0		ns	Figure 2a
t_{WHA}	Address Hold		-0.5		ns	
t_{WSD}	Data Set-up		6.0		ns	
t_{WHD}	Data Hold		-2.5		ns	
t_W	Write Pulse Width, Min		4.0		ns	
t_{SW}	$\overline{WE}$ to $\overline{WE}$ Set-up		0		ns	Figure 2b
t_{HW}	$\overline{WE}$ to $\overline{WE}$ Hold		0		ns	
	Master Reset Timing					
t_M	Reset Pulse Width, Min		9.0		ns	Figure 3a
t_{MHW}	$\overline{WE}$ Hold to Write		14		ns	
t_{MQ}	Output Disable		2.7		ns	Figure 3b

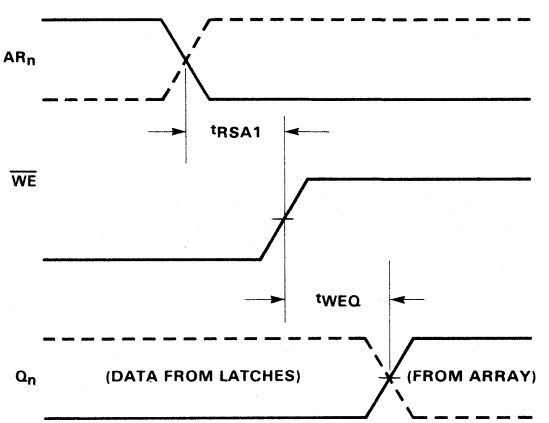
NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

100145 TIMING RELATIONSHIPS

a) Address access time ($\overline{WE}_1$, or $\overline{WE}_2$ = HIGH; $\overline{OE}_1 = \overline{OE}_2$ = LOW)



b) Address set-up time before $\overline{WE}$, to ensure min delay (unpulsed $\overline{WE} = \overline{OE}_1 = \overline{OE}_2$ = LOW)



c) Address set-up time to ensure latching data from new address (unpulsed $\overline{WE}$ = LOW)

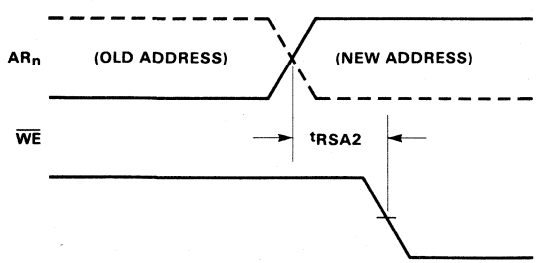
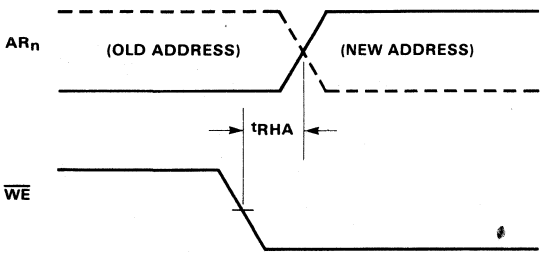


Fig. 1 Read Timing

11

TIMING RELATIONSHIPS (Cont'd)

d) Address hold time to ensure latching data from old address (unpulsed $\overline{WE}$ = LOW)



e) Output recovery/disable times, OE to Q_n (unpulsed OE = LOW)

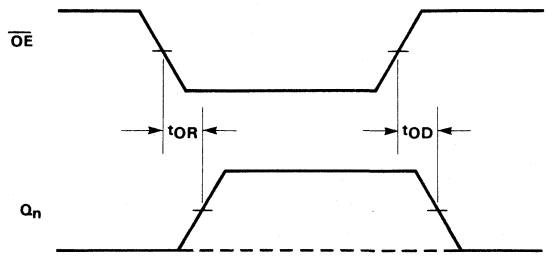
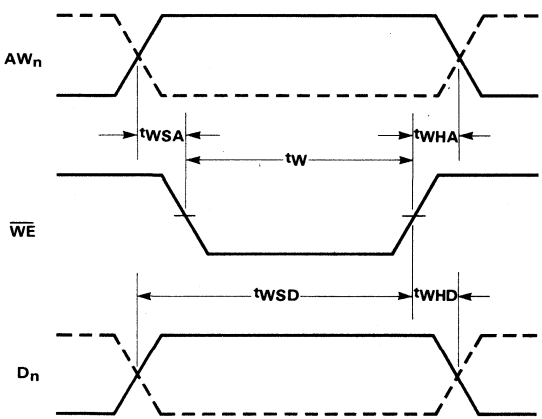


Fig. 1 Read Timing (Cont'd)

a) Address and data set-up and hold times; write pulse width (unpulsed $\overline{WE}$ = LOW)



b) $\overline{WE}$ set-up and hold times, write with other $\overline{WE}$

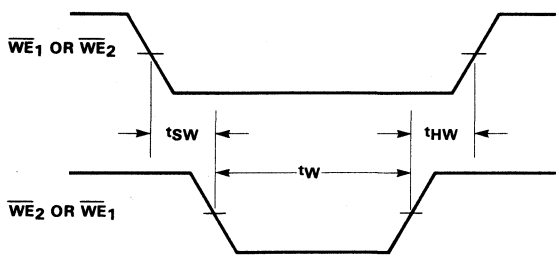
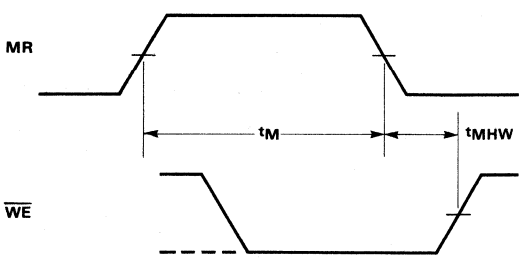


Fig. 2 Write Timing

a) *Reset pulse width; $\overline{WE}$ hold time for subsequent writing* (address already set-up, unpulsed $\overline{WE}$ = LOW)



b) *Output reset delay, MR to Q_n*

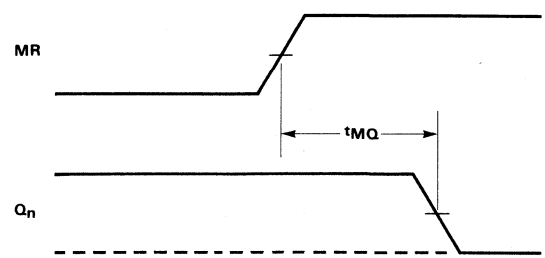


Fig. 3 Master Reset Timing

ECL ISOPLANAR MEMORY F100414

256 × 1-BIT FULLY DECODED RANDOM ACCESS MEMORY

FAIRCHILD TEMPERATURE AND VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION – The F100414 is a 256-bit Read/Write Random Access Memory, organized 256 words by one bit. It has typical access time of 7 ns and is designed for high speed scratch pad, control and buffer storage applications. The device includes full address decoding on the chip, has separate Data In and non-inverted Data Out lines, and has three active LOW Chip Select lines.

With on chip voltage and temperature compensation the F100414 is compatible with the F100K and F95K series of ECL Logic. The device is packaged in the hermetic ceramic 16-pin dual in-line or 16-pin flat package and specified for operation over the temperature range 0° to 85°C.

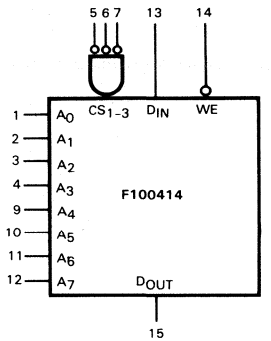
- **VERY HIGH SPEED**
- **COMPATIBLE WITH F100K and F95K ECL LOGIC**
- **READ ACCESS TIME – 7 ns TYP**
- **CHIP SELECT ACCESS TIME – 4 ns TYP**
- **POWER DISSIPATION – 1.8 mW/BIT**
- **50 kΩ INPUT PULL-DOWN RESISTORS ON CHIP SELECT**
- **OUTPUTS CAN BE WIRED-OR FOR EASY MEMORY EXPANSION**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**
- **ORGANIZED – 256 WORDS X 1 BIT**

PIN NAMES

$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$	Chip Select Inputs
$A_0 - A_7$	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

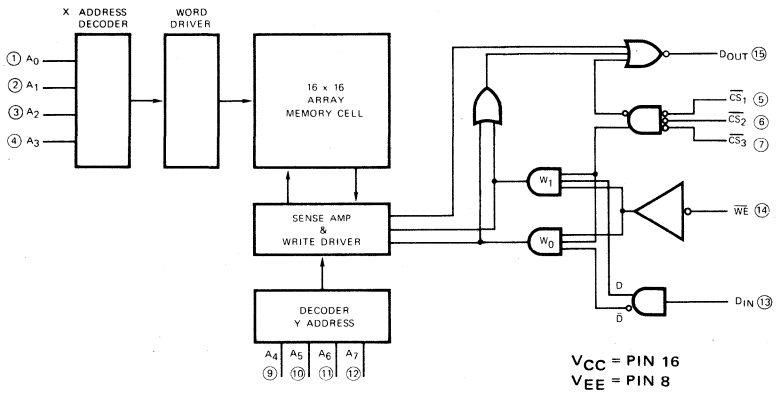
PRELIMINARY

LOGIC SYMBOL



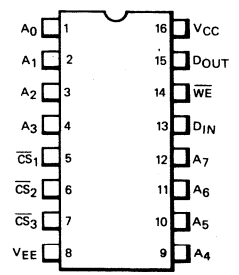
V_{CC} = PIN 16
V_{EE} = PIN 8

LOGIC DIAGRAM



V_{CC} = PIN 16
V_{EE} = PIN 8
○ = PIN NUMBERS

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

11

FUNCTIONAL DESCRIPTION – The F100414 is a fully decoded 256-bit Read/Write Random Access Memory, organized 256 words by one bit. Word selection is achieved by means of an 8-bit address A_0 to A_7.

The active LOW chip select inputs are provided for increased logic flexibility. This permits memory array expansion up to 2048 words with the 10161 decoder. For larger memories, the fast chip select time permits the decoding of Chip Select, $\overline{CS}$, from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable, ($\overline{WE}$, pin 14). With $\overline{WE}$ held LOW, and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH, and the chip selected. Data in the addressed location is presented at D_{OUT} and is read out non-inverted. The D_{OUT} is LOW except when reading a stored HIGH.

Open emitter outputs are provided on the F100414 to allow maximum flexibility in output wired-OR connection for memory expansion.

TABLE 1 – TRUTH TABLE

INPUT					OUTPUT	MODE
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}		
X	X	H*	X	X	L	NOT SELECTED
L	L	L	L	L	L	WRITE "0"
L	L	L	L	H	L	WRITE "1"
L	L	L	H	X	D_{OUT}	READ

*One or more Chip Selects HIGH

NOTE:
L = LOW Voltage Levels = –1.7 V
H = HIGH Voltage Levels = –0.9 V (Nominal Values)
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to 150°C
Temperature (Ambient) Under Bias	–55°C to 125°C
V_{EE} Pin Potential to Ground Pin	–7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	–30 mA to +0.1 mA

GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE SEE NOTE 4
MIN	TYP	MAX	
–5.7 V	–4.5 V	–4.2 V	0°C to 85°C

DC CHARACTERISTICS: V_{EE} = –4.5 V, V_{CC} = GND, T_A = 0°C +85°C, output load 50 Ω to –2.0 V

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output HIGH Voltage	–1025	–955	–880	mV	V_{IN} = V_{IHA} or V_{ILB}	Loading is 50 Ω to –2.0 V
V_{OL}	Output LOW Voltage	–1810	–1705	–1620	mV		
V_{OHC}	Output HIGH Voltage	–1035			mV	V_{IN} = V_{IHB} or V_{ILA}	
V_{OLC}	Output LOW Voltage			–1610	mV		
V_{IH}	Input HIGH Voltage	–1165		–880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	–1810		–1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IH}	Input HIGH Current			220	μA	V_{IN} = V_{IHA}	
I_{IL}	Input LOW Current, $\overline{CS}$ All others	0.5 –50		170	μA	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current		–100		mA	All inputs and output open	

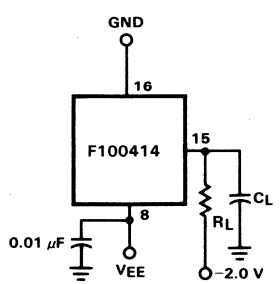
AC CHARACTERISTICS: V_{EE} = −4.5 V, ±10% → Output Load = 50 Ω 10 pF to −2.0 V

SYMBOL	PARAMETER	MIN LIMIT	TYP (Note 3)	MAX LIMIT	UNITS	CONDITIONS
READ MODE						
t_{ACS}	Chip Select Access Time		4		ns	Fig. 1a & b Measured at 50% of Input to Valid Output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH}). Note 5.
t_{RCS}	Chip Select Recovery Time		4		ns	
t_{AA}	Address Access Time		7		ns	
WRITE MODE						
t_W	Write Pulse Width	6	4		ns	t_{WSA} = 3 ns
t_{WSD}	Data Set-up Time Prior to Write		0		ns	
t_{WHD}	Data Hold Time After Write		0		ns	
t_{WSA}	Address Set-up Time		1		ns	t_W = 6 ns Fig. 2 Measured at 50% of Input to Valid Output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})
t_{WHA}	Address Hold Time		0		ns	
t_{WSCS}	Chip Select Set-up Time		0		ns	
t_{WHCS}	Chip Select Hold Time		1		ns	
t_{WS}	Write Disable Time		4		ns	
t_{WR}	Write Recovery Time		5		ns	
RISE AND FALL TIME						
t_r	Output Rise Time		4		ns	Measured between 20% & 80% points. (Fig. 1a)
t_f	Output Fall Time		4		ns	
CAPACITANCE						
C_{IN}	Input Lead Capacitance		4		pF	Measure with a Pulse Technique
C_{OUT}	Output Lead Capacitance		7		pF	

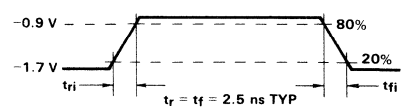
NOTES:
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{EE} = −5.2 V, T_A = +25°C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and two minute warm up period. Typical thermal resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET:
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
   "A" the value closest to positive infinity.
   "B" the value closest to negative infinity.

AC TEST LOAD AND WAVEFORMS

LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels
C_L = 10 pF including Jig and Stray Capacitance
R_L = 50 Ω to −2.0 V

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READ MODE PROPAGATION DELAY
FROM CHIP SELECT

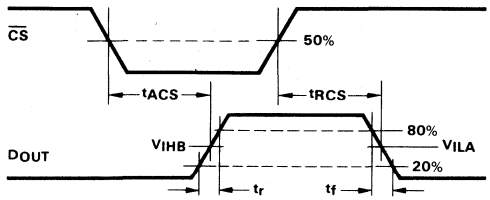


Fig. 1a

READ MODE PROPAGATION DELAY
FROM ADDRESS

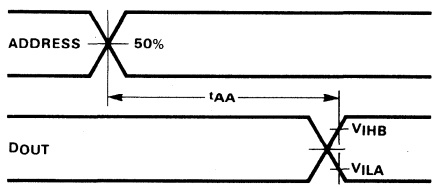


Fig. 1b

WRITE MODE

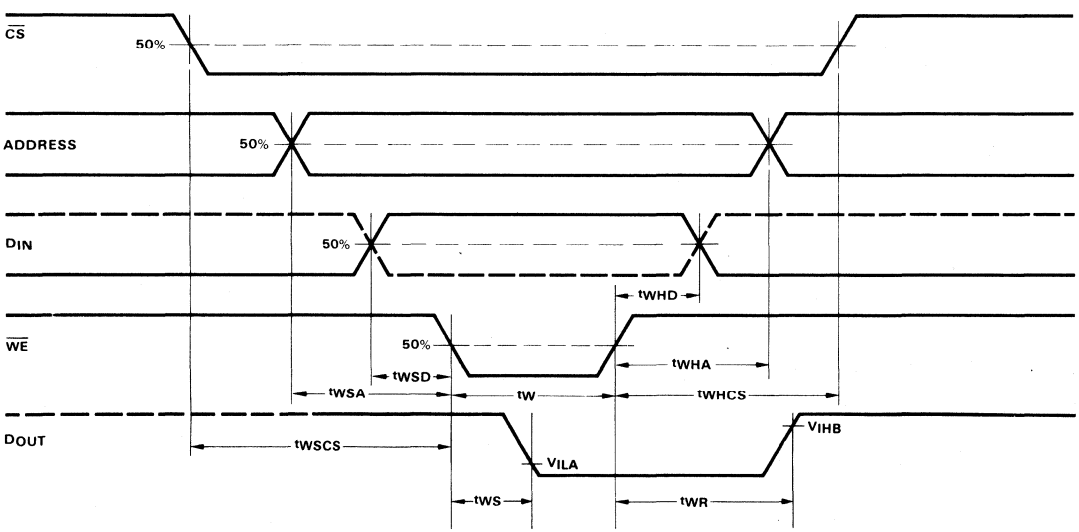


Fig. 2

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

4096 WORD X N–BIT SYSTEM

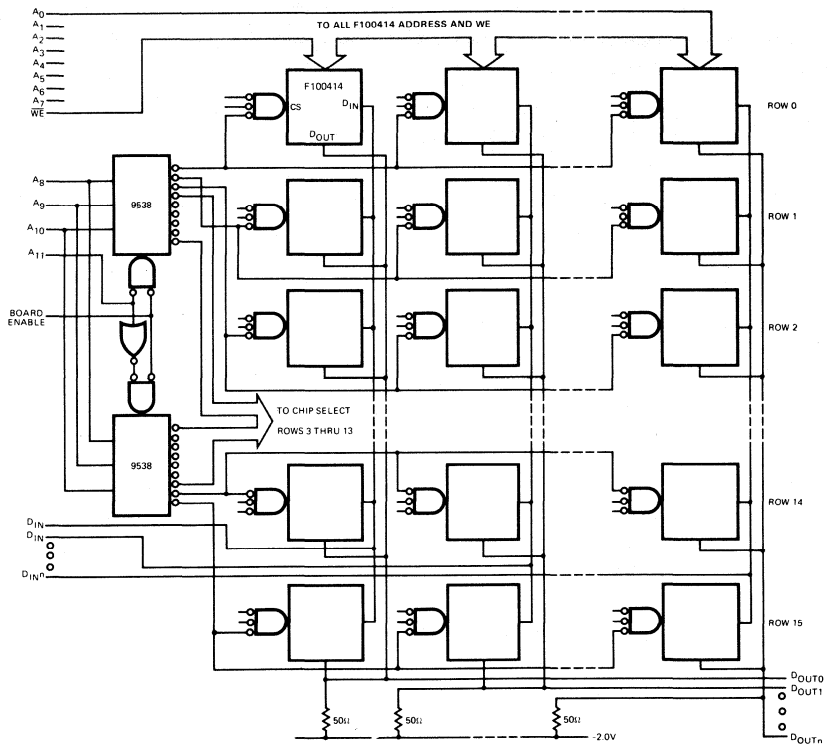


Fig. 3.

F100415
ECL ISOPLANAR MEMORY
1024×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION – The F100415 is a 1024-bit Read/Write Random Access Memory organized 1024 words by one bit per word. Designed for high speed scratchpad, control and buffer storage applications. The device is specified with a maximum read cycle time of 20 ns over the commercial temperature and voltage range.

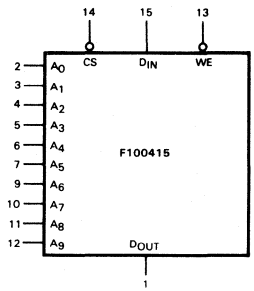
With on-chip voltage and temperature compensation, this memory is compatible with the F100K and F95K Series of ECL logic.

Other features include full address decoding on chip, separate Data In and non-inverting Data Out lines, and an active LOW Chip Select input.

The F100415 is packaged in a hermetic ceramic 16-pin dual in-line package and is specified for operation over the 0°C to +85°C temperature range.

- **COMPATIBLE WITH F100K AND F95K ECL LOGIC**
- **MAXIMUM CYCLE TIME OF 20 ns OVER TEMPERATURE**
- **OPEN EMITTER OUTPUTS FOR EASE OF MEMORY EXPANSION**
- **ORGANIZATION – 1024 WORDS X 1 BIT**
- **POWER DISSIPATION OF 0.5 mW/BIT**

LOGIC SYMBOL

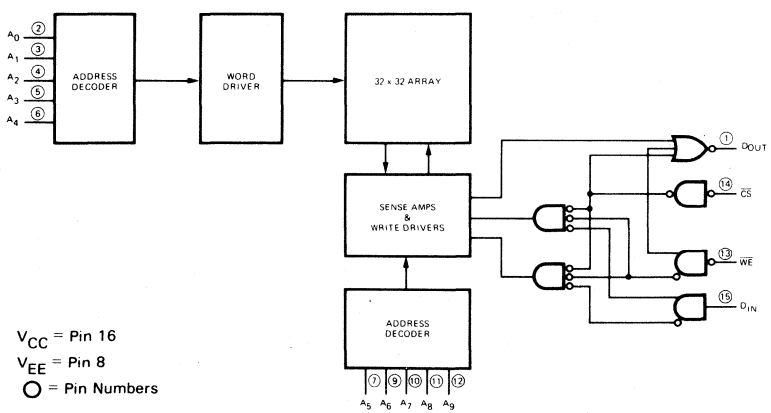


V_{CC} = Pin 16
V_{EE} = Pin 8

PIN NAMES

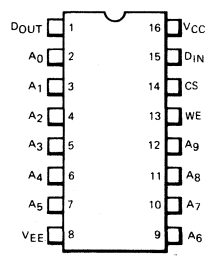
$\overline{CS}$	Chip Select Input
A_0 to A_9	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

LOGIC DIAGRAM



V_{CC} = Pin 16
V_{EE} = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The F100415 is a fully decoded 1024-bit Read/Write Random Access Memory organized 1024 words by one bit. Bit selection is acheived by means of a 10-bit address, A_0 to A_9. One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select ($\overline{CS}$) form the address without increasing address access time. The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$). With $\overline{WE}$ and $\overline{CS}$ held LOW, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and $\overline{CS}$ held LOW. Data in the specified location is presented at D_{OUT} and is non-inverted.

An unterminated emitter-follower output is provided on the F100415 to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F100415 can be tied together. In other applications the wired-OR is not used. In either case an external 50 Ω pull down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is off.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{EE} Pin Potential to Ground Pin	−7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	−30 mA to +0.1 mA

TABLE 1 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	OPEN EMITTER	
H	X	X	L	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	L	WRITE "1"
L	H	X	D_{OUT}	READ

L = LOW Voltage Levels = −1.7 V
H = HIGH Voltage Levels = −0.9 V
(Nominal values)
X = Don't Care

GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE NOTE 4
MIN	TYP	MAX	
−5.7 V	−4.5 V	−4.2 V	0°C to 85°C

DC CHARACTERISTICS: V_{EE} = −4.5V, V_{CC} = GND, T_A = 0°C to +85°C (Note A)

SYMBOL	CHARACTERISTIC	LIMITS (Note 6)			UNITS	CONDITIONS	
		B	TYP (Note 3)	A			
V_{OH}	Output Voltage HIGH	−1025	−955	−880	mV	V_{IN} = V_{IHA} or V_{ILB}	Loading is 50 Ω to −2.0 V
V_{OL}	Output Voltage LOW	−1810	−1705	−1620	mV		
V_{OHC}	Output Voltage HIGH	−1035			mV	V_{IN} = V_{IHB} or V_{ILA}	
V_{OLC}	Output Voltage LOW			−1610	mV		
V_{IH}	Input Voltage HIGH	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input Voltage LOW	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IH}	Input Current HIGH			220	μA	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW, $\overline{CS}$ All others	0.5 −50		170	μA	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	−150	−105		mA	All Inputs and Output open	

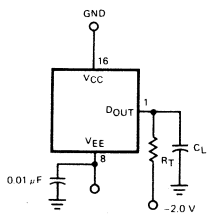
NOTES:
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified Limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{EE} = −5.2 V, T_A = 25°C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET:
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.

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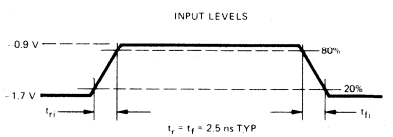
AC CHARACTERISTICS: V_{EE} = −4.5 V, T_A = 0°C to 85°C, V_{CC} = GND

SYMBOL	PARAMETER	MIN	TYP (Note 3)	MAX	UNITS	CONDITIONS
t_{ACS}	Chip Select Access Time		5		ns	Fig 1a and b measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} or V_{OH})
t_{RCS}	Chip Select Recovery Time		5		ns	
t_{AA}	Address Access Time		12	20	ns	
t_W	Write Pulse Width (to Guarantee writing)	12	9		ns	t_{WSA} = 8 ns
t_{WSD}	Data Sep-up Time Prior to Write		0		ns	
t_{WHD}	Data Hold Time After Write		0			
t_{WSA}	Address Set-up Time Prior to Write		5		ns	t_W = 12 ns
t_{WHA}	Address Hold Time After Write		0		ns	
t_{WSCS}	Chip Select Set-up Time Prior to Write		0		ns	
t_{WHCS}	Chip Select Hold Time After Write		0		ns	Fig. 2 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})
t_{WS}	Write Disable Time		5		ns	
t_{WR}	Write Recovery Time		10		ns	
t_r	Output Rise Time		4.5		ns	Measured between 20% and 80% points. (Fig. 1a)
t_f	Output Fall Time		5.5		ns	
C_{IN}	Input Pin Capacitance		4	5	pF	Measure with a Pulse Technique
C_{OUT}	Output Pin Capacitance		7	8	pF	

LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels

C_L = 30 pF including Jig and Stray Capacitance

R_T = 50 Ω Termination of Scope

READ MODE PROPAGATION DELAY FROM CHIP SELECT

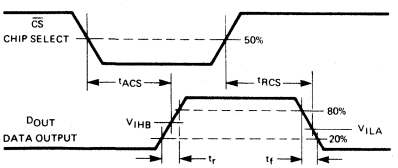


Fig. 1a

READ MODE PROPAGATION DELAY FROM ADDRESS

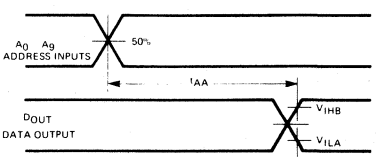


Fig. 1b

WRITE MODE

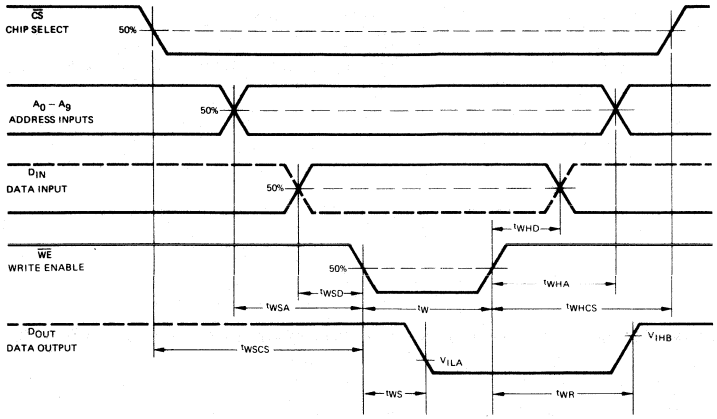
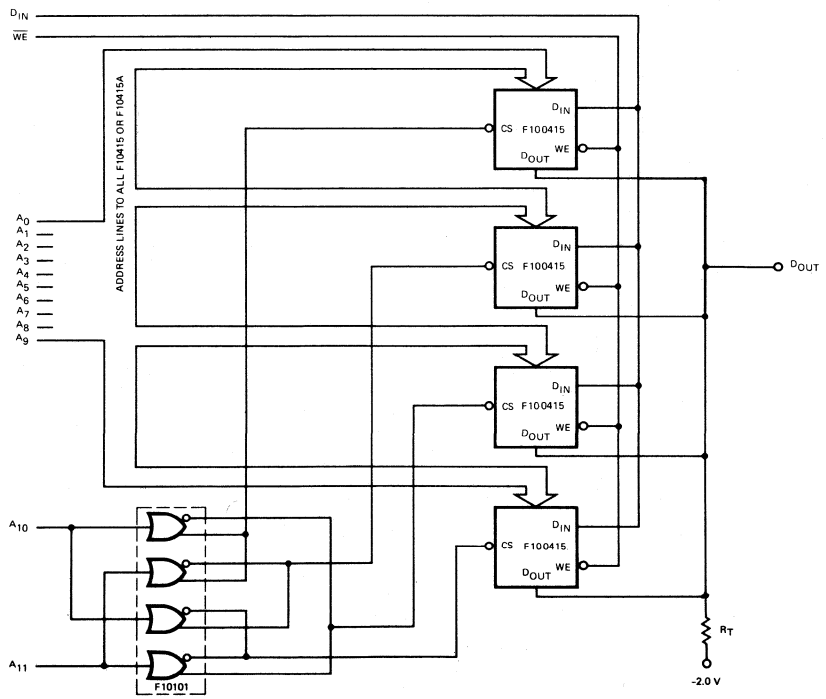


Fig. 2

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

APPLICATIONS



4096-WORD X 1-BIT SYSTEM

Fig. 3

F10416 / F100416

ECL ISOPLANAR MEMORY

256×4-BIT PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION – The F10416 and F100416 are fully decoded high speed 1024-bit field Programmable Read Only Memories, organized 256 words by four bits. The F10416 is voltage compensated and compatible with 10K ECL families. The 100416 is voltage and temperature compensated and compatible with the F100K family. Either device is enabled when $\overline{CS}$ is LOW. Prior to programming, all outputs are active HIGH in the enabled state. Programmed bits will furnish LOW levels at corresponding outputs. When either device is disabled ($\overline{CS}$ is HIGH) all outputs are forced LOW.

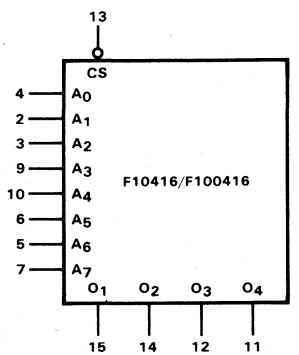
PRELIMINARY

- **ADVANCED ISOPLANAR PROCESS**
- **FAST CYCLE TIME – 15 ns TYP**
- **ORGANIZATION – 256 WORDS X 4 BITS**
- **F10K AND UNCOMPENSATED 10K ECL LOGIC – F10416**
- **F100K LOGIC – F100416**
- **CHIP SELECT INPUT PROVIDES EASY MEMORY EXPANSION**
- **OPEN EMITTER OUTPUTS FOR MEMORY EXPANSION**
- **STANDARD 16-PIN DUAL IN-LINE PACKAGE**
- **FULL ADDRESS DECODING ON CHIP**

PIN NAMES

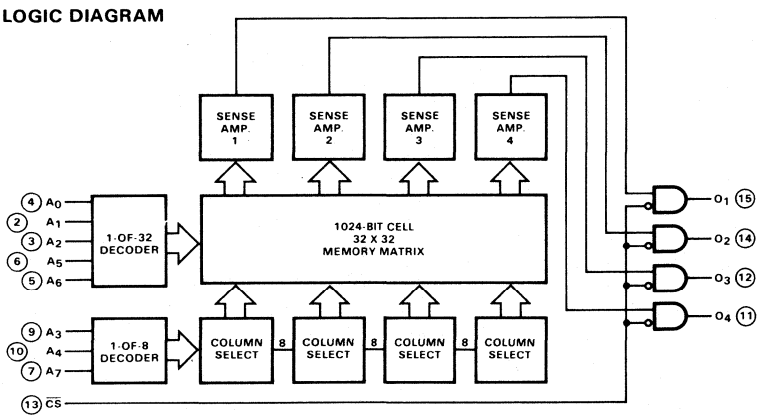
$\overline{CS}$	Chip Select Input
A_0 to A_7	Address Inputs
O_1 to O_4	Data Outputs

LOGIC SYMBOL



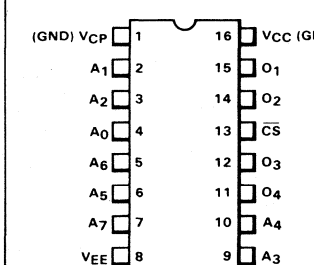
V_{CP} = GND (Read only) = Pin 1
V_{CP} = +12 V (Programming only) = Pin 1
V_{CC} = GND = Pin 16
V_{EE} = Pin 8

LOGIC DIAGRAM



V_{CP} = GND (Read only) = Pin 1
V_{CP} = +12 V (Programming only) = Pin 1
V_{CC} = GND = Pin 16
V_{EE} = Pin 8
◯ – Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
V_{CP} (Pin 1) is connected to the Programmer (+12 V) during programming only.

INTRODUCTION

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ECL CIRCUIT BASICS 2

ECL LOGIC DESIGN 3

TRANSMISSION LINE CONCEPTS 4

ECL INTERCONNECTIONS 5

POWER DISTRIBUTION AND THERMAL CONSIDERATIONS 6

F10K SERIES DATA SHEETS 7

F95K SERIES DATA SHEETS 8

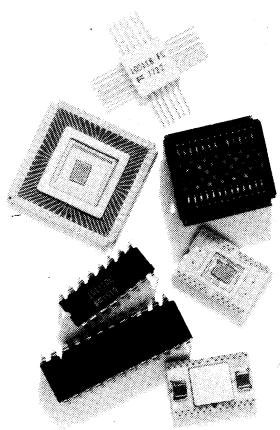
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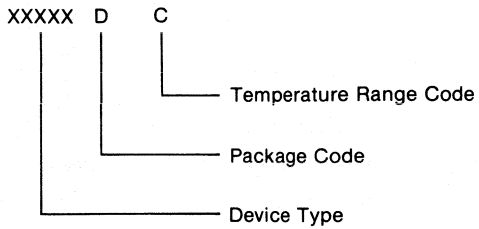
FAIRCHILD FIELD SALES OFFICES, REPRESENTATIVES AND DISTRIBUTORS 13



ORDER AND PACKAGE INFORMATION

Fairchild ECL may be ordered by using a simplified purchasing code where the package style and temperature range is defined as follows:

PACKAGE STYLE
D = Dual In-line — Ceramic (hermetic)
P = Dual In-line — Plastic
F = Flatpak



In order to accommodate varying die sizes and numbers of pins (14, 16, 24, etc.), a number of different package forms are required. The Package Information list on the following pages indicates the specific package codes currently used for device type. The detailed package outline corresponding to each package code is shown at the end of this section.

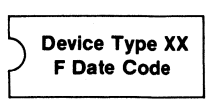
TEMPERATURE RANGES
Two basic temperature grades are in common use: C = Commercial-Industrial, 0°C to +75°C;/0°C to 85°C. M = Military, -55°C to +125°C. Exact values and conditions are indicated on the data sheets.

EXAMPLES:
(a) 10501FM
This number code indicates a QUAD OR/NOR in a flatpak with military temperature rating.

(b) 11C05DC
This number code indicates a 1 GHz, ÷ 4 Counter in a ceramic dual in-line package with commerical temperature rating.

(c) 10101PC
This number code indicates a Quad, OR/NOR in a plastic package with a commercial temperature rating.

DEVICE IDENTIFICATION/MARKING
All Fairchild standard catalog ECL will be marked as follows:



(XX) = Package and Temperature Range

10K ECL

MILITARY -55°C to +125°C			COMMERCIAL (C) INDUSTRIAL 0°C to 75°C			
DEVICE	Ceramic DIP (D)	Flatpak (F)	DEVICE	Ceramic DIP (D)	Plastic DIP (P)	Flatpak (F)
10000	6B	4L	10000	6B	9B	4L
10010	6B	4L	10010	6B	9B	4L
10014	6B	4L	10014	6B	9B	4L
10016	6B	4L	10016	6B	9B	4L
10500	6B	4L	10100	6B	9B	4L
10501	6B	4L	10101	6B	9B	4L
10502	6B	4L	10102	6B	9B	4L
10503	6B	4L	10103	6B	9B	4L
10504	6B	4L	10104	6B	9B	4L
10505	6B	4L	10105	6B	9B	4L
10506	6B	4L	10106	6B	9B	4L
10507	6B	4L	10107	6B	9B	4L
10509	6B	4L	10109	6B	9B	4L
10510	6B	4L	10110	6B	9B	4L
10511	6B	4L	10111	6B	9B	4L
10513	6B	4L	10113	6B	9B	4L
10514	6B	4L	10114	6B	9B	4L
10515	6B	4L	10115	6B	9B	4L
10516	6B	4L	10116	6B	9B	4L
10517	6B	4L	10117	6B	9B	4L
10518	6B	4L	10118	6B	9B	4L
10519	6B	4L	10119	6B	9B	4L
10521	6B	4L	10121	6B	9B	4L
10523	6B	4L	10123	6B	9B	4L
10524	6B	4L	10124	6B	9B	4L
10525	6B	4L	10125	6B	9B	4L
10530	6B	4L	10130	6B	9B	4L
10531	6B	4L	10131	6B	9B	4L
10532	6B	4L	10132	6B	9B	4L
10533	6B	4L	10133	6B	9B	4L
10534	6B	4L	10134	6B	9B	4L
10535	6B	4L	10135	6B	9B	4L
10536	6B	4L	10136	6B		4L
10537	6B	4L	10137	6B		4L
10541	6B	4L	10141	6B		4L
10545A	6B	4L	10145A	6B		4L
10553	6B	4L	10153	6B	9B	4L
10558	6B	4L	10158	6B	9B	4L
10559	6B	4L	10159	6B	9B	4L
10560	6B	4L	10160	6B	9B	4L
10561	6B	4L	10161	6B	9B	4L
10562	6B	4L	10162	6B	9B	4L
10564	6B	4L	10164	6B	9B	4L
10565	6B	4L	10165	6B	9B	4L
10566	6B	4L	10166	6B		4L
10568	6B	4L	10168	6B	9B	4L
10570	6B	4L	10170	6B		4L
10571	6B	4L	10171	6B	9B	4L
10572	6B	4L	10172	6B	9B	4L
10573	6B	4L	10173	6B	9B	4L

10K ECL

MILITARY -55°C to +125°C			COMMERCIAL (C) INDUSTRIAL 0°C to 75°C			
DEVICE	CERAMIC DIP (D)	FLATPAK (F)	DEVICE	CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
10574	6B	4L	10174	6B	9B	4L
10575	6B	4L	10175	6B	9B	4L
10576	6B	4L	10176	6B	9B	4L
10577	6B	4L	10177	6B	9B	4L
10579	6B	4L	10179	6B	9B	4L
10580			10180	6B	9B	
10581	6B	4L	10181	6B		4L
10586	6B	4L	10186	6B	9B	4L
10592	6B	4L	10192	6B	9B	4L
10610	6B	4L	10210	6B		4L
10611	6B	4L	10211	6B		4L
10612			10212	6B		
10631	6B	4L	10231	6B	9B	4L
10405			10405	6E		4B
10410			10410	6F	9B	4B
10411			10411	6F	9B	4B;
10414			10414	6E		4B
10415			10415	6E		4B
10416			10416	6E		4B

95K ECL

COMMERCIAL (C) INDUSTRIAL 0°C to 75°C	
DEVICE	CERAMIC DIP (D)
95000	6B
95002	6B
95003	6B
95004	6B
95010	6B
95016	6B
95029	6B
95101	6B
95102	6B
95103	6B
95105	6B
95106	6B
95107	6B
95109	6B
95110	6B
95111	6B
95115	6B
95116	6B
95124	6B
95130	6B
95231	6B

PACKAGE INFORMATION

100K ECL

COMMERCIAL (C) INDUSTRIAL 0°C to 75°C		
DEVICE	**CERAMIC DIP (D)**	**FLATPAK (F)**
100101	6Q	4Q
100102	6Q	4Q
100107	6Q	4Q
100112	6Q	4Q
100114	6Q	4Q
100117	6Q	4Q
100118	6Q	4Q
100122	6Q	4Q
100123	6Q	4Q
100130	6Q	4Q
100131	6Q	4Q
100136	6Q	4Q
100141	6Q	4Q
100142	6Q	4Q
100145	6Q	4Q
100151	6Q	4Q
100150	6Q	4Q
100155	6Q	4Q
100156	6Q	4Q
100158	6Q	4Q
100160	6Q	4Q
100163	6Q	4Q
100164	6Q	4Q
100165	6Q	4Q
100166	6Q	4Q
100170	6Q	4Q
100171	6Q	4Q
100179	6Q	4Q
100180	6Q	4Q
100181	6Q	4Q
100191	6Q	4Q
100414	6E	4B
100415	6E	4B
100416	6E	4B

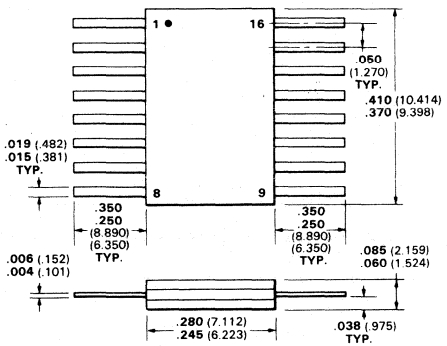
11C ECL

MILITARY -55°C to +125°C		COMMERCIAL (C) INDUSTRIAL 0°C to 75°C		
DEVICE	**CERAMIC DIP (D)**	**CERAMIC DIP (D)**	**PLASTIC DIP (P)**	**FLATPAK (F)**
11C01				4L
11C05	6A	6A		
11C06		6B		
11C24	6A	6A		
11C44	6A	6A		
11C58		6B		
11C70	6B	6B		
11C83		6A		
11C84		6B	9B	
11C85		6B		
11C90	6B	6B		
11X91	6B	6B		

PACKAGE OUTLINES

16-Pin Cerpak

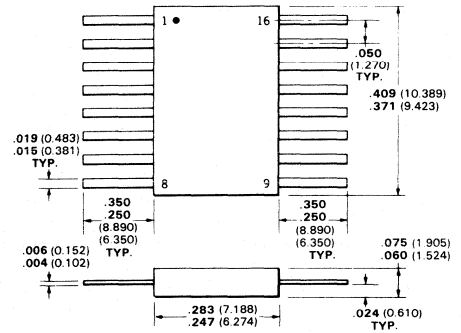
4B



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are tin plated nickel alloy 42 or kovar
Cap and base are BeO
Package weight is 0.4 gram

16-Pin Cerpak

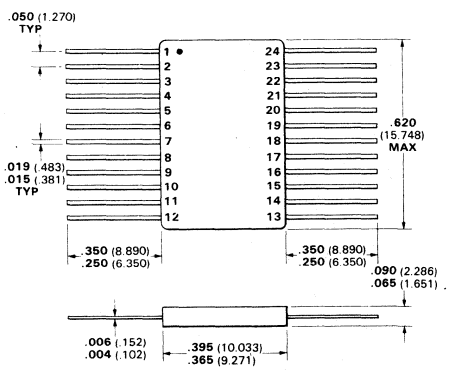
4L



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are alloy 42
Package weight is 0.4 gram
Hermetically sealed beryllia package

24-Pin BeO Cerpak

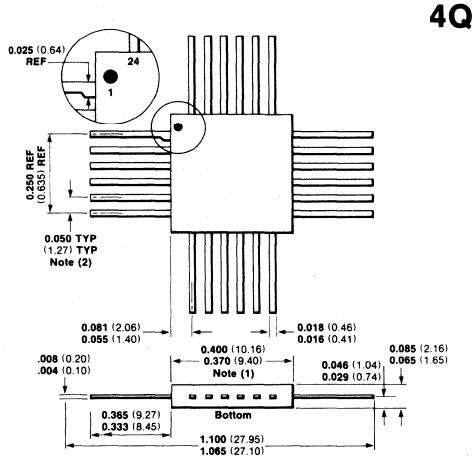
4M



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are alloy 42
Package weight is 0.8 gram
Hermetically sealed beryllia package

24-Pin Flatpak

4Q

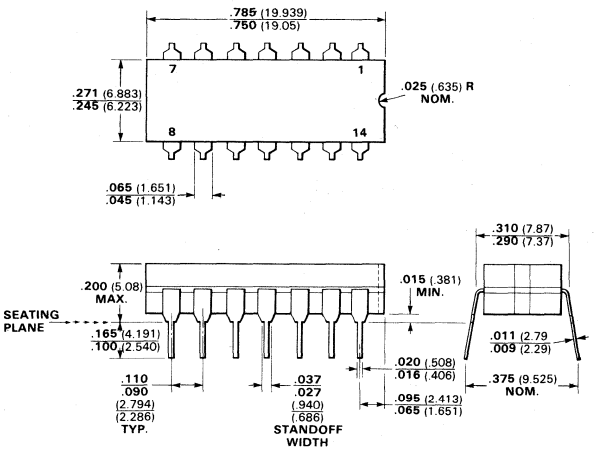


NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are tin plated nickel alloy
Base is AL203 or BeO
Package weight is ≈ 0.8 grams
(1) Dimension is 0.375 + 0.025/-0.005 to include misalignment and bonding material squeeze out
(2) Each lead location may vary +/- 0.005 (0.13) from designated datum line

PACKAGE OUTLINES

In accordance with JEDEC (TO-116) outline 14-Pin Ceramic Dual In-Line

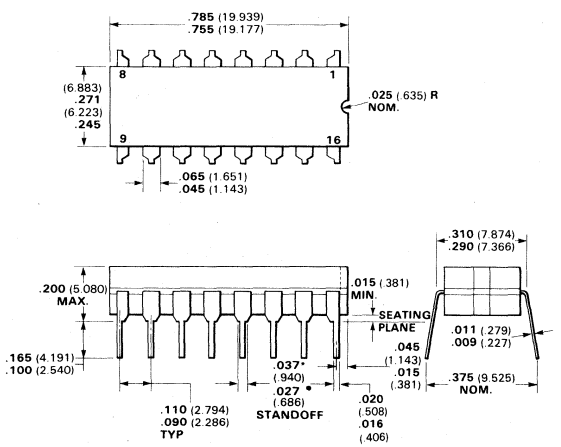
6A



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are intended for insertion in hole rows on .300" (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" (0.508) diameter pin
Pins are alloy 42
Package weight is 2.0 grams

16-Pin Ceramic Dual In-Line

6B

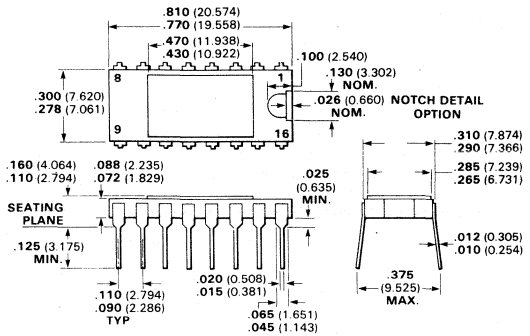


NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are intended for insertion in hole rows on .300" (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin
Pins are alloy 42
Package weight is 2.0 grams
*The .037/.027 (.940/.686) dimensions does not apply to the corner pins

PACKAGE OUTLINES

16-Pin Dual In-Line (Metal Cap)

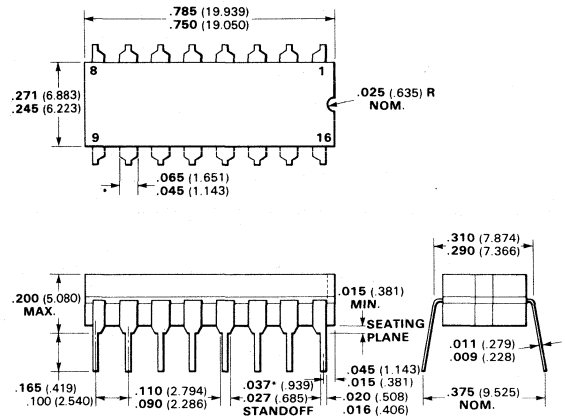
6E



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are gold-plated nickel alloy 42
Base is AL203
Cap is gold-plated kovar
Pins are intended for insertion in hole rows on .300 (.762) centers. They are purposely shipped with positive alignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 (.051) diameter pin
Package weight is 2.0 grams

16-Pin SSI Dual In-Line

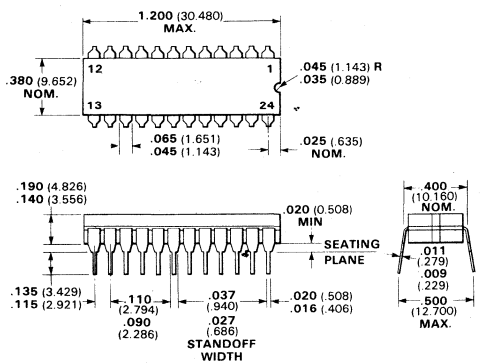
6F



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are tin-plated kovar or nickel alloy 42
Pins are intended for insertion in hole rows on .300 (7.62) centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .030 (0.76) diameter pins
Hermetically sealed alumina package (black)
*The .037-.027 (0.94/0.69) dimension does not apply to the corner pins
Package weight is 2.0 grams

24-Pin Ceramic Dual In-Line

6Q



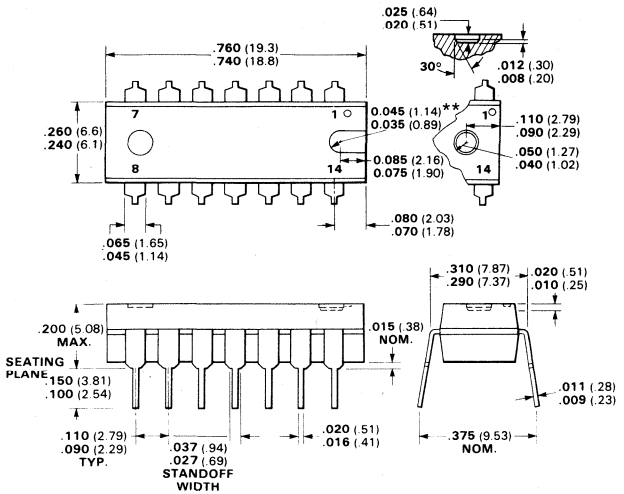
NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are intended for insertion in hole rows on .400" (10.16) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin
Pins are alloy 42

12

PACKAGE OUTLINES

14-Pin Plastic Dual In-Line

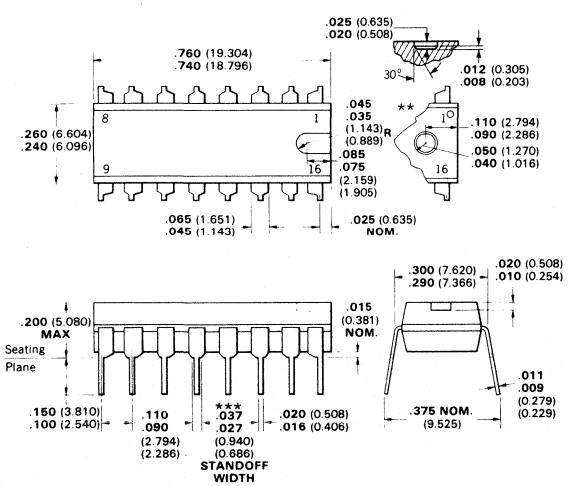
9A



NOTES:
All dimensions in inches (bold) and millimeters (parantheses)
Pins are intended for insertion in hole rows on .300" (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin
Pins are alloy 42
Package weight is 0.9 gram
Package material is silicone

16-Pin Plastic Dual In-Line

9B



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are alloy 42
Pins are intended for insertion in hole rows on .300" (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch (0.508) diameter pin
***The .037/.027 (.940/.686) dimension does not apply to the corner pins
Package weight is 0.9 gram

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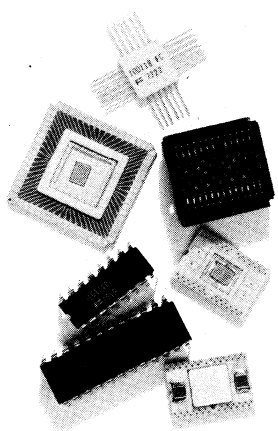
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Printed in Italy

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